TEK SERVICE MANUAL

070-4999-00
Product Group 41

2230
DIGITAL STORAGE OSCILLOSCOPE
SERVICE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

Please Check for CHANGE INFORMATION at the Rear of This Manual

First Printing JUL 1986
Revised MAY 1987

Tektronix
COMMITTED TO EXCELLENCE

Copyright © 1986 Tektronix, Inc. All rights reserved. Contents of this publication may not be reproduced in any form without the written permission of Tektronix, Inc.

Products of Tektronix, Inc. and its subsidiaries are covered by U.S. and foreign patents and/or pending patents.

TEKTRONIX, TEK, SCOPE-MOBILE, and are registered trademarks of Tektronix, Inc.

Printed in U.S.A. Specification and price change privileges are reserved.

INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

TABLE OF CONTENTS

Page

LIST OF ILLUSTRATIONS iv

LIST OF TABLES vi

OPERATORS SAFETY SUMMARY viii

SERVICING SAFETY SUMMARY ix

Section 1 GENERAL INFORMATION

INTRODUCTION 1-1
SPECIFICATION 1-1

Section 2 OPERATING INFORMATION

PREPARATION FOR USE 2-1
SAFETY 2-1
LINE VOLTAGE 2-1
POWER CORD 2-1
LINE FUSE 2-2
INSTRUMENT COOLING 2-2
START-UP 2-2
REPACKAGING 2-3
CONTROLS, CONNECTORS, AND INDICATORS 2-4
POWER AND DISPLAY 2-4
VERTICAL 2-4
HORIZONTAL 2-8
TRIGGER 2-12
STORAGE CONTROLS 2-15
MENU SELECTED FUNCTIONS 2-17
REAR PANEL 2-19
SIDE PANEL 2-19
CRT READOUT 2-20
OPERATING CONSIDERATIONS 2-23
GRATICULE 2-23
GROUNDING 2-23
SIGNAL CONNECTIONS 2-23
INPUT-COUPLING CAPACITOR PRECHARGING 2-24

Page

OPERATOR'S CHECKS AND ADJUSTMENTS 2-25
INITIAL SETUP 2-25
TRACE ROTATION ADJUSTMENT 2-26
PROBE COMPENSATION 2-26
HORIZONTAL ACCURACY CHECK 2-27

Section 3 THEORY OF OPERATION

SECTION ORGANIZATION 3-1
INTEGRATED CIRCUIT DESCRIPTIONS 3-1
GENERAL DESCRIPTION 3-1
DETAILED CIRCUIT DESCRIPTION 3-7
ANALOG CIRCUITRY 3-7
VERTICAL ATTENUATORS 3-7
VERTICAL PREAMPLIFIERS 3-10
VERTICAL OUTPUT AMPLIFIER 3-12
TRIGGERING 3-13
A SWEEP GENERATOR AND LOGIC 3-17
B TIMING AND ALTERNATE B SWEEP 3-20
HORIZONTAL 3-23
MICROPROCESSOR AND STORE-PANEL CONTROLS 3-25
STATUS ADC AND BUS INTERFACE 3-26
STORAGE ACQUISITION 3-28
ACQUISITION MEMORY 3-30
DIGITAL TIME BASE 3-38
DIGITAL DISPLAY 3-44
VECTOR GENERATOR 3-45
POWER INPUT, PREREGULATOR AND INVERTER 3-47
POWER SUPPLY SECONDARIES, Z-AXIS AND CRT 3-49
X-Y PLOTTER 3-51

TABLE OF CONTENTS (cont)

Page

Section 4 PERFORMANCE CHECK PROCEDURE

INTRODUCTION 4-1
PURPOSE 4-1
PERFORMANCE CHECK INTERVAL 4-1
STRUCTURE 4-1
TEST EQUIPMENT REQUIRED 4-1
LIMITS AND TOLERANCES 4-1
PREPARATION FOR CHECKS 4-1
INDEX TO PERFORMANCE CHECK STEPS 4-3
VERTICAL 4-4
INITIAL CONTROL SETTINGS 4-4
PROCEDURE STEPS 4-4
HORIZONTAL 4-12
INITIAL CONTROL SETTINGS 4-12
PROCEDURE STEPS 4-12
TRIGGER 4-17
INITIAL CONTROL SETTINGS 4-17
PROCEDURE STEPS 4-17
EXTERNAL Z-AXIS, PROBE ADJUST, EXTERNAL CLOCK, AND X-Y PLOTTER 4-21
INITIAL CONTROL SETTINGS 4-21
PROCEDURE STEPS 4-21

Section 5 ADJUSTMENT PROCEDURE

INTRODUCTION 5-1
PURPOSE 5-1
STRUCTURE 5-1
TEST EQUIPMENT 5-1
LIMITS AND TOLERANCES 5-1
ADJUSTMENTS AFFECTED BY REPAIRS 5-1
PREPARATION FOR ADJUSTMENT 5-1
INDEX TO ADJUSTMENT PROCEDURE STEPS 5-3
POWER SUPPLY AND CRT DISPLAY 5-4
INITIAL CONTROL SETTINGS 5-4
PROCEDURE STEPS 5-4

Page

VERTICAL 5-6
INITIAL CONTROL SETTINGS 5-6
PROCEDURE STEPS 5-6
HORIZONTAL 5-19
INITIAL CONTROL SETTINGS 5-19
PROCEDURE STEPS 5-19
TRIGGER 5-27
INITIAL CONTROL SETTINGS 5-27
PROCEDURE STEPS 5-27
EXTERNAL Z-AXIS, PROBE ADJUST, EXTERNAL CLOCK, AND X-Y PLOTTER 5-32
INITIAL CONTROL SETTINGS 5-32
PROCEDURE STEPS 5-32

Section 6 MAINTENANCE

STATIC-SENSITIVE COMPONENTS 6-1
PREVENTIVE MAINTENANCE 6-2
INTRODUCTION 6-2
GENERAL CARE 6-2
INSPECTION AND CLEANING 6-2
LUBRICATION 6-5
SEMICONDUCTOR CHECKS 6-5
PERIODIC READJUSTMENT 6-5
TROUBLESHOOTING 6-5
INTRODUCTION 6-5
TROUBLESHOOTING AIDS 6-5
TROUBLESHOOTING EQUIPMENT 6-11
TROUBLESHOOTING TECHNIQUES 6-11
DIAGNOSTICS 6-14
CORRECTIVE MAINTENANCE 6-31
INTRODUCTION 6-31
MAINTENANCE PRECAUTIONS 6-31
OBTAINING REPLACEMENT PARTS 6-31
MAINTENANCE AIDS 6-31
INTERCONNECTIONS 6-33
TRANSISTORS AND INTEGRATED CIRCUITS 6-33
SOLDERING TECHNIQUES 6-33
REMOVAL AND REPLACEMENT INSTRUCTIONS 6-34

TABLE OF CONTENTS (cont)

Page

Section 7 OPTIONS

INTRODUCTION 7-1
POWER CORD OPTIONS 7-1
OPTION 33 7-1
OPTION 10 AND OPTION 12 7-1
INTRODUCTION 7-1
STANDARD FUNCTIONS, FORMATS, AND FEATURES 7-2
PERFORMANCE CONDITIONS 7-3
OPTIONS SIDE PANEL 7-3
INTERFACE STATUS INDICATORS 7-8
MENU SELECTED FUNCTIONS 7-8
GPIB PARAMETER SELECTION 7-9
RS-232-C PARAMETER SELECTION 7-10
MESSAGES AND COMMUNICATION PROTOCOL 7-10
COMMAND LISTS 7-12
WAVEFORM TRANSFERS 7-28
REMOTE-LOCAL OPERATING STATES 7-31
INSTRUMENT RESPONSE TO INTERFACE MESSAGES 7-32
GPIB PROGRAMMING 7-33
RS-232-C PROGRAMMING 7-33
RESET UNDER COMMUNICATION OPTIONS CONTROL 7-34
STATUS AND ERROR REPORTING 7-34

Page

READOUT/MESSAGE COMMAND CHARACTER SET 7-35
ASCII CODE CHART 7-35
OPTION 10 THEORY OF OPERATION 7-40
OPTION 12 THEORY OF OPERATION 7-41
OPTION MEMORY 7-43
PERFORMANCE CHECK PROCEDURE 7-44
ADJUSTMENT PROCEDURE 7-45
OPTION MAINTENANCE INFORMATION 7-45

Section 8 REPLACEABLE ELECTRICAL PARTS

Section 9 DIAGRAMS

Section 10 REPLACEABLE MECHANICAL PARTS

CHANGE INFORMATION

Diagnostic Information:

Diagnostics 6-14
Diagnostic Messages 6-17
Diagnostic Tests 6-21

LIST OF ILLUSTRATIONS

Figure		Page
	The 2230 Digital Storage Oscilloscope	x
1-1	Maximum input voltage vs. frequency derating curve for CH 1 OR X, CH 2 OR Y, and EXT INPUT connectors	1-14
1-2	Physical Dimensions of the 2230 Oscilloscope	1-15
2-1	Securing the detachable power-cord to the instrument	2-1
2-2	Optional power cord data	2-2
2-3	Fuse holder and detachable power-cord connector	2-2
2-4	Power and display controls and power-on indicator	2-5
2-5	Vertical controls and connectors	2-6
2-6	Horizontal controls	2-9
2-7	Trigger controls, connector, and indicator	2-12
2-8	Storage controls	2-15
2-9	Rear-panel	2-19
2-10	Side Panel	2-20
2-11	X-Y Plotter interfacing	2-21
2-12	Crt readout display	2-22
2-13	Graticule measurement markings	2-23
2-26	Probe compensation	2-26
3-1	Simplified block diagram	3-2
3-2	Block diagram of the Channel 1 Attenuator circuit	3-8
3-3	Store-Non Store Vertical Switching	3-11
3-4	Block diagram of Trigger Amplifiers and Switching	3-14
3-5	A Sweep Generator and Logic Circuitry	3-18
3-6	Horizontal Amplifier block diagram	3-24
3-7	Sampling mode acquisition timing at 0.05 μs per division (ADCLK = CONV = 20 MHz)	3-31
3-8	MIN/MAX Acquisition timing at 20 μs per division	3-33
3-9	Acquisition Memory timing	3-37
3-10	Clock timing	3-39
3-11	Simplified diagram of the Dc Restorer circuitry	3-50
6-1	Multi-connector holder orientation	6-7
6-2	Grounding the signal lines of P2111 and P2112	6-7
6-3	Isolated kernel timing	6-9
6-4	Diagnostic Menu	6-19
6-5	Error code timing (U4119)	6-20
6-6	PU error display	6-21
6-7	Location of screws and spacers on the Storage circuit board	6-37
6-8	Recessed screw and rear hinge removal	6-38
6-9	Location of screws securing Power-Supply shield and the support bracket to the rear chassis frame	6-40
7-1	Option side panels	7-4
7-2	Interface status indicators	7-8

LIST OF ILLUSTRATIONS (cont)

Figure

9-1 Color codes for resistors and capacitors.
9-2 Semiconductor lead configurations.
9-3 Locating components on schematic diagrams and circuit board illustrations.
9-4 Detailed analog block diagram
9-5 Detailed storage block diagram.
9-6 A2—Attenuator board.
9-7 A14—CH 1 Logic board.
9-8 A14—CH 2 Logic board.
9-9 A1—Main board.
9-10 Circuit view of A1—Main board.
9-11 A17—Position Interface board.
9-12 A3—Front Panel board.
9-13 Circuit view of A3—Front Panel board.
9-14 A4—Timing board.
9-15 A13—Sweep Interface board.
9-16 A5—Alternate Sweep board.
9-17 A16—Sweep Reference board.
9-18 A6—Line Filter board.
9-19 A18—Thermal Shutdown board.
9-20 A7—Intensity Pot board.
9-21 A10—Storage board.
9-22 A11A1—Input/Output board.
9-23 A11A2—Vector Generator board.
9-24 A20—X-Y Plotter board.
9-25 A21—RS-232 Option board.
9-26 A22—GPIB Option board.
9-27 A23—Option Memory board.

LIST OF TABLES

Table		Page
1-1	Electrical Characteristics	1-3
1-2	Environmental Characteristics	1-13
1-3	Physical Characteristics	1-14
2-1	Probe Coding	2-7
2-2	Default Digital Storage Modes	2-9
2-3	Repetitive Store Sampling Data Acquisition	2-10
2-4	Auxiliary Connector	2-20
3-1	Memory Space Allocation	3-27
3-2	MIN/MAX Clock Selector Multiplexer Switching	3-32
3-3	Time Base Clock Frequencies	3-41
3-4	Time Base Divider Preload Bits	3-42
3-5	Trigger Logic Multiplexer Switching	3-43
4-1	Test Equipment Required	4-2
4-2	Deflection Accuracy Limits	4-4
4-3	Storage Deflection Accuracy	4-5
4-4	Settings for Bandwidth Checks	4-7
4-5	Settings for Timing Accuracy Checks	4-13
4-6	Settings for Delay Time Differential Checks	4-15
4-7	Switch Combinations for A Triggering Checks	4-18
5-1	Adjustments Affected by Repairs	5-2
5-2	Power Supply Limits	5-5
5-3	Deflection Accuracy Limits	5-8
5-4	Store Deflection Accuracy	5-10
5-5	Attenuator Compensation Adjustments	5-12
5-6	Settings for Bandwidth Checks	5-16
5-7	Settings for Timing Accuracy Checks	5-23
5-8	Settings for Delay Time Differential Checks	5-24
5-9	Switch Combinations for A Triggering Checks	5-28
6-1	Relative Susceptibility to Static-Discharge Damage	6-1
6-2	External Inspection Checklist	6-3
6-3	Internal Inspection Checklist	6-3
6-4	Timing Switch Interface Voltages	6-10
6-5	Vertical VOLTS/DIV Switch Interface Voltages	6-11
6-6	AC GND DC Switch Interface Voltages	6-11
6-7	Power Supply Voltage and Ripple Limits	6-12
6-8	Diagnostic Messages and Tests	6-14
6-9	Circuitry Checked by Each Test and Exerciser	6-15
6-10	U4119 Error Code Display	6-16
6-11	Diagnostic Messages	6-17
6-12	Diagnostic Acquisition Values	6-20
6-13	PU TEST Failure Codes	6-22
6-14	Acquisition Address Bus Test Patterns	6-23

LIST OF TABLES (cont)

Table		Page
6-15	PRC Test Patterns	6-24
6-16	Display Format	6-28
6-17	Display Format Bit Definitions	6-28
6-18	ACQ_MEM 0x48000	6-29
6-19	ACQ_MODE 0x437BE	6-29
6-20	TB_MODE 0x407DE	6-29
6-21	TB_SWP_RATE 0x407EE	6-29
6-22	FP_A/D_CTL 0x437F6	6-29
6-23	Display Format Digit Definitions	6-30
6-24	Maintenance Aids	6-32
7-1	Function Subsets Implemented	7-2
7-2	Specific Format Choices	7-3
7-3	Implementation of Specific Features	7-3
7-4	Option Electrical Characteristics	7-4
7-5	GPIB Connector	7-5
7-6	GPIB PARAMETERS Switch	7-5
7-7	RS-232-C PARAMETERS Switch	7-6
7-8	Baud Rate	7-6
7-9	Parity Selection	7-7
7-10	RS-232-C DTE Connector	7-7
7-11	RS-232-C DCE Connector	7-7
7-12	Numeric Argument Format for Commands	7-12
7-13	Vertical Commands	7-13
7-14	Horizontal Commands	7-14
7-15	Trigger Commands	7-15
7-16	Cursor Commands	7-16
7-17	Display Commands	7-17
7-18	Acquisition Commands	7-18
7-19	Save and Recall Reference Commands	7-20
7-20	Waveform Commands	7-22
7-21	Waveform Preamble Fields	7-23
7-22	Service Request Group Commands	7-25
7-23	Miscellaneous Commands	7-26
7-24	RS-232-C Specific Commands	7-26
7-25	Query and Response Examples	7-27
7-26	Typical 8-Bit Binary Waveform Data	7-29
7-27	Typical 16-Bit Binary Waveform Data	7-30
7-28	Typical 8-Bit Hexadecimal Waveform Data	7-30
7-29	Typical 16-Bit Hexadecimal Waveform Data	7-31
7-30	Typical ASCII Waveform Data	7-31
7-31	Status Event and Error Categories	7-35
7-32	Event Codes	7-36
7-33	Readout/MESsage Command Character Set	7-38
7-34	ASCII Code Chart	7-39
7-35	GPIB Status Buffer Functions	7-41
7-36	RS-232-C Status Buffer Functions	7-43
7-37	Test Equipment Required	7-44

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltage see Table 1-2.

Symbols as Marked on Equipment

DANGER — High voltage.

Protective gound (earth) terminal.

ATTENTION — Refer to manual.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors, see Figure 2-2.

Use the Proper Fuse

To avoid fire hazard, use only a fuse of the correct type, voltage rating and current rating as specified in the parts list for your product.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

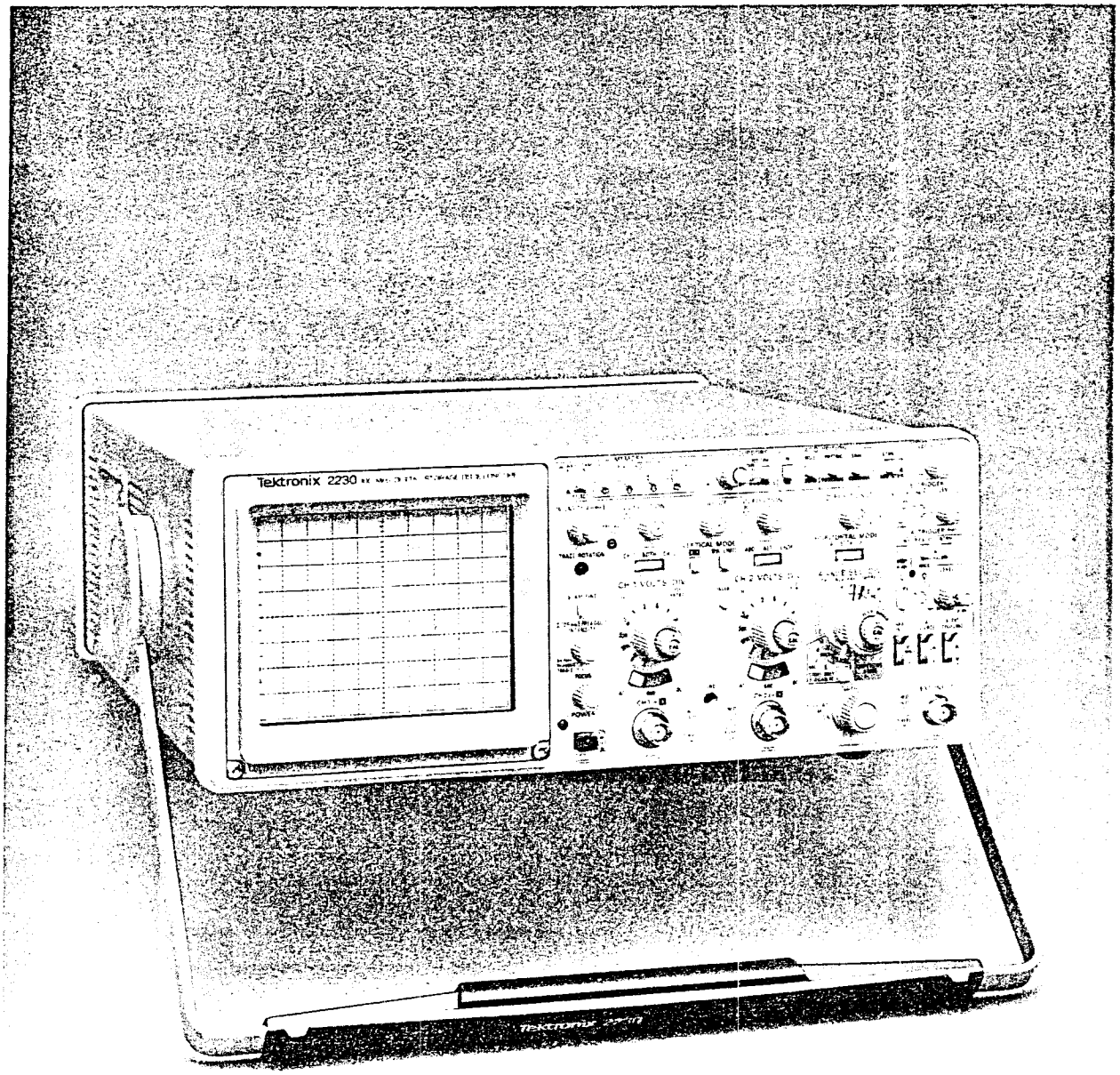
Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding connector in the power cord is essential for safe operation.



4998-01

The 2230 Digital Storage Oscilloscope.

GENERAL INFORMATION

INTRODUCTION

The TEKTRONIX 2230 Oscilloscope is a combination nonstorage and digital storage dual-channel 100 MHz bandwidth instrument. It is a rugged, lightweight oscilloscope featuring microprocessor operation and alphanumeric crt readout of many of the front-panel controls. In the digital storage mode, up to three waveform sets (CH 1 and/or CH 2) may be stored in a SAVE REF memory and recalled for display at a later time. The vertical system provides calibrated deflection factors from 2 mV per division to 5 V per division. The horizontal system provides calibrated sweep speeds from 50 ns per division to 0.5 s per division for nonstorage mode with three slower sweep speeds (1 s, 2 s, and 5 s per division) added for store mode operation. A X10 magnifier extends the maximum sweep speed to 5 ns per division.

The digital storage sampling rate is 20 megasamples per second maximum, and the acquired record length is 4K samples (1K may also be selected) for a single channel or 2K samples for dual-channel (CHOP or ALT) displays. Any contiguous 1K sample of an acquired record is displayable. The fast sampling rate can capture a glitch with a pulse width of at least 100 ns. A 4K compress feature enables a 4K record length acquisition to be compressed to 1K in length for ease in viewing or storing in the SAVE REF memory. If compression is not desired, all 4K or any 1K portion of a 4K record may be stored in the SAVE REF memory. The SAVE store mode stops the waveform acquisition in progress, allowing a particular display to be stored or examined before further acquisitions cause a waveform update.

Cursors may be used to obtain voltage measurements, time difference measurements, and delay-time measurements on any of the store mode waveform displays. Delta volts, delay time, delta time, and 1/delta time (either delta time or 1/delta time is selectable via the MENU) are displayed in the crt readout for ease in obtaining precise measurement results. The cursors are positioned to any displayed store mode waveform to make measurements. An alternate use of the cursor-positioning control is to horizontally position the 1K display window to any location within a 4K record length waveform acquisition. The displayed portion of a 4K acquisition is stored when the SAVE REF feature is used.

The instrument is shipped with the following standard accessories:

- 1 Operators Manual
- 1 Users Reference Guide
- 2 Probe Packages
- 1 Front Panel Cover
- 1 Accessory Pouch
- 1 Power Cord
- 1 Fuse
- 1 DB-9 Male Connector and Connector Shell
- 1 Loop Clamp
- 1 Flat Washer
- 1 Self-Tapping Screw

For part numbers and further information about both standard and optional accessories, refer to "Options and Accessories" (Section 7) of this manual. Your Tektronix representative, local Tektronix Field Office, or Tektronix products catalog can also provide additional accessories information.

SPECIFICATION

The following electrical characteristics (Table 1-1) are valid when the instrument has been adjusted at an ambient temperature between +20°C and +30°C, has had a warm-up period of at least 20 minutes, and is operating at an ambient temperature between 0°C and +50°C (unless otherwise noted).

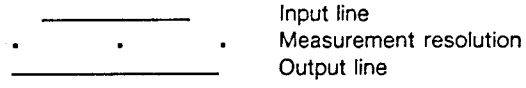
Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 1-2. This instrument meets the requirements of MIL-T-28800C for Type III, Class 5 equipment, except where noted otherwise.

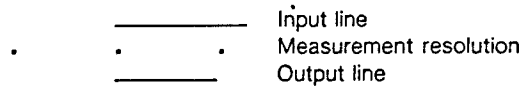
Physical characteristics of the instrument are listed in Table 1-3.

Finite resolution affects any measurement using discrete numbers. All digital storage stores amplitude values as discrete numbers and associates those amplitude numbers with discretely numbered times. Many measurements must be rounded or truncated. The size of the truncation or rounding becomes a part of the measurement error. For example, the following line is 1.5 units long. If it must be drawn as a line connecting points one unit apart, then it may be drawn as a line one unit long or two units long, depending on how it occurs relative to the points.

Case 1: Line approaches three points:



Case 2: Line approaches two points:



There are several places where measurements are quantified, and a one-count error in the measurement cannot be detected. The input channels are digitized to an 8-bit resolution, where one division is (ignoring expansion and compression) 25 counts. This means there is an inherent error of 1/25 of a division in any voltage measurement at acquisition time. Averaging can increase the resolution of a voltage measurement above the sampler's eight-bit limit. To use the increased resolution, the display has a 10-bit dynamic range in the vertical axis, as well as the horizontal axis. An averaged signal has a resolution of 100 points per division (ignoring expansion and compression). In addition, the averaged number is stored with up to twelve bits of resolution. Expansion is required to view the eleventh and twelfth bits of increased resolution.

Time is quantified to determine when each sample occurred and which display interval gets each sample. Time is resolved by storing, for example, 4K points. If 4K points are stored, 4K time intervals are represented. However, in 4K mode, not all of the 4K-point resolution may be displayed on the 10-bit (1K-point) screen. Therefore, if 4K COMPRESS is selected to present the whole picture on-screen at once, only 1K resolution remains in the display. When peak-detected information is acquired, events with high-frequency content such as fast steps, or short pulses, can only be located within the time interval from which the peaks came. Even though two display points result from the interval, the event cannot be tied with certainty to the first or second point in the interval.

Time is also quantified to determine where to put points in REPETITIVE acquisitions, where the points acquired at 50 ns intervals fill only part of the screen. A counting device produces a number to represent the portion of 50 ns between the samples acquired and the ones that would have included the trigger. This number ranges from 0 to about 205, which allows accurate placement into the display record. The display record will have at most 100 slots to choose from on the basis of the 0-205 number (this is where each slot represents 0.5 ns of acquisition time, and the counter's resolution is about 0.244 ns per count).

Table 1-1

Electrical Characteristics

Characteristics	Performance Requirements
VERTICAL DEFLECTION SYSTEM	
Deflection Factor	
Range	2 mV/div to 5 V/div in a 1-2-5 sequence.
DC Accuracy (NON STORE)	
+15°C to +35°C	Within ±2%.
0°C to +50°C	Within ±3%.[a] For 5 mV/div to 5 V/div VOLTS/DIV switch settings, the gain is set at a VOLTS/DIV switch setting of 10 mV/div. 2 mV/div gain is set with the VOLTS/DIV switch set to 2 mV/div.
On Screen DC Accuracy (STORE)	
+15°C to +35°C	Within ±2%.
0°C to +50°C	Within ±3%.[a] STORE Mode gain set with the VOLTS/DIV switch set to 5 mV/div.
Storage Acquisition Vertical Resolution	8 bits, 25 levels per division. 10.24 divisions dynamic range.[a]
Range of VOLTS/DIV Variable Control	Continuously variable between settings. Increases deflection factor by at least 2.5 to 1.
Step Response (NON STORE)	
Rise Time	
0°C to +35°C	
5 mV/div to 5 V/div	3.5 ns or less.[a]
2 mV/div	4.4 ns or less.[a]
+35°C to +50°C	
5 mV/div to 5 V/div	3.9 ns or less.[a]
2 mV/div	4.4 ns or less.[a] Rise time is calculated from: $\text{Rise Time} = \frac{0.35}{\text{Bandwidth } (-3 \text{ dB})}$
Step Response (STORE Mode)	
Useful Storage Rise Time	**Single Trace** / **CHOP/ALT**
SAMPLE	$\frac{\text{SEC/DIV} \times 1.6}{100}$ s[a] / $\frac{\text{SEC/DIV} \times 1.6}{50}$ s[a]
PEAKDET or ACCPEAK with SMOOTH	$\frac{\text{SEC/DIV} \times 1.6}{50}$ s[a] / $\frac{\text{SEC/DIV} \times 1.6}{25}$ s[a] Rise time is limited to 3.5 ns minimum with derating over temperature (see NON STORE Rise Time).

[a]**Performance Requirement not checked in Service Manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
Aberrations (NON STORE and STORE in Default Modes)	
2 mV/div to 50 mV/div	+4%, −4%, 4% p-p. 3% or less at +25°C with cabinet installed.
0.1 V/div to 0.5 V/div	+6%, −6%, 6% p-p. 5% or less at +25°C with cabinet installed.
1 V/div to 5 V/div	+12%, −12%, 12% p-p.[a] 10% or less at +25°C with cabinet installed. Measured with a five-division reference signal, from a 50 Ω source driving a 50 Ω coaxial cable terminated in 50 Ω at the input connector with the VOLTS/DIV Variable control in the CAL detent. Vertically center the top of the reference signal.
NON STORE Bandwidth (−3 dB)	
0°C to +35°C	
5 mV/div to 5 V/div	DC to at least 100 MHz.
2 mV/div	DC to at least 80 MHz.
+35°C to +50°C	
2 mV/div to 5 V/div	DC to at least 80 MHz.[a] Measured with a vertically centered six-division reference signal, from a 50 Ω source driving a 50 Ω coaxial cable terminated in 50 Ω at the input connector; with the VOLTS/DIV Variable control in the CAL detent.
NON STORE BW LIMIT (−3 dB)	20 MHz ±10%.
AC Coupled Lower Cutoff Frequency	10 Hz or less at −3 dB.[a]
Useful Storage Performance	
RECORD, SCAN and ROLL Store Modes	
SAMPLE Acquisition, no AVERAGE	**Single Trace** **CHOP/ALT**
5 μs/div to 5 s/div	$\frac{10}{\text{SEC/DIV}}$ Hz[a] $\frac{5}{\text{SEC/DIV}}$ Hz[a]
EXT CLOCK (up to 1 kHz)	$\frac{\text{EXT}}{10}$ Hz[a] $\frac{\text{EXT}}{20}$ Hz[a]
	Useful storage performance is limited to the frequency where there are 10 samples per sine wave signal period at the maximum sampling rate. (Maximum sampling rate is 20 MHz in Single trace and 10 MHz in CHOP or ALT at a SEC/DIV setting of 5 μs/div.) This yields a maximum amplitude uncertainty of 5%. Accuracy at the useful storage bandwidth limit is measured with respect to a six-division 50 kHz reference sine wave.
PEAK DETECT	**Single Trace and ALT** **CHOP**
Sine-Wave Amplitude Capture (5% p-p maximum amplitude uncertainty)	1 MHz[a] 1 MHz[a]
Pulse Width Amplitude Capture (50% p-p maximum amplitude uncertainty)	100 ns $\frac{\text{SEC/DIV}}{50}$

[a]Performance Requirement not checked in Service Manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	
REPETITIVE Store Mode		
SAMPLE and AVERAGE	**Single Trace**	**ALT**
0.05 μs/div	100 MHz (−3 dB)[b]	100 MHz (−3 dB)[b]
0.1 μs/div	100 MHz (−3 dB)[a, b]	50 MHz (−3 dB)[a]
0.2 μs/div to 2 μs/div (5% maximum amplitude uncertainty)	$\frac{10}{\text{SEC/DIV}}$ Hz[a]	$\frac{5}{\text{SEC/DIV}}$ Hz[a]
ACCPEAK		
0.05 μs/div to 5 s/div	Same as NON STORE Bandwidth.[a]	
AVERAGE Mode		
Sweep Limit	Adjustable from 1 to 2047 or NO LIMIT.	
Weight of Last Acquisition	1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, or 1/256 (MENU selections).[a] AVERAGE mode default weight is 1/4.	
Resolution	Assuming uncorrelated triggers and greater than 1 LSB of the 8-bit acquisition of vertical signal noise; the averaging weight for the first acquistion is 1, the averaging weight for the second acquisition is 1/2 and for n acquisitions is $1/2^{n-1}$. The MENU selects the least weight used. Maximum signal-to-noise improvement is achieved after 2 × (weight factor) × (expected acquisitions to fill).[a]	
Frequency Response	Frequency response of the AVERAGE Storage Mode is a function of the number of triggered acquisitions added to the weighted average.[a] Time jitter of a signal with respect to the sample clock will produce a low-pass filter characteristic of an averaged waveform.	
NON STORE CHOP Mode Switching Rate	500 kHz ±30%.[a]	
STORE Chop Rate		
SAMPLE	50/(SEC/DIV) for sweep speeds from 5 s per division to and including 10 μs per division.[a]	
PEAK DETECT	25/(SEC/DIV) for sweep speeds from 5 s per division to and including 20 μs per division.[a]	
5 μs/div through 0.05 μs/div	No CHOP mode; acts as in ALT.[a]	
A/D Converter Linearity	Monotonic with no missing codes.[a]	
STORE Mode Cross Talk	<2% measured in CHOP at 10 μs/div and 10 mV/div using a 100 kHz square wave signal vertically centered and the other input coupling set to ground.	

[a]**Performance Requirement not checked in Service Manual.**

[b]**One-hundred MHz bandwidth is derated for temperature outside 0°C to +35°C and at 2 mV per division as for NON STORE.**

Table 1-1 (cont)

Characteristics	Performance Requirements
NON STORE Common-Mode Rejection Ratio (CMRR)	At least 10 to 1 at 50 MHz. Checked at 10 mV per division for common-mode signals of six divisions or less with the VOLTS/DIV Variable control adjusted for the best CMRR at 50 kHz.
Input Current	1 nA or less (0.5 division or less trace shift when switching between DC and GND input coupling with the VOLTS/DIV switch set to 2 mV per division.[a]
Input Characteristics	
Resistance	1 MΩ ±2%.[a]
Capacitance	20 pF ±2 pF.[a]
Maximum Safe Input Voltage (CH 1 and CH 2) ⚠	400 V (dc + peak ac) or 800 V ac p-p at 10 kHz or less.[a] See Figure 1-1 for maximum input voltage vs. frequency derating curve.
NON STORE Channel Isolation*	Greater than 100 to 1 at 50 MHz.
STORE Channel Isolation	100 to 1 at 50 MHz.
POSITION Control Range	At least ±11 divisions from graticule center.
A/B SWP SEP Control Range (NON STORE Mode Only)	±3.5 divisions or greater.
Trace Shift with VOLTS/DIV Switch Rotation	0.75 division or less; VOLTS/DIV Variable control in the CAL detent.[a]
Trace Shift as the VOLTS/DIV Variable Control is Rotated	1 division or less.[a]
Trace Shift with INVERT	1.5 division or less.[a]

[a]Performance Requirement not checked in Service Manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING SYSTEM	
A Trigger Sensitivity	
P-P AUTO and NORM	**10 MHz** **60 MHz** **100 MHz**
Internal	0.35 div 1.0 div 1.5 div
External	40 mV 120 mV 150 mV
	External trigger signal from a 50 Ω source driving a 50 Ω coaxial cable terminated in 50 Ω at the input connector.
HF REJ Coupling	Reduces trigger signal amplitude at high frequencies by about 20 dB with rolloff beginning at 40 kHz ±15 kHz. Should not trigger with a one-division peak-to-peak 250 kHz signal when HF REJ is ON.
P-P AUTO Lowest Usable Frequency	20 Hz with 1 division internal or 100 mV external.[a]
TV LINE	
Internal	0.35 div.[a]
External	35 mV p-p.[a]
TV FIELD	⩾ 1 division of composite sync.[a]
B Trigger Sensitivity (Internal Only)	**10 MHz** **60 MHz** **100 MHz**
	0.35 div 1.0 div 1.5 div
EXT INPUT	
Maximum Input Voltage ⚠	400 V (dc + peak ac) or 800 V ac p-p at 10 kHz or less.[a] See Figure 1-1 for maximum input voltage vs frequency derating curve.
Input Resistance	1 MΩ ±2%.[a]
Input Capacitance	20 pF ±2.5 pF.[a]
AC Coupled Lower Cutoff Frequency	10 Hz or less at −3 dB.[a]
LEVEL Control Range	
A Trigger (NORM)	
INT	May be set at any voltage level of the trace that can be displayed.[a]
EXT, DC	At least ±1.6 V, 3.2 V p-p.
EXT, DC÷10	At least ±16 V, 32 V p-p.[a]
B Trigger (Internal)	May be set at any point of the trace that can be displayed.[a]
VAR HOLDOFF Control (NON STORE Holdoff)	Increases NON STORE A Sweep holdoff time by at least a factor of 10.[a] STORE holdoff is a function of microprocessor activity and the pretrigger acquisition. The VAR HOLDOFF control maintains some control over the STORE holdoff by preventing a new trigger from being accepted by the storage circuitry until the next (or current, if one is in progress) NON STORE holdoff has completed.
Acquisition Window Trigger Point	
PRETRIG	Seven-eighths of the waveform acquisition window is prior to the trigger (other trigger points are selectable via the MENU).
POST TRIG	One-eighth of the waveform acquisition window is prior to the trigger (other trigger points are selectable via the MENU).

[a]**Performance Requirement not checked in Service Manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
HORIZONTAL DEFLECTION SYSTEM	
NON STORE Sweep Rates	
Calibrated Range	
A Sweep	0.5 sec per division to 0.05 μs per division in a 1-2-5 sequence of 22 steps.[c]
B Sweep	50 ms per division to 0.05 μs per division in a 1-2-5 sequence of 19 steps.[c]
STORE Mode Ranges	
REPETITIVE	0.05 μs per division to 2 μs per division.[a, d]
RECORD	5 μs per division to 50 ms per division.[a, d]
ROLL/SCAN	0.1 s per division to 5 s per division (A sweep only)[a, d]
NON STORE Accuracy	**Unmagnified** **Magnified**
+15°C to +35°C	Within ±2% Within ±3%
0°C to +50°C	Within ±3%[a] Within ±4%[a]
	Sweep accuracy applies over the center eight divisions. Exclude the first 40 ns of the sweep for magnified sweeps and anything beyond the 100th magnified division.
STORE Accuracy	See Horizontal Differential Accuracy and Cursor Time Difference Accuracy.[a]
NON STORE Sweep Linearity	±5%. Linearity measured over any two of the center eight divisions. Exclude the first 25 ns and anything past the 100th division of the X10 magnified sweeps.
Digital Sample Rate	**Single Trace** **CHOP/ALT**
SAMPLE (5 μs/div to 5 s/div)	$\frac{100}{\text{SEC/DIV}}$ Hz[a] $\frac{50}{\text{SEC/DIV}}$ Hz[a]
PEAKDET or ACCPEAK (20 μs/div to 5 s/div)	10 MHz[a] 10 MHz[a] (50% duty factor on each channel in CHOP)
REPETITIVE Store	
0.05 μs/div to 1 μs/div	20 MHz[a] 20 MHz[a]
2 μs/div	10 MHz[a] 10 MHz[a]
External Clock	
Input Frequency	Up to 1 kHz.
Digital Sample Rate	10 MHz in ACCPEAK and PEAKDET, otherwise it is equal to the input frequency.[a]
Store Rate	One data pair for every second falling edge.[a]
Duty Cycle	10% or greater (100 μs minimum hold time).[a]
Ext Clock Logic Thresholds	TTL Compatible.[a]
Maximum Safe Input Voltage ⚠	25 V (dc + peak ac) or 25 V p-p ac at 1 kHz or less.[a]
Input Resistance	>20 kΩ.[a]

[a] **Performance Requirement not checked in Service Manual.**

[c] **The X10 MAG control extends the maximum sweep speed to 5 ns per division.**

[d] **The X10 MAG control extends the maximum sweep speed to 5 ns per division. The 4K COMPRESS control multiplies the SEC/DIV by 4.**

Table 1-1 (cont)

Characteristics	Performance Requirements
STORE Mode Dynamic Range	10.24 divisions.[a]
STORE Mode Resolution	
Acquisition Record Length	1024 or 4096 data points.[a]
Single Waveform Acquisition Display	1024 data points (100 data points per division across the graticule area).[a]
CHOP or ALT Acquisition Display	512 data points (50 data points per division across the graticule area).[a]
Horizontal POSITION Control Range (NON STORE)	Start of the 10th division will position past the center vertical graticule line; 100th division in X10 magnified.
Horizontal Variable Sweep Control Range	
NON STORE	Continuously variable between calibrated settings of the SEC/DIV switch. Extends the A and the B Sweep speeds by at least a factor of 2.5 times over the calibrated SEC/DIV settings.
STORE	Horizontal Variable Sweep has no affect on the STORE Mode time base. Rotating the Variable SEC/DIV control out of the CAL detent position horizontally compresses a 4K point acquisition record to 1K points in length, so that the whole record length can be viewed on screen. Screen readout is altered accordingly.
Displayed Trace Length	
NON STORE	Greater than 10 divisions.
STORE	10.24 divisions.[a]
Delay Time	
0.5 μs per division to 0.5 sec per division (A Sweep)	
Delay POSITION Range	Less than (0.5 div + 300 ns) to greater than 10 divisions. Delay Time is functional, but not calibrated, at A Sweep speeds faster than 0.5 μs per division.
NON STORE Delay Jitter	One part or less in 5,000 (0.02%) of the maximum available delay time.
Delay Time Differential Measurement Accuracy (Runs After Delay only)	
+15°C to +35°C	±1% of reading, ±0.3% of full scale (10 div).
0°C to +50°C	±2% of reading, ±0.3% of full scale (10 div).[a] Exclude delayed operation when the A and B SEC/DIV knobs are locked together at any sweep speed or when the A SEC/DIV switch is faster than 0.5 μs per division. Accuracy applies over the B DELAY TIME POSITION control range.

[a]Performance Requirement not checked in Service Manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
DIGITAL STORAGE DISPLAY	
Vertical	
Resolution	10 bits (1 part in 1024).[a] Display waveforms are calibrated for 100 data points per division.
Differential Accuracy	Graticule indication of the voltage cursor difference is within 2% of the readout value, measured over the center six divisions.
POSITION Range	Any portion of a stored waveform vertically magnified or compressed up to 10 times can be positioned to the top and to the bottom of the graticule area.
Position Registration	
NON STORE to STORE	Within ±0.5 division at graticule center at VOLTS/DIV switch settings from 2 mV per division to 5 V per division.
CONTINUE to SAVE	Within ±0.5 division at VOLTS/DIV switch settings from 2 mV per division to 5 V per division.
SAVE Mode Expansion or Compression Range	Up to 10 times as determined by the remaining VOLTS/DIV switch positions up or down. 2 mV per division acquisitions cannot be expanded, and 5 V per division acquisitions cannot be compressed.
Storage Display Expansion Algorithm Error	±0.1% of full scale.[a]
Storage Display Compression Algorithm Error	+0.16% of reading ±0.4% of full scale.[a]
Horizontal	
Resolution	10 bits (1 part in 1024).[a] Calibrated for 100 data points per division.
Differential Accuracy	Graticule indication of time cursor difference is within ±2% of the readout value, measured over the center eight divisions.
SAVE Mode Expansion Range	
Y-T Mode	10 times as determined by the X10 MAG switch.
Expansion Accuracy	Same as the Vertical.[a]

[a]**Performance Requirement not checked in Service Manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
DIGITAL READOUT DISPLAY	
CURSOR Accuracy	
Voltage Difference	Within ±3% of the ΔV readout value.
Time Difference	
RECORD or ROLL/SCAN	
SAMPLE or AVERAGE	±1 display interval.[a]
PEAKDET or ACCPEAK	±2 display intervals.
REPETITIVE	
SAMPLE or AVERAGE	±(2 display intervals + 0.5 ns).
ACCPEAK	± (4 display intervals + 0.5 ns).[a] A display interval is the time between two adjacent display points on a waveform.
X-Y OPERATION (X1 MAGNIFICATION ONLY)	
Deflection Factors	Same as vertical deflection system with the VOLTS/DIV Variable controls in the CAL detent position.
NON STORE Accuracy	Measured with a dc-coupled, five-division reference signal.
X-Axis	
+15°C to +35°C	Within ±3%.
0°C to +50°C	Within ±4%.[a]
Y-Axis	Same as vertical deflection system.[a]
NON STORE Bandwidth (−3 dB)	Measured with a five-division reference signal.
X-Axis	DC to at least 2.5 MHz.
Y-Axis	Same as vertical deflection system.[a]
NON STORE Phase Difference Between X-Axis and Y-Axis Amplifiers	±3 degrees or less from dc to 150 kHz.[a] Vertical Input Coupling set to DC.
STORE Accuracy	
X-Axis and Y-Axis	Same as digital storage vertical deflection system.[a]
Useful Storage Bandwidth	
RECORD and REPETITIVE Store Modes	$\frac{5}{\text{SEC/DIV}}$ Hz[a]
STORE Mode Time Difference Between Y-Axis and X-Axis Signals	
RECORD, SCAN, and ROLL Modes	100 ns. The X-Axis signal is sampled before the Y-Axis signal.[a]
REPETITIVE Store	$\frac{\text{SEC/DIV}}{100} \times 4$[a]

[a]Performance Requirement not checked in Service Manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
PROBE ADJUST	
Output Voltage on PRB ADJ Jack	0.5 V ±5%.
Probe Adjust Signal Repetition Rate	1 kHz ±20%.[a]
Z-AXIS	
Sensitivity (NON STORE Only)	5 V causes noticeable modulation. Positive-going input decreases intensity. Usable frequency range is dc to 20 MHz.
Maximum Input Voltage ⚠	30 V (dc + peak ac) or 30 V p-p ac at 1 kHz or less.[a]
Input Resistance	>10 kΩ.[a]
POWER SUPPLY	
Line Voltage Range	90 Vac to 250 Vac.[a]
Line Frequency	48 Hz to 440 Hz.[a]
Maximum Power Consumption	85 watts (150 VA).[a]
Line Fuse	2 A, 250 V, slow blow.[a]
Primary Circuit Dielectric Requirement	Routine test to 1500 Vrms, 60 Hz, for 10 seconds without breakdown.[a]
CRT DISPLAY	
Display Area	8 cm × 10 cm.[a]
Standard Phosphor	P31.[a]
Nominal Accelerating Voltage	14 kV.[a]
X-Y PLOTTER OUTPUT	
Maximum Safe Applied Voltage, Any Connector Pin ⚠	25 V (dc + peak ac) or 25 V p-p ac at 1 kHz or less.[a]
X and Y Plotter Outputs	
Pen Lift/Down	Fused relay contacts, 100 mA maximum.[a]
Output Voltage Levels	500 mV per division ±10%. Center screen is 0 V ±0.2 division.
Series Resistance	2 kΩ ±10%.[a]
4.2 V Output	4.2 V ±10% through 2 kΩ.[a]

[a]Performance Requirement not checked in Service Manual.

Table 1-2

Environmental Characteristics

Characteristics	Performance Requirements
Environmental Requirements	Instrument meets the requirements of Tektronix Standard 062-2853-00, Class 5, except EMI. The instrument meets the following MIL-T-28800C requirements for Type III, Class 5 equipment, except where noted otherwise.
Temperature	
Operating	0°C to +50°C (+32°F to +122°F).
Nonoperating	−55°C to +75°C (−67°F to +167°F). Tested to MIL-T-28800C, para 4.5.5.1.3 and 4.5.5.1.4, except that in para 4.5.5.1.3 steps 4 and 5 are performed before step 2 (−55°C nonoperating test). Equipment shall remain off upon return to room ambient temperature during step 6. Excessive condensation shall be removed before operating during step 7.
Altitude	
Operating	To 4,500 meters (15,000 feet). Maximum operating temperature decreases 1°C per 1,000 feet above 5,000 feet.
Nonoperating	To 15,000 meters (50,000 feet).
Humidity	
Operating and Nonoperating	5 cycles (120 hours) referenced to MIL-T-28800C para 4.5.5.1.2.2 for Type III, Class 5 instruments. Operating and nonoperating at 95%, −5% to +0%, relative humidity. Operating, +30°C to +50°C; nonoperating, +30°C to +60°C.
EMI (electromagnetic interference)	Meets radiated and conducted emission requirements per VDE 0871, Class B. To meet EMI regulations and specifications, use the specified shielded cable and metal connector housing with the housing grounded to the cable shield on the AUXILIARY CONNECTOR.
Vibration	
Operating	15 minutes along each of three major axes at a total displacement of 0.015 inch p-p (2.4 g at 55 Hz) with frequency varied from 10 Hz to 55 Hz to 10 Hz in one-minute sweeps. Hold for 10 minutes at 55 Hz in each of the three major axes. All major resonances are above 55 Hz.
Shock	
Operating and Nonoperating	30 g, half-sine, 11 ms duration, three shocks per axis each direction, for a total of 18 shocks.

Table 1-3

Physical Characteristics

Characteristics	Description
Weight	See Figure 1-2 for dimensional drawing.
With Power Cord, Cover, Probes, and Pouch	9.4 kg (20.7 lb).
With Power Cord Only	8.2 kg (18 lb).
Domestic Shipping Weight	12.2 kg (26.9 lb).
Height	137 mm (5.4 in).
Width	
With Handle	362 mm (14.3 in).
Without Handle	327 mm (12.9 in).
Depth	
With Front Cover	445 mm (17.5 in).
Without Front Cover	435 mm (17.1 in).
With Handle Extended	510 mm (20.1 in).

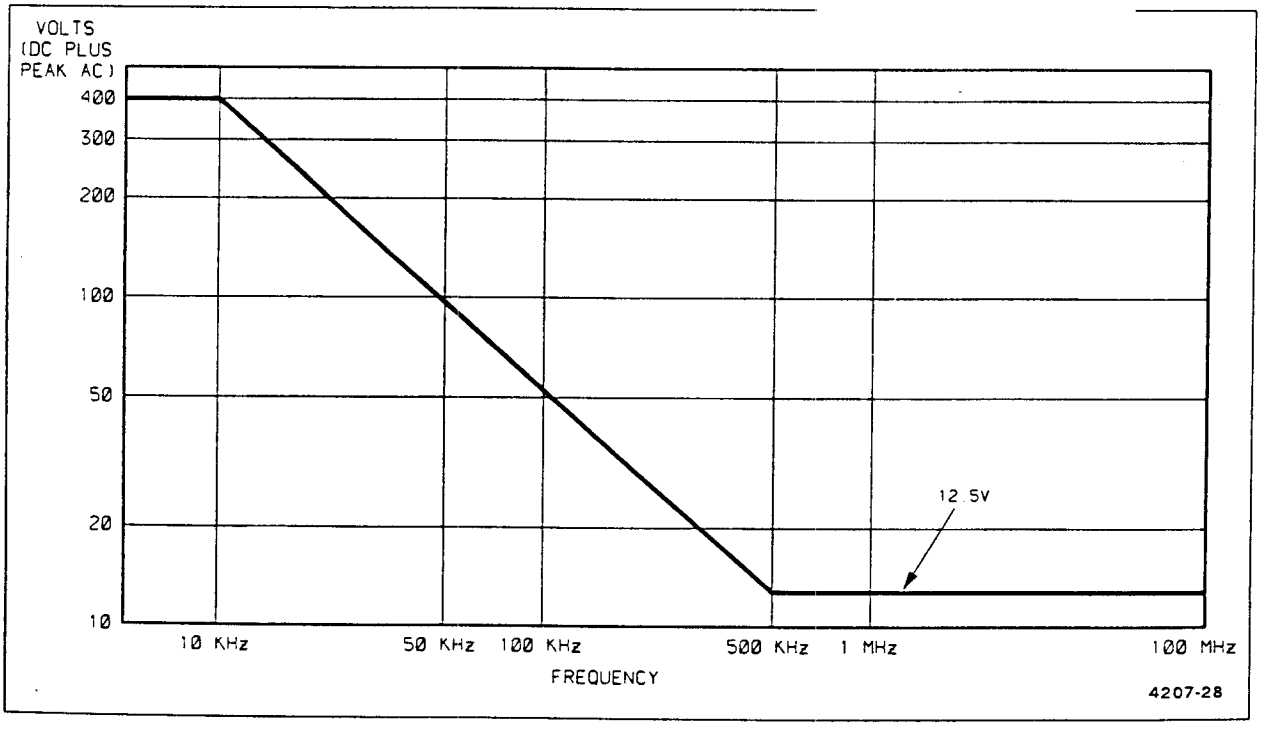


Figure 1-1. Maximum input voltage vs frequency derating curve for CH 1 OR X, CH 2 OR Y, and EXT INPUT connectors.

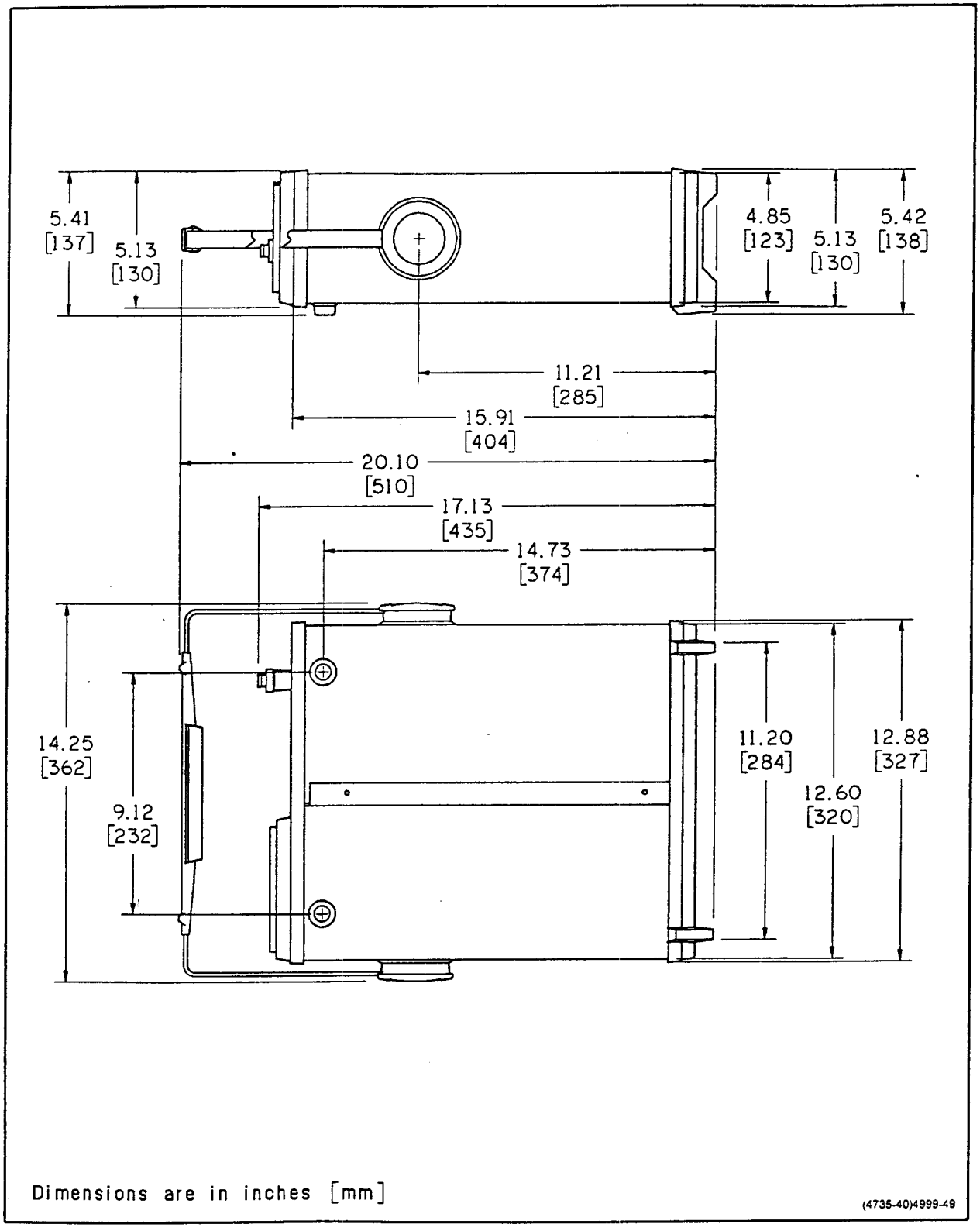


Figure 1-2. Physical dimensions of the 2230 Oscilloscope.

OPERATING INFORMATION

PREPARATION FOR USE

SAFETY

This part of the manual tells how to prepare for and to proceed with the initial start-up of the instrument.

Refer to the Safety Summary at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of the instrument. Before connecting the oscilloscope to a power source, read entirely both this section and the Safety Summary.

LINE VOLTAGE

This instrument is capable of continuous operation with input voltages that range from 90 V to 250 V with source voltage frequencies from 48 Hz to 440 Hz.

POWER CORD

A detachable three-wire power cord with a three-contact plug is provided with each instrument for connecting to both the power source and protective ground. The power cord may be secured to the rear panel by a cord-set-securing clamp (see Figure 2-1). The protective-ground contact in the plug connects (through the protective-ground conductor) to the accessible metal parts of the instrument. For electrical-shock protection, insert this plug only into a power-source outlet that has a properly grounded protective-ground contact.

Instruments are shipped with the power cord specified by the customer. Available power-cord information is presented in Figure 2-2, and part numbers are listed in "Options and Accessories" (Section 7). Contact your Tektronix representative or local Tektronix Field Office for additional power-cord information.

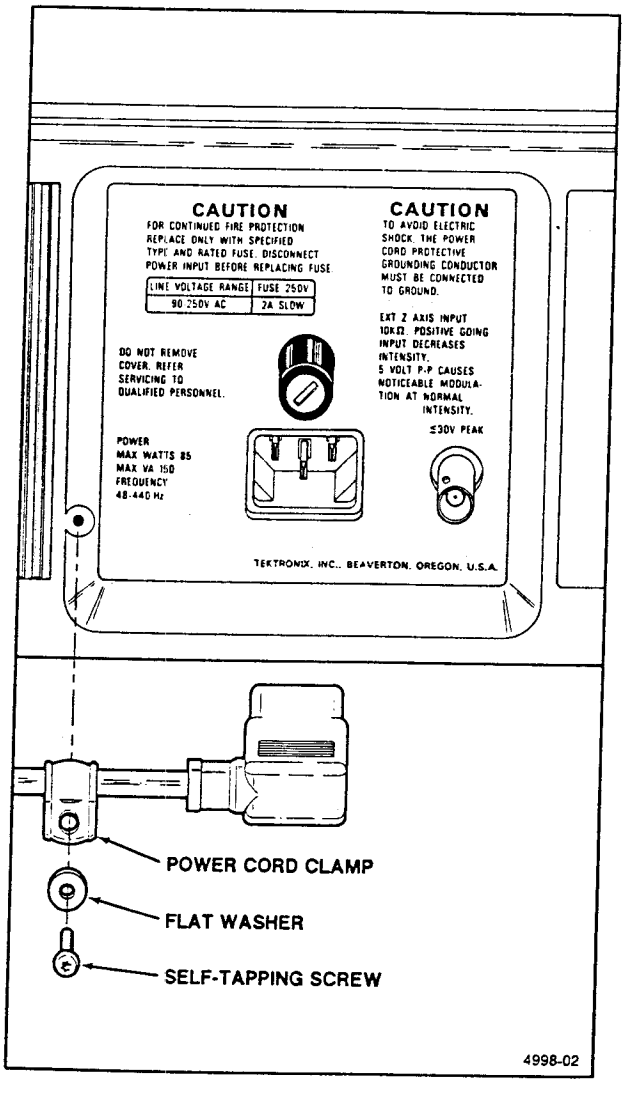
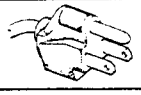
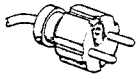
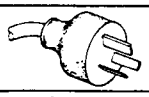
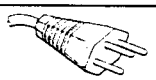


Figure 2-1. Securing the detachable power-cord to the instrument.

Plug Configuration	Usage	Line Voltage	Reference Standards
	North American 120V/ 15A	120V	ANSI C73.11 NEMA 5-15-P IEC 83
	Universal Euro 240V/ 10-16A	240V	CEE (7),II,IV,VII IEC 83
	UK 240V/ 13A	240V	BS 1363 IEC 83
	Australian 240V/ 10A	240V	AS C112
	North American 240V/ 15A	240V	ANSI C73.20 NEMA 6-15-P IEC 83
	Switzerland 220V/ 6A	220V	SEV

Abbreviations:
ANSI — American National Standards Institute
AS — Standards Association of Australia
BS — British Standards Institution
CEE — International Commission on Rules for the Approval of Electrical Equipment
IEC — International Electrotechnical Commission
NEMA — National Electrical Manufacturer's Association
SEV — Schweizevischer Elektrotechischer Verein

(2931-21)4204-53

Figure 2-2. Optional power-cord data.

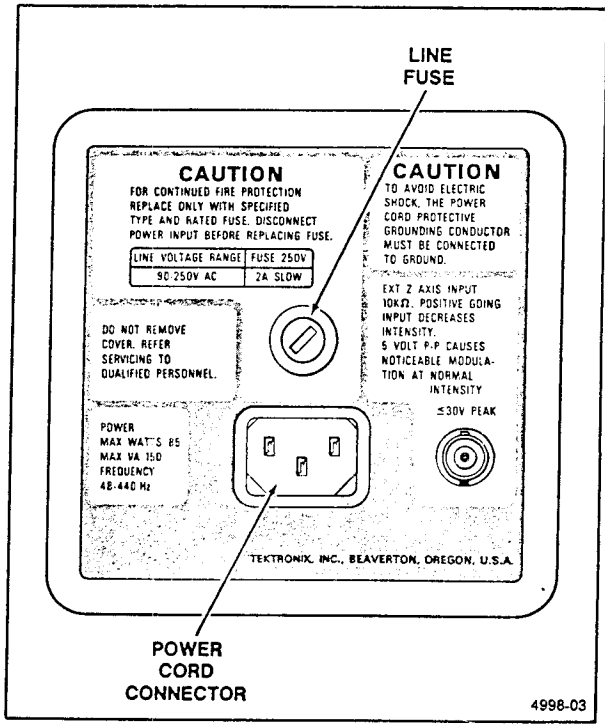


Figure 2-3. Fuse holder and detachable power-cord connector.

LINE FUSE

The instrument fuse holder is located on the rear panel (see Figure 2-3) and contains the line-protection fuse. The following procedure may be used either to verify that the proper fuse is installed or to install a replacement fuse.

1. Unplug the power cord from the power-input source (if plugged in).

2. Press in the fuse-holder cap and release it with a slight counterclockwise rotation.

3. Pull the cap (with the attached fuse inside) out of the fuse holder.

4. Verify that the proper fuse is installed (see the rear-panel fuse nomenclature).

5. Reinstall the proper fuse in the fuse cap and replace the cap and fuse in the fuse holder by pressing in and giving a slight clockwise rotation of the cap.

INSTRUMENT COOLING

To prevent instrument damage from overheated components, adequate internal airflow must be maintained at all times. Before turning on the power, first verify that both the fan-exhaust holes on the rear panel and the air-intake holes on the side panel are free from any obstructions to airflow. After turning on the instrument, verify that the fan is exhausting air.

START-UP

The instrument automatically performs power-up tests of the digital portion of the circuitry each time the instrument is turned on. The purpose of these tests is to provide the user with the highest possible confidence level that the instrument is fully functional. If no faults are encountered during the power-up testing, the instrument will enter the

normal operating mode. If the instrument fails one of the power-up tests, the instrument attempts to indicate the cause of the failure.

If a failure of any power-up test occurs, the instrument may still be useable for some applications, depending on the nature of the failure. If the instrument functions for your immediate measurement requirement, it may be used, but refer it to a qualified service technician for repair of the problem at the earliest convenience. Consult your service department, your local Tektronix Service Center, or your nearest Tektronix representative if additional assistance is required.

REPACKAGING

If this instrument is shipped by commercial transportation, use the original packaging material. Unpack the instrument carefully from the shipping container to save the carton and packaging material for this purpose.

If the original packaging is unfit for use or is not available, repackage the instrument as follows:

1. Obtain a corrugated cardboard shipping carton having inside dimensions at least six inches greater than the instrument dimensions and having a carton test strength of at least 275 pounds.

2. If the instrument is being shipped to a Tektronix Service Center for repair or calibration, attach a tag to the instrument showing the following: owner of the instrument (with address), the name of a person at your firm who may be contacted if additional information is needed, complete instrument type and serial number, and a description of the service required.

3. Wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of packing materials into the instrument.

4. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing for three inches of padding on each side (including top and bottom).

5. Seal the carton with shipping tape or with an industrial stapler.

6. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

CONTROLS, CONNECTORS, AND INDICATORS

The following descriptions are intended to familiarize the operator with the location and function of the instrument's controls, connectors, and indicators.

POWER AND DISPLAY

Refer to Figure 2-4 for location of items 1 through 9.

(1) **Internal Graticule**—Eliminates parallax viewing error between the trace and the graticule lines. Rise-time amplitude and measurement points are indicated at the left edge of the graticule.

(2) **POWER Switch**—Turns instrument power on or off. Press in for ON; press again for OFF.

(3) **Power On Indicator**—Lights up while instrument is operating.

(4) **FOCUS Control**—Adjusts for optimum display definition. Once set, proper focusing is maintained over a wide range of display intensity.

(5) **STORAGE/READOUT INTENSITY Control**—Adjusts the brightness of the STORE mode displayed waveforms and the readout intensity in both STORE and NON STORE mode. The fully counterclockwise position of the control toggles the STORE/NON STORE readout on and off.

(6) **BEAM FIND Switch**—Compresses the vertical and horizontal deflection to within the graticule area and intensifies the display to aid in locating traces that are overscanned or deflected outside of the crt viewing area.

(7) **TRACE ROTATION Control**—Permits alignment of the trace with the horizontal graticule line. This control is a screwdriver adjustment that, once set, should require little attention during normal operation.

(8) **A INTENSITY Control**—Adjusts the brightness of all NON STORE displayed waveforms. The control has no effect on the STORE mode displays or the crt readouts.

(9) **B INTENSITY Control**—Adjusts the brightness of the NON STORE B Delayed Sweep and the Intensified zone on the A Sweep. The control has no effect on STORE mode displays or crt readouts.

VERTICAL

Refer to Figure 2-5 for location of items 10 through 19.

(10) **VOLTS/DIV Switches**—Select the vertical channel deflection factors from 2 mV to 5 V per division in a 1-2-5 sequence. The VOLTS/DIV switch setting for both channels is displayed in the crt readout. The VOLTS/DIV control settings for displayed waveforms containing cursor symbols are shown in the crt readout.

In STORE mode, SAVE waveforms and waveforms waiting to be updated between trigger events may be vertically expanded or compressed by up to a factor of 10 times (or as many VOLTS/DIV switch positions remaining—whichever is less) by switching the corresponding VOLTS/DIV control (waveforms acquired at 2 mV/div cannot be expanded and waveforms acquired at 5 V/div cannot be compressed). The VOLTS/DIV readout reflects the vertical scale factor of the displayed waveform. If the VOLTS/DIV switch is switched beyond the available expansion or compression range, the readout is tilted to indicate that the VOLTS/DIV switch setting and the VOLTS/DIV readout no longer agree.

1X PROBE—Front-panel marking that indicates the deflection factor set by the VOLTS/DIV switch when a X1 probe or a coaxial cable is attached to the channel input connector.

10X PROBE—Front-panel marking that indicates the deflection factor set by the VOLTS/DIV switch when a properly coded 10X probe is attached to the channel input connector.

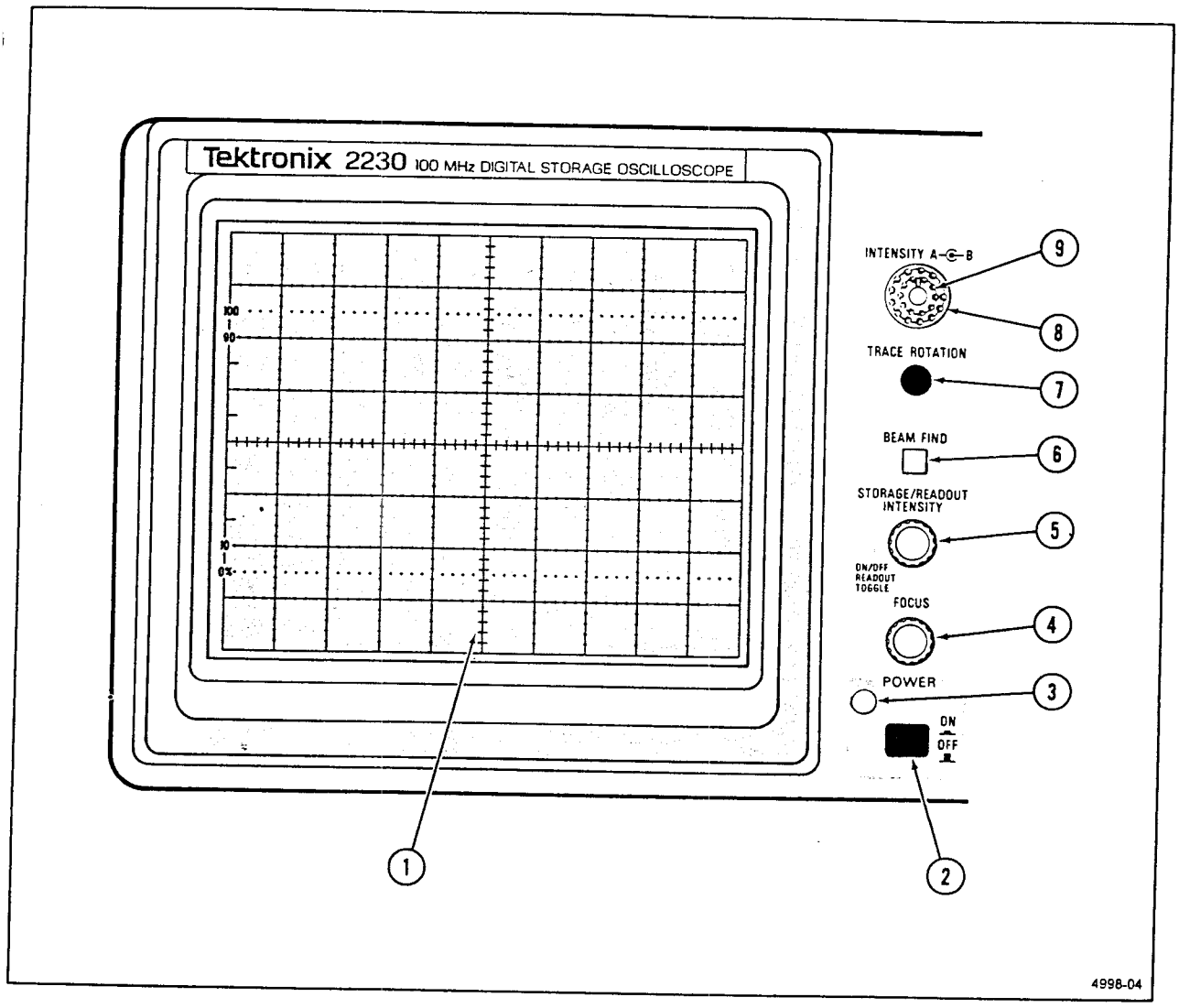


Figure 2-4. Power and display controls and power-on indicator.

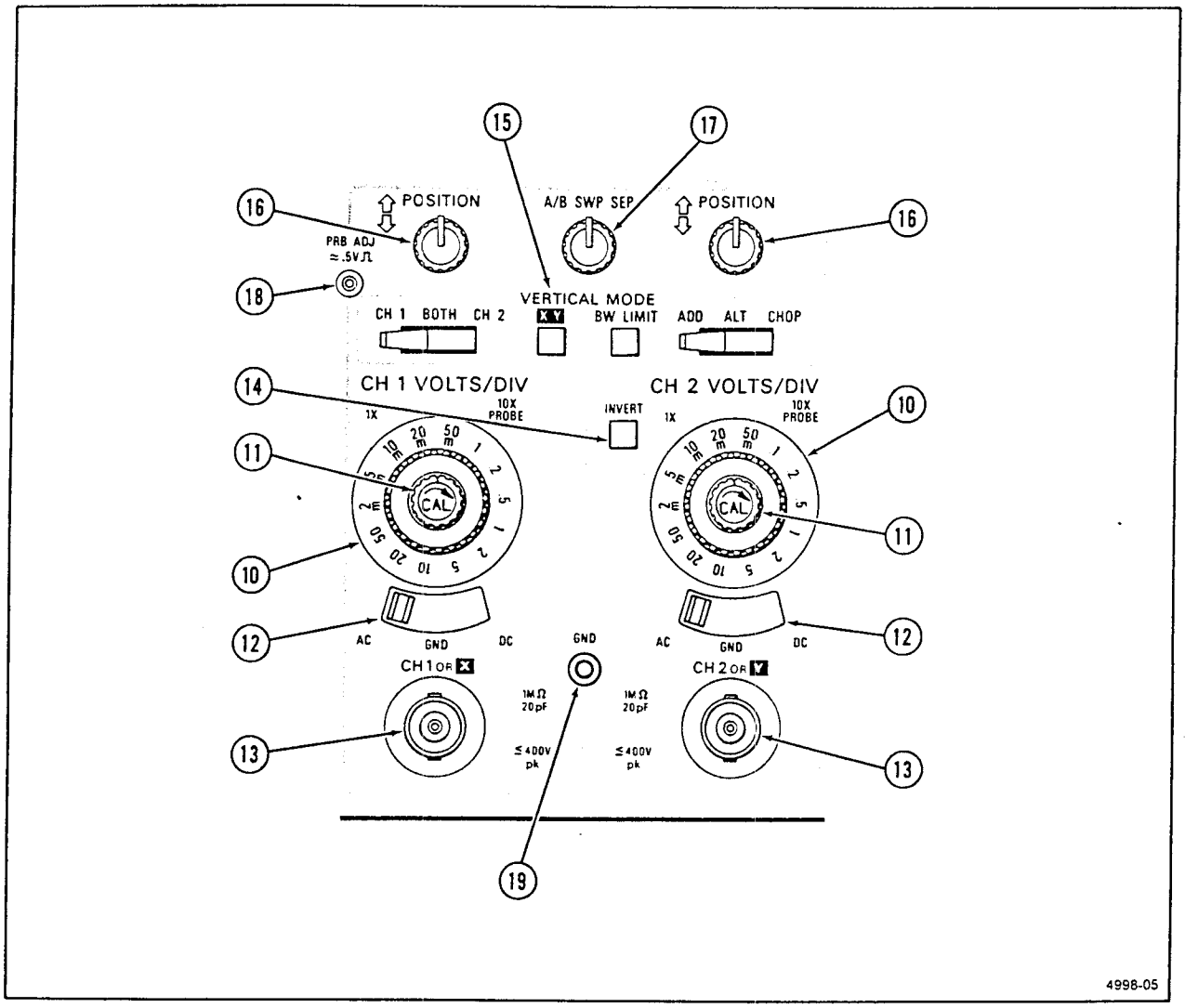


Figure 2-5. Vertical controls and connectors.

If properly coded probes (1X, 10X, or 100X, see Table 2-1) are connected to a channel input connector, the crt VOLTS/DIV readout will reflect the correct deflection factor of the display.

Table 2-1
Probe Coding

Probe	Coding Resistance
1X	Infinite
10X	11 kΩ ±10%
100X	5.6 kΩ −10% to 6.2 kΩ +10%
IDENTIFY	0 Ω or none of the above

(11) **Variable VOLTS/DIV Controls**—Provide continuously variable uncalibrated deflection factors between the calibrated positions of the VOLTS/DIV controls. The VOLTS/DIV sensitivity is reduced by up to at least 2.5 times the sensitivity at the fully counterclockwise position of the variable knob. A detent at the fully clockwise position indicates the calibrated VOLTS/DIV position of the variable knob. The uncalibrated condition is indicated by a greater-than symbol (>) in front of the affected VOLTS/DIV readout.

(12) **AC-GND-DC (Input Coupling) Switches**—Select the method of coupling the input signal to the CH 1 and CH 2 vertical amplifiers and the storage acquisition system.

AC—Capacitively couples the input signal to the vertical deflection and signal acquisition systems. The DC component of the input signal is blocked. The lower −3 dB bandpass is 10 Hz or less. Selection of AC input coupling is indicated in the readout by a tilde symbol (~) over the V on the associated channel's VOLTS/DIV readout.

GND—Grounds the input of the vertical amplifier; provides a zero (ground) reference voltage display (does not ground the input signal). In STORE mode, the ground reference is acquired and displayed in the first sample location of the acquisition waveform display. When GND input coupling is selected, a ground symbol is displayed in the associated VOLTS/DIV readout.

DC—All frequency components of the input signal are coupled to the vertical deflection and signal acquisition systems. When DC input coupling is selected, no additional indicators are displayed with the associated VOLTS/DIV readout.

(13) **CH 1 OR X and CH 2 OR Y Input Connectors**—Provide for application of signals to the inputs of the vertical deflection system and the storage acquisition system.

Coding-ring contacts on each of the input connectors are used to automatically switch the scale factor displayed by the crt readout when a properly coded probe is attached to the input connector. Displayed STORE mode waveforms are reformatted to maintain the correct deflection as indicated by the VOLTS/DIV readout on the affected channel(s). In X-Y mode, the signal connected to the CH 1 OR X input controls the horizontal deflection, and the signal connected to the CH 2 OR Y input controls the vertical deflection.

(14) **CH 2 INVERT Switch**—Inverts the Channel 2 display and STORE mode Channel 2 acquisition signal when pressed in. An invert symbol (↓) is displayed with the CH 2 VOLTS/DIV readout when CH 2 is inverted. With CH 2 inverted, the oscilloscope may be operated as a differential amplifier when the Vertical MODE of BOTH-ADD is selected.

(15) **VERTICAL MODE Switches**—Select the mode of operation for the vertical amplifier. There are two three-position switches and one two-position switch that determine display and acquisition modes and one two-position push-button switch that controls the nonstore bandwidth.

CH 1—Selects only the Channel 1 input signal for acquisition or display.

BOTH—Selects a combination of Channel 1 and Channel 2 input signals for acquisition or display. The CH 1-BOTH-CH 2 switch must be in the BOTH position for ADD, ALT, and CHOP operation.

CH 2—Selects only the Channel 2 input signal for acquisition or display.

ADD—Displays (NON STORE) or acquires and then displays (STORE) the sum of the Channel 1 and Channel 2 input signals when BOTH is also selected. The difference of the Channel 1 and Channel 2 input signals is displayed (NON STORE) or acquired and then displayed (STORE) when the Channel 2 signal is inverted.

ALT—Alternately displays the nonstore Channel 1 and Channel 2 input signals. The nonstore alternation occurs during retrace at the end of each sweep. ALT Vertical MODE is most useful for

acquiring and viewing both channel input signals at sweep rates of 0.5 ms per division and faster. Channel 1 and Channel 2 STORE mode signals are acquired on alternate acquisition cycles at one-half the sampling rate of a single-channel acquisition.

CHOP—Switches the nonstore display between the Channel 1 and Channel 2 vertical input signals during the sweep. The chopped switching rate for NON STORE mode (CHOP frequency) is approximately 500 kHz. Chopped STORE mode signals are acquired on alternate time-base clock cycles with each channel being acquired at one-half the sampling rate of a single-channel acquisition. In STORE mode at sweep speeds of 5 μs per division or faster, CHOP becomes ALT mode.

BW LIMIT Switch—When pressed in while in NON STORE mode, the bandwidth of the vertical amplifier system and the A Trigger system is limited to approximately 20 MHz. This reduces interference from unwanted high-frequency signals when viewing low-frequency signals. In STORE mode, pressing in the BW LIMIT switch reduces only the trigger bandwidth. Press the switch a second time to release the switch and regain full bandwidth.

X-Y Switch—Automatically selects X-Y mode when pressed in. The CH 1 input signal provides horizontal deflection for X-Y displays, and the CH 2 input signal provides vertical deflection. In STORE mode, CH 1 and CH 2 signals are acquired in a chopped manner with no more than 100 ns between corresponding sample points on opposite channels, with the CH 1 signal being sampled before the CH 2 signal. The sampling mode and sampling rate are controlled by the A or the B SEC/DIV switch (depending on the Horizontal Display mode). The X-Y waveform is acquired in SAMPLING mode and displayed with dots. Set the SEC/DIV controls to obtain at least 10 samples per cycle of the highest frequency component in both the X and the Y input signals. The sampling rate is determined by the formula 50/(SEC/DIV) Hz.

(16) **Vertical POSITION Controls**—Control the vertical display position of the CH 1 and CH 2 signals.

In STORE mode, the controls determine the vertical position of displayed waveforms during acquisition and in SAVE mode. Any portions of a signal being acquired that are outside the dynamic range of the A/D converter are blanked when positioned on screen. The Vertical POSITION controls can also reposition a vertically expanded SAVE waveform so that portions of the waveform outside the graticule area can be observed.

In NON STORE X-Y mode, the CH 2 POSITION control vertically positions the display, the horizontal POSITION control positions the display horizontally, and the CH 1 POSITION control is not active. In STORE mode, the CH 1 POSITION control is active, and both it and the Horizontal POSITION control affect the horizontal position of the displayed waveform.

(17) **A/B SWP SEP Control (NON STORE only)**—While in NON STORE mode, vertically positions the B Sweep trace with respect to the A Sweep trace when the HORIZONTAL MODE is BOTH.

(18) **PRB ADJ Connector**—Provides an approximately 0.5 V, negative-going, square-wave voltage (at approximately 1 kHz) for compensating voltage probes and checking the operation of the oscilloscope's vertical system. It is not intended to verify the accuracy of the vertical gain or the horizontal time-base circuitry.

(19) **GND Connector**—Provides an auxiliary ground connection directly to the instrument chassis via a banana-tip jack.

HORIZONTAL

Refer to Figure 2-6 for location of items 20 through 26.

(20) **SEC/DIV Switches**—Determine the SEC/DIV setting for both the NON STORE sweeps and the STORE mode waveform acquisitions. To obtain calibrated A and B NON STORE sweeps, the Variable SEC/DIV control must be in the CAL detent.

In STORE mode, the SEC/DIV switches determine the default acquisition and display modes, set the sampling rate, and establish the seconds-per-division scale factor of the displayed waveforms. The SEC/DIV parameters displayed on the crt readout are for the waveforms identified by CURSORS.

Table 2-2 lists the default Storage and Display modes with respect to the SEC/DIV switch setting and the selected Trigger mode. The default modes may be changed by selecting the Acq Mode Setup Table in the menu. Waveforms of SCAN, and ROLL displays are updated one data point at a time. All data points of a RECORD display are updated at the same time (total record replacement).

A SEC/DIV Switch—Selects the calibrated A Sweep rates from 0.5 s to 0.05 μs/div in a 1-2-5 sequence of 22 steps for the A Sweep generator and sets the delay time scale factor for delayed-sweep operation.

In STORE mode, the A SEC/DIV switch controls the default Storage, Acquisition, Process, and Display modes when making acquisitions using the A Time Base. It also selects the external clock signal, from the EXT CLK input, for the storage acquisition circuitry.

B SEC/DIV Switch—Selects the calibrated B Sweep rates from 50 ms/div to 0.05 μs/div in a 1-2-5 sequence of 19 steps.

In STORE mode, the B SEC/DIV switch controls the default Storage, Acquisition, Process, and Display modes when making acquisitions using the B Horizontal mode.

UNTRIGGERED mode performs acquisitions without reference to the trigger circuit, and there is no trigger marker on the screen. Triggers are ignored in STORE mode at SEC/DIV settings of 5 s per division to 0.1 s per division under the following conditions:

ROLL is selected. Selecting ROLL forces the screen to continuously update as on a chart recorder. Triggers would stop the display. ROLL is operational at sweep speeds slow

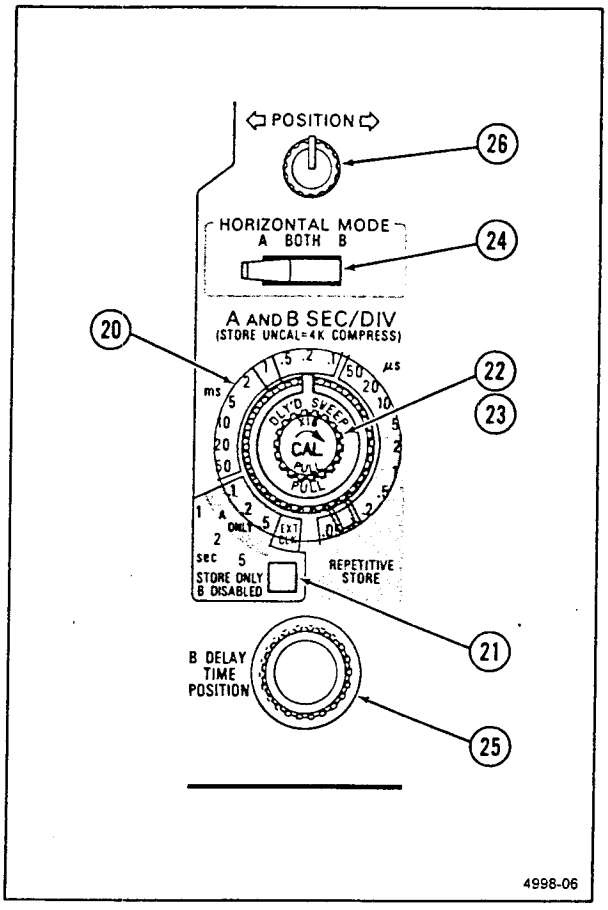


Figure 2-6. Horizontal controls.

Table 2-2

Default Digital Storage Modes

	UN-TRIG[a] 5 s to 0.1 s or EXT CLK	TRIG[b] 5 s to 0.1 s or EXT CLK	SLOW RECORD 50 ms to 20 μs	FAST RECORD 10 μs to 5 μs	REPETITIVE 2 μs to 0.05 μs
SAMPLE[c]	OFF	OFF	OFF	ON	OFF
AVERAGE[c]	—	OFF	OFF	OFF	ON
ACCPEAK[c]	—	OFF	OFF	OFF	OFF
PEAKDET[c]	ON	ON	ON	—	—
SMOOTH[d]	ON	ON	ON	OFF	OFF
VECTORS	ON	ON	ON	ON	DOTS only

[a]See the "UNTRIGGERED" discussion.

[b]See the "TRIGGERED" discussion.

[c]These Storage modes are mutually exclusive.

[d]Works with ACCPEAK and PEAKDET only.

enough that the acquisition can manually be stopped when events of interest are observed.

P-P AUTO is selected. P-P AUTO provides a baseline in the absence of triggers from the input signal. The circuit considers the absence of triggers to be about half of a second without a trigger. Below 50 ms per division, the triggers are prevented for longer than that by the sweep time itself, therefore triggers are ignored.

TRIGGERED mode performs triggered acquisitions in STORE mode at SEC/DIV settings of 5 s per division to 0.1 s per division when triggers can be meaningful. Triggers are meaningful in SCAN mode if the A TRIGGER mode is NORM or SGL SWP. Triggers are not meaningful in ROLL mode or in the A TRIGGER Mode of P-P AUTO.

REPETITIVE Store mode (2 μs/div to 0.05 μs/div) requires a repetitive trigger signal. Sampling occurs at the maximum A/D conversion rate. If a control affecting an acquisition parameter or function is changed, the acquisition is reset, and the waveform being acquired is cleared on the next sample acquired. On each valid trigger, 10 or more equally spaced samples are acquired and displayed on the waveform record, depending on the SEC/DIV setting (see Table 2-3). The random time delay from the trigger to the following sample clock transition is measured by the Clock Delay Timer circuit and used to place the acquired waveform samples in the correct display memory location. Any display location is equally likely to be filled. Table 2-3 gives the statistically expected number of trigger events required to completely fill the display, assuming a uniform distribution of trigger events relative to the sample interval.

FAST RECORD Storage mode (5 μs/div to 10 μs/div) updates a full record of the acquired waveform.

SLOW RECORD Storage mode (20 μs/div to 50 ms/div) updates a full record of the acquired waveform.

SCAN Storage mode (for NORM TRIGGER mode and 0.1 s/div to 5 s/div or EXT CLOCK) updates pretrigger data when a trigger is received. The waveform display then scans to the right from the trigger point to finish the post-trigger acquisition and then freezes.

SCAN Storage mode (for P-P AUTO TRIGGER mode with auto triggers disabled and 0.1 s/div to 5 s/div or EXT CLOCK) continuously updates the display serially as each data point is acquired. It writes over previous data from left to right.

ROLL Storage mode (P-P AUTO TRIGGER mode and 0.1 s/div to 5 s/div or EXT CLOCK) continuously acquires and displays signals. Triggers are disabled. The waveform display scrolls from right to left across the crt with the latest samples appearing at the right edge of the crt.

SCAN-ROLL-SCAN Storage mode (SGL SWP TRIGGER mode and 0.1 s/div to 5 s/div or EXT CLOCK) serially updates the display. The waveform display SCANS left to right until the pretrigger record is filled, and then ROLLS right to left until a trigger is received. It then SCANS left to right again to fill the post-trigger acquisition record and then freezes (see SGL SWP description for further details).

PEAKDET Acquisition mode digitizes and stores, in acquisition memory as a data pair, the minimum and maximum levels of the input signal within the time represented by 1/50 of a division UN-MAG (1/25 division in CHOP or ALT).

SAMPLE samples the signal at a rate that produces 100 samples per graticule division. In the RECORD Sampling modes, the displayed sample points are displayed by vectors or dots. For REPETITIVE Store mode, the sample points are displayed as dots.

Table 2-3

Repetitive Store Sampling Data Acquisition

SEC/DIV Switch Setting	Samples Per Acquisition		Expected Acquisitions Per Waveform[a]	
	1K Mode	4K Mode	1 Channel	2 Channels
0.05 μs	10	40	519	450
0.1 μs	20	80	225	191
0.2 μs	40	160	96	83
0.5 μs	100	400	30	23
1 μs	200	800	12	11
2 μs	200	800	12	11

[a]Expected acquisitions per waveform for a 50% probability of fill.

AVERAGE Acquisition mode can be used for multiple record averaging. A normalized algorithm is used for continuous display of the signal at full amplitude during the averaging process. The amplitude resolution increases with the number of weighted acquisitions included in the display. The default mode for REPETITIVE Store mode is AVERAGE. The averaging weight (the number of weighted waveform acquisitions included in each average display) is MENU selectable. The default average weight is 1/4. The number of sweeps (SWP LIMIT) allowed to occur before averaging stops is also MENU selectable. The averaging process is reset by changing any control that causes an acquisition reset.

ACCPEAK Acquisition mode causes accumulation of peaks over multiple acquisitions. The largest maximum and smallest minimum samples are retained for each trigger-referenced acquisition record. For 20 μs per division to 5 s per division, hardware peak detection is used, updating maximum and minimum samples within each time base clock period. The ACCPEAK display is reset by changing any control that causes an acquisition reset. ACCPEAK mode is valid for triggered acquisitions only and is not operational in untriggered modes (see Table 2-2).

SMOOTH Processing mode reorders acquired data for correct slope and interpolates the data for drawing a smooth waveform. Smoothing looks at the change in data point values between adjacent sample intervals. If the change in value does not exceed certain limits, the values are interpreted as a continuous slope for drawing vectors or dots. If the value change exceeds the interpreted "no-change" limit, the data point value is not modified, and the vectors drawn in the display will show a discontinuity in the waveform. This method of display of the waveform data provides a smoothed display of the waveform, yet retains the glitch-catching capabilities of PEAKDET or ACCPEAK modes.

(21) **STORE Mode A SEC/DIV Multiplier**—Functions only in the STORE mode at SEC/DIV switch settings of 0.1, 0.2, and 0.5 s/div. When pressed in, the A Sweep time base of these three settings is increased by a factor of 10 to 1 s/div, 2 s/div, and 5 s/div. Releasing the button returns the STORE mode time base to X1. The X10 MAG control is still functional on waveforms acquired at the slow STORE mode SEC/DIV settings.

(22) **Variable SEC/DIV and 4K COMPRESS Control**—Controls the NON STORE sweep time per division and compresses STORE mode waveform records.

Variable SEC/DIV—Continuously varies the uncalibrated NON STORE sweep time per division to at least four times the calibrated time per division set by the SEC/DIV switch (increases the slowest NON STORE A Sweep time per division to at least 2 s). The Variable SEC/DIV control does not affect the storage time base for acquiring or displaying signals.

4K COMPRESS—If the Variable SEC/DIV control is rotated out of the CAL detent position during waveform acquisitions or SAVE mode, a 4K record is compressed by a factor of four (4K COMPRESS) to display the acquired data in one display window. For 4K COMPRESS the SEC/DIV is further multiplied by 4. In PEAKDET or ACCPEAK acquisition modes, peaks are acquired but not displayed when 4K COMPRESS is selected.

(23) **X10 Magnifier Switch**—Magnifies the NON STORE displays or expands the STORE acquisition and SAVE waveform displays by 10 times. STORE mode displays are expanded when the Variable SEC/DIV knob is pulled to the out position (X10 PULL). The SEC/DIV scale factor readouts are adjusted to correspond to the correct SEC/DIV of the displayed waveform (either NON STORE or STORE). Magnification of the NON STORE displays occurs around the center vertical graticule division; STORE mode displays are expanded around the active CURSOR. The display window for STORE mode X10 expanded waveforms may be positioned using the CURSORS Control to view any one-window portion of the acquisition record.

(24) **HORIZONTAL MODE Switch**—Determines the operating mode of the horizontal deflection system in both NON STORE and STORE. For STORE mode, the switch selects the acquisition time base and storage mode (either A SEC/DIV or B SEC/DIV).

A—Only the A Sweep is displayed. NON STORE time base and STORE acquisitions are controlled by the A SEC/DIV switch. The A SEC/DIV switch setting is displayed on the crt readout.

BOTH—Alternates the NON STORE display between the A Intensified and B Delayed Sweeps.

The STORE mode display is the A Intensified trace only. The intensified zone on the A trace indicates the approximate delay position and length of the B Delayed Sweep. The displayed position of the intensified zone is updated after each trigger. The A SEC/DIV, B SEC/DIV, and B DELAY TIME POSITION settings are displayed on the crt readout. In BOTH, STORE mode acquisitions are controlled by the A SEC/DIV switch.

B—Displays either the NON STORE or the STORE B Sweep trace. The A SEC/DIV, B SEC/DIV, and B DELAY TIME POSITION settings are displayed on the crt readout, just as in BOTH. The STORE mode waveform acquisitions are controlled by the B SEC/DIV switch.

(25) **B DELAY TIME POSITION Control**—Adjusts the delay between the start time of the A Sweep and the time that the B Sweep either starts (RUNS AFTER DLY) or can be triggered (Triggerable After Dly). (The A Sweep does not have to be displayed.) The delay time is variable from 0.5 to 10 times the A SEC/DIV, plus 300 ns.

In Triggerable After Delay, the delay time readout indicates the time that must elapse after the A trigger before the delayed sweep or delayed acquisition can be triggered; not the actual position of the trigger point. However, the readout of the delay time on the crt follows the setting of the B DELAY TIME POSITION control in either B Trigger mode.

The setting of the 1K/4K switch affects the delay time position setting for STORE mode displays by a factor of approximately four times. When switching between 1K and 4K record lengths, the delay time position setting must be readjusted to obtain the same delay time.

(26) **Horizontal POSITION Control**—Positions all the NON STORE waveforms horizontally over a one-sweep-length range (either X1 or X10 Magnified). Using the Horizontal POSITION control, STORE mode waveforms may be positioned over a range of only one display window. When a STORE mode acquisition display is longer than one screen (as in 4K records and/or X10 MAG), the CURSORS POSITION control is used to position the display window to any position of the acquisition record. The Horizontal POSITION control does not position the crt readout displays.

TRIGGER

Refer to Figure 2-7 for location of items 27 through 38.

NOTE

The Trigger controls affect the acquisition of the next waveform. They are inactive in SAVE Acquisition mode.

(27) **A TRIGGER Mode Switches**—Determine the NON STORE A Sweep triggering mode. STORE mode triggering depends on the position of the A SEC/DIV, the SCAN/ROLL switch, and the A Trigger mode. The trigger position is marked by a T on acquired waveforms.

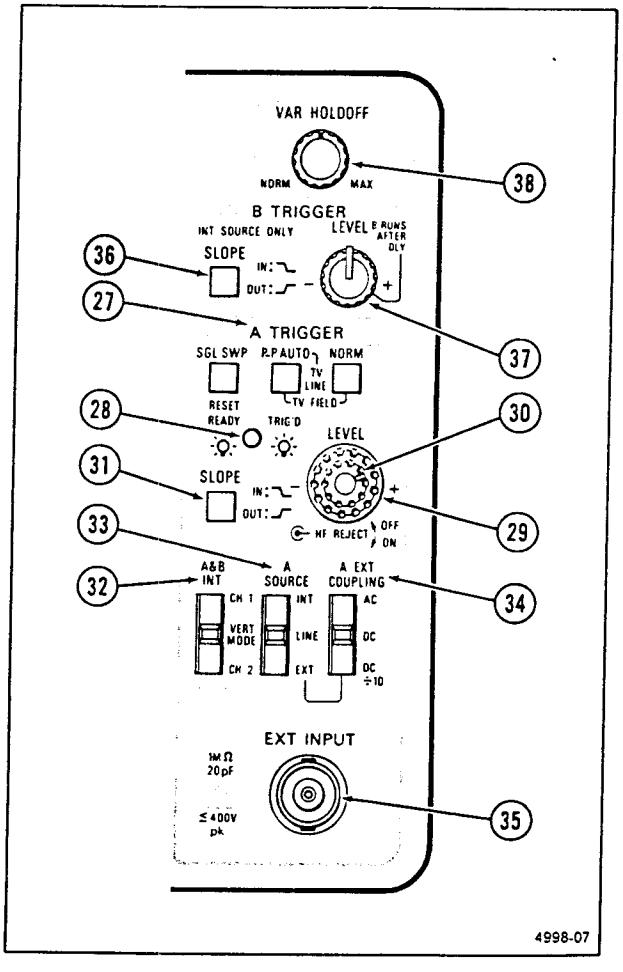


Figure 2-7. Trigger controls, connector, and indicator.

NORM—Permits triggering at all sweep rates (an autotrigger is not generated in the absence of an adequate trigger signal). NORM Trigger mode is especially useful for low-frequency and low-repetition-rate signals.

In STORE mode, the last acquired waveform is held on display between triggering events. The pretrigger portion of the acquisition memory is continually acquiring new pretrigger data until a trigger event occurs. How the waveform display is updated after the trigger occurs, depends on the SEC/DIV setting. From 5 s per division to 0.1 s per division, the pretrigger portion of the displayed waveform is updated by the pretrigger data in the acquisition memory, then the post-trigger data points are placed in the display as they are acquired. For faster sweep speeds, the post-trigger data points are acquired in the acquisition memory prior to completely updating the waveform display, using the newly acquired data.

P-P AUTO—TV LINE—In NON STORE mode, triggering occurs on trigger signals having adequate amplitude and a repetition rate of about 20 Hz or faster. In the absence of a proper trigger signal, an autotrigger is generated, and the sweep free runs.

In STORE mode, for SEC/DIV settings of 5 s per division to 0.1 s per division, the P-P AUTO trigger mode is disabled, and the acquisition free-runs. At faster SEC/DIV settings, triggered acquisitions occur under the same conditions as NON STORE mode P-P AUTO triggering, and the acquisition free-runs if proper triggering conditions are not met. The manner in which the display is filled and updated is the same as for NORM triggering.

For either NON STORE or STORE mode, the range of the A TRIGGER LEVEL control is automatically restricted to the peak-to-peak limits of the trigger signal for ease in obtaining triggered displays and acquisitions. P-P AUTO is the usual Trigger mode selection to obtain stable displays of TV Line information.

TV FIELD—Permits stable triggering on a television field (vertical sync) signal when the P-P AUTO and the NORM Trigger buttons are pressed in together. In the absence of an adequate trigger signal, the sweep (or acquisition) free-runs. The instrument otherwise behaves as in P-P AUTO.

SGL SWP—Arms the A Trigger circuit for a single sweep in NON STORE or a single acquisition in STORE. Triggering requirements are the same as in NORM Trigger mode. After the completion of a triggered NON STORE sweep or a STORE SGL SWP acquisition, pressing in the SGL SWP button rearms the trigger circuitry to accept the next triggering event or start the next storage acquisition.

In STORE mode, when the SGL SWP is armed, the acquisition cycle begins, but the READY LED does not come on until the pretrigger portion of the acquisition memory is filled. At the time the READY LED comes on, the acquisition system is ready to accept a trigger. When a trigger event occurs, the post-trigger waveform data is stored to complete the single-sweep acquisition. After the acquisition is completed, the READY LED goes out, and the single sweep can be rearmed.

The SEC/DIV switch setting and the STORE mode determine how the display is updated. For settings of 5 s per division to 0.1 s per division, a storage process known as SCAN-ROLL-SCAN is used. The last acquired waveform is erased when SGL SWP is armed, then the pretrigger acquisition scans from the left edge to the trigger position. At that point, the pretrigger portion of the display is rolled left from the trigger position until a triggering event occurs. Upon receiving an adequate trigger, the post-trigger portion of the display scans from the trigger point to the right until the remaining data points are filled, and then the display freezes.

For SEC/DIV settings of 0.05 s per division and faster, the display is updated as a full record. The previously displayed waveform remains on the crt until the post-trigger portion of the acquisition memory is filled after a triggering event. Then the waveform display is updated with the newly acquired data in its entirety.

(28) **READY—TRIG'D Indicator**—A dual-function LED indicator. In P-P AUTO and NORM Trigger modes, the LED is turned on when triggering occurs. In SGL SWP Trigger mode, the LED turns on when the A Trigger circuit is armed, awaiting a triggering event, and turns off again after the single sweep (or acquisition) completes.

In STORE mode, pressing the SGL SWP button to arm the trigger circuitry does not immediately turn on the READY LED. The pretrigger portion of the acquisition memory starts filling after the SGL SWP

button is pressed in; the READY LED is turned on when the filling is completed. The storage acquisition system is then ready to accept a triggering event. The READY LED is turned off after an acquisition is completed.

(29) **A TRIGGER LEVEL Control**—Selects the amplitude point on the A Trigger signal that produces triggering. The trigger point for STORE mode is identified by a T on the acquired waveform.

(30) **HF REJECT Switch**—Rejects (attenuates) the high-frequency components (above 40 kHz) of the trigger signal when the control is in the ON posiltion.

(31) **A TRIGGER SLOPE Switch**—Selects either the positive or negative slope of the trigger signal to start the NON STORE A Sweep or to reference the next STORE mode acquisition cycle.

(32) **A&B INT Switch**—Determines the source of the internal trigger signal for both the A and the B Trigger Generator circuits.

CH 1—Trigger signal is obtained from the CH 1 input.

VERT MODE—Trigger signal is obtained alternately from the CH 1 and CH 2 input signals if the VERTICAL MODE is ALT. In the CHOP VERTICAL MODE, the trigger signal is the sum of the CH 1 and CH 2 input signals.

CH 2—Trigger signal is obtained from the CH 2 input. The CH 2 INVERT switch also inverts the polarity of the internal CH 2 trigger signal so the displayed slope agrees with the Trigger SLOPE switch.

(33) **A SOURCE Switch**—Determines if the SOURCE of the A Trigger signal is internal, external, or from line.

INT—Routes the internal trigger signal selected by the A&B INT switch to the A Trigger circuit.

LINE—Routes a sample of the ac power source to the A Trigger circuit.

EXT—Routes the signal applied to the EXT INPUT connector to the A Trigger circuit.

(34) **A EXT COUPLING Switch**—Determines the method of coupling the signal applied to the EXT INPUT connector to the input of the A Trigger circuit.

AC—Input signal is capacitively coupled, and the dc component is blocked.

DC—All frequency components of the external signal are coupled to the A Trigger circuit.

DC÷10—Attenuates the external signal by a factor of 10 before application to the A Trigger circuit. As with DC COUPLING, all frequency components of the input signal are passed.

(35) **EXT INPUT Connector**—Provides for connection of external signals to the A Trigger circuit.

(36) **B TRIGGER (INT SOURCE ONLY) SLOPE Switch**—Selects either the positive or the negative slope of the B Trigger signal that starts the NON STORE sweep or completes the STORE acquisition.

(37) **B TRIGGER LEVEL Control**—Selects the amplitude point on the B Trigger signal where triggering occurs in Triggerable After Delay mode. The B Trigger point is displayed as a T on the STORE mode waveform display when in B Horizontal mode. The fully clockwise position of the B TRIGGER LEVEL Control selects the Runs After Delay mode of operation for the B Trigger circuitry. Out of the cw position, B Sweep is triggerable after the delay time.

(38) **VAR HOLDOFF Control**—Adjusts the NON STORE Variable Holdoff time over a 10 to 1 range. NON STORE Variable Holdoff starts at the end of the A Sweep. STORE mode Holdoff starts at the end of the acquisition cycle, and ends after the waveform data has been transferred from the acquisition to the display memory and the pretrigger portion of the acquisition memory has been filled. After STORE mode Holdoff ends, the next acquisition can be triggered after the next (or current, if one is in progress) NON STORE Variable Holdoff ends. STORE mode Holdoff may be many times the length of the A Sweep time so that several NON STORE Holdoffs may occur during STORE Holdoff time. This ensures that STORE mode triggering is controllable by the VAR HOLDOFF control and will be stable if the NON STORE display is stable.

STORAGE CONTROLS

See Figure 2-8 for the location of items 38 through 42.

(39) **STORE/NON STORE Switch**—Selects either the NON STORE or the STORE waveforms for display. The STORE acquisition system is turned off while NON STORE is selected, keeping the last-acquired STORE waveform in memory. Selects NON STORE when out and STORE when pressed in.

(40) **ACQUISITION Controls**—Determine the method of acquiring and displaying the acquired STORE waveform.

1K/4K Switch (Record Length)—Selects an acquisition record length of either one screen (1K) or four screens (4K). Pressing the button in selects 1K record length, and pressing it again to release it returns to 4K record length acquisitions. In either case, the displayed waveform has 100 data points per horizontal graticule division (50 if two channels are acquired).

When a waveform is acquired using the B time base, switching between record lengths also changes the delay time position setting by the same factor of four. The B DELAY TIME POSITION control must be repositioned to obtain the same delay.

When the 4K record length is selected, a one-screen (1K) window of the acquisition is displayed, and a bar graph is used to indicate the position of the displayed window within the record. Turn the CURSORS Position control to move the display window to any position within the record.

The 4K acquisition record can be compressed to a length of 1K by rotating the Variable SEC/DIV control out of the CAL detent position. The SEC/DIV readout is adjusted to reflect the correct time per division of the displayed waveform. The acquisition record may be magnified using the X10 Magnifier.

PRETRIG/POST TRIG Switch—Positions the trigger point for acquisitions either near the end (PRETRIG) or the beginning (POST TRIG) of the waveform. A T is displayed on the waveform to indicate the trigger point. Pressing the button in sets the trigger point to PRETRIG; out is the POST TRIG position.

ROLL/SCAN Switch—Selects either ROLL or SCAN acquisition and display mode. When pressed in (ROLL mode), at SEC/DIV switch settings from 0.1 s per division to 5 s per division the triggers are disabled for NORM and P-P AUTO Trigger modes, and the signals are continuously acquired and displayed. The waveform display scrolls from right to left across the crt with the latest samples appearing at the right edge of the crt. At SEC/DIV switch settings from 0.1 s per division to 5 s per division in SGL SWP Trigger mode, SCAN/ROLL/SCAN storage mode is selected.

At SEC/DIV switch settings of 0.05 s per division and faster, the ROLL/SCAN switch is not functional, and waveform samples require a triggering event to complete the acquisition before the display is updated.

When the ROLL/SCAN switch is in the out position (SCAN mode), the A TRIGGER Mode controls are functional. For NORM Trigger mode, the pretrigger waveform is updated by the trigger and the post trigger scans from the trigger position to the right. For SGL SWP, SCAN mode is overridden by SCAN/ROLL/SCAN. Triggers are disabled in P-P AUTO and TV FIELD Trigger modes.

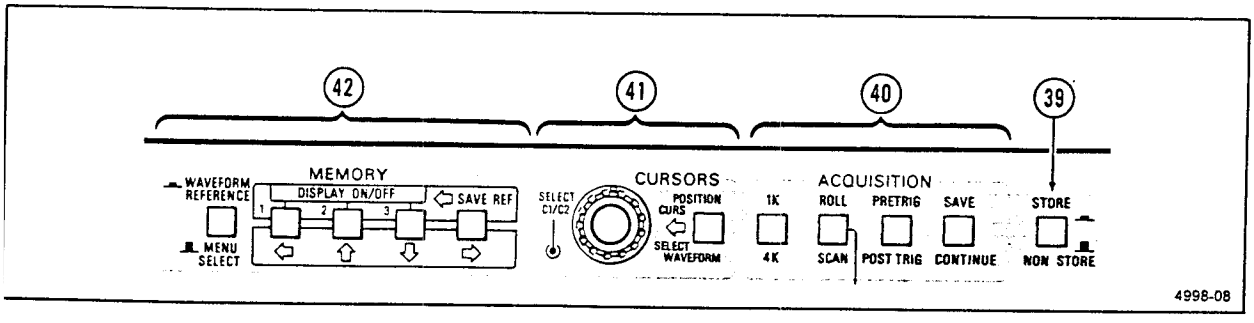


Figure 2-8. Storage controls.

SAVE/CONTINUE Switch—Stops the current acquisition and display update in progress when pressed in. Pressing the SAVE/CONTINUE switch a second time releases it and restarts (CONTINUE) the acquisition process. If the SEC/DIV switch setting is 0.1 s per division or slower, the SAVE state is entered immediately upon pressing the button. At SEC/DIV settings of 50 ms per division and faster, if an acquisition has been triggered, the acquisition is allowed to complete before the SAVE state is entered.

The pretrigger portion of an untriggered acquisition stops filling in SAVE mode. When leaving SAVE, a new acquisition is started, and a trigger is not accepted until the pretrigger portion again refills.

(41) **CURSORS Controls**—These controls apply to all displayed STORE mode waveforms. Delta Volts, Delta Time, One Over Delta Time, and Delay Time measurements of the STORE displays are made using the CURSORS controls. Positioning of the display window within a 4K acquisition record length is done using the CURSORS Position control. See the "Crt Readout" description for the cursor readout display.

POSITION CURS/SELECT WAVEFORM Switch—Determines the function of the CURSORS Position control. When pressed in (POSITION CURSORS mode), the CURSORS Position control functions as a cursor horizontal positioning control. When the push button is in the out position (SELECT WAVEFORM mode), the CURSORS Position control or the C1/C2 switch may be used to position the cursor to the desired waveform(s).

CURSORS Position Control—Provides for either horizontal positioning of the active cursor (or active cursors when there are two waveforms displayed in a display set) or for switching the cursors between waveform display sets. When cursors are positioned to a new waveform set, they return to the position that they had when they were last on that waveform set. Cursor positioning continues to function during SAVE mode, and measurements can be made on any displayed waveform. When an acquisition control is changed, the cursors return to the acquisition waveform set.

Cursors are placed on all waveforms in a display set. A display set is one or both waveforms from the following: Acquisition, CH 1 and CH 2; Reference 1, CH 1 and CH 2; Reference 2, CH 1 and CH 2; and Reference 3, CH 1 and CH 2. Cursors move to the acquisition waveform if they were on a SAVE REF waveform that is turned off. The acquisition parameters of the waveform set in which the cursors are located are displayed in the crt readout. Cursors movable by the CURSORS Position control are enclosed in a box.

When the displayable acquisition record length is greater than one screen, a one-screen window of the record is displayed. A bar graph indicates the position of the display window within the acquisition record. The position of the display window is adjusted to provide a display of the cursor position. If the displayed cursor is positioned to either edge of the display window, further positioning starts the waveform display scrolling in the opposite direction as the display-window position moves. Display-window positioning can be continued to the ends of the record, allowing observations and measurements to be made over the entire acquisition record.

SELECT C1/C2 (Cursor-Select) Switch—In Position CURS mode this switch selects the cursor(s) that can be positioned by the CURSORS Position control. Cursors are activated alternately with each press of the C1/C2 button. Each selected cursor is enclosed in a box. In Select Waveform mode, pressing the C1/C2 switch moves the cursor set between displayed waveforms.

(42) **MEMORY and Menu Controls**—These switches control MENU operation while the MENU is displayed, and they control the storage and display of the SAVE Reference waveforms when the MENU is not displayed.

WAVEFORM REFERENCE/MENU SELECT Switch—Selects either the MENU or SAVE REF MEMORY displays. In Waveform Reference mode, the MEMORY switches control the Save Reference Memory. In MENU mode, the MEMORY switches control the Menu, allowing selection of alternate parameters and modes that override the default front-panel settings.

SAVE REF MEMORY CONTROL—When the WAVEFORM REFERENCE/MENU SELECT switch is in the WAVEFORM REFERENCE position (button in), the MEMORY switches control the Save Reference Memory.

SAVE REF/→ Switch—Pressing this button just prior to pressing one of the DISPLAY ON/OFF buttons writes the displayed acquisition waveform into the selected Save

Reference memory. The written waveform remains displayed on the crt. A control change or a delay of five seconds between pressing the SAVE REF button and selecting a memory location cancels the SAVE request.

In 4K acquisition mode, a choice may be made to save the entire 4K acquisition or the 1K display window. To save a 4K acquisition, press SAVE REF, then press DISPLAY ON/OFF 1 twice. The 4K record fills MEMORY 1, 2, and 3. To save only the 1K displayed window, press SAVE REF, then press DISPLAY ON/OFF 1, then DISPLAY ON/OFF 2. The 1K display window may also be saved in MEMORY 2 or 3 by pressing SAVE REF, then the desired DISPLAY ON/OFF button.

Menu Select/DISPLAY ON/OFF Switches—These buttons select one of three memories that is either written to for saving a 1K acquisition waveform (if SAVE REF has been pressed) or toggles the reference memory display on or off (if the SAVE button has not been pressed). The stored waveforms of all three memories can be displayed at the same time. Two channels acquired in CHOP or ALT may be stored in a SAVE REF memory.

MENU CONTROL—When the WAVEFORM REFERENCE/MENU SELECT switch is in the MENU SELECT position (button out), the MEMORY switches control Menu Operation. Waveforms are only displayed with menus when a menu choice requires a waveform be displayed in order to perform the selected change. The Menu allows selection of alternate parameters and modes that override the default front-panel settings.

SAVE REF/→ Switch—When pressed, the next (to the right) Menu level is entered.

Menu Select/DISPLAY ON/OFF Switches—These three buttons select choices presented in the MENU. The ← button recalls the previous (to the left, higher) Menu level. The ↑ button selects the previous entry in the **current** Menu level. The ↓ button selects the next entry in the current Menu level.

MENU SELECTED FUNCTIONS

This part describes the Menu selected functions that provide selection of parameters, settings, and features not controlled by the front-panel switches.

ACQ MODE SETUP TABLE

ACQ MODE SETUP TABLE controls the acquisition mode setup using a table.

SELECT MODE—Displays the acquisition modes in a table. The desired modes for each sweep speed may be selected using the SEC/DIV switch to select the column, the CURSORS Position control selects the row, and the SELECT C1/C2 switch toggles the choice for the table position that is enclosed in a box.

SWP LIMIT—Selects the number of acquisitions before the acquisition system halts. SWP LIMIT may be reset by changing any control that affects acquisition parameters.

WEIGHT—Selects the weight of the last sample in AVERAGE mode.

A TRIG POS

A TRIG POS selects the number of points acquired prior to or following the trigger.

DISPLAY

DISPLAY controls the selection of display parameters.

DELTA T MODE—Selects either DELTA TIME or ONE OVER DELTA TIME for display in the readout.

VECTORS ON/OFF—Selects either DOTS or VECTORS as the waveform display mode. Vectors are not allowed in REPETITIVE mode.

SMOOTH ON/OFF—Selects the process with which the vector displays are produced when in PEAKDET or ACCPEAK.

With SMOOTH OFF, no reordering of the data points is done, and vectors are drawn between all of the minimum and maximum data points.

With SMOOTH ON, data points are reordered for correct slope and interpolated for drawing a smooth waveform. Smoothing looks at the change in value of

reordered data points between adjacent sample intervals. If the change in value does not exceed certain limits, the values are interpreted as a continuous slope for drawing either vectors or dots. If the value change exceeds the interpreted "no-change" limit, the data point value is not modified, and the vectors drawn in the display show a discontinuity in the waveform. This method of display of the waveform data provides a smoothed display of the waveform, yet retains the glitch-catching capabilities of PEAKDET or ACCPEAK modes.

DEFAULT

Selects the default acquisition modes for all sweep speeds (see Table 2-2 for the default modes).

FORMATTING

FORMATTING selects a SAVE REF memory for formatting. The vertical gain, horizontal gain, and vertical position of the selected reference waveform may be changed. The acquisition mode used to store the waveform may also be displayed.

TARGET REFERENCE—Selects one of the SAVE REF memories for formatting.

VGAIN—Allows adjustment of the vertical gain of SAVE REF memories.

VPOSITION—Allows adjustment of the vertical position of SAVE REF memories.

HMAG—Turns X10 horizontal magnification of SAVE REF memories on or off.

MODE—Displays the parameters used to acquire a SAVE REF memory.

PLOT

PLOT controls the transmission of waveforms over the X-Y Plotter output.

START—Initiates the transmission of a waveform over the X-Y Plotter output.

GRATICULE ON/OFF—Enables or disables plotting of the graticule.

SET UP—Allows calibration of analog plotter gain and offset.

SPEED—Allows selection of plotter pen speed.

ADVANCED FUNCTIONS

REFERENCE—Allows a SAVE REF memory to be Erased or Copied when one of the communication options is installed.

ERASE—Selects and erases a nonvolatile SAVE REF memory.

COPY—Selects and copies one nonvolatile SAVE REF memory to another SAVE REF memory.

COMM—Allows the selection of parameters for optional communications options, when they are present.

ACQ MODE SETUP TREE—Controls the acquisition mode setup using a tree. This provides control of the same functions as the ACQ MOD SETUP TABLE.

DEFAULT—Selects the default acquisition modes for all sweep speeds (see Table 2-2 for the default modes).

REPETITIVE—Selects the acquisition modes for sweep speeds from 0.05 μs to 2 μs per division.

FAST RECORD—Selects the acquisition modes for sweep speeds from 5 μs to 10 μs per division.

SLOW RECORD—Selects the acquisition modes for sweep speeds from 20 μs to 50 ms per division.

SLOW TRIGGERED—Selects the triggered acquisition modes for sweep speeds from 0.1 to 5 s per division or EXT CLOCK.

SLOW UNTRIGGERED—Selects the untriggered acquisition modes for sweep speeds from 0.1 to 5 s per division or EXT CLOCK.

DIAGNOSTICS—Controls the selection of diagnostic TESTS, EXERCISERS, and PICTURES.

Acquisition Modes

PEAK DETECT (PEAKDET) and SAMPLE—Select how samples are processed on successive acquisitions. See Table 2-2 for the default modes set by the SEC/DIV switch.

In Peak Detect mode, the minimum and maximum levels of the input signal within the time represented by 1/50 of a division unmagnified (1/25 of a division in CHOP or ALT) are digitized and stored in acquisition memory as a data pair. The displayed data points are connected by vectors.

In Sample mode, the signal is sampled at a rate that produces 100 samples per graticule division. In RECORD sampling, the displayed sample points are connected by either vectors or dots. For REPETITIVE Storage mode, the sample points are displayed as dots.

ACCPEAK—Will cause displays to accumulate. The largest maximum and smallest minimum sample acquisitions are retained for each trigger-referenced sample record over multiple acquisition cycles. When ACCPEAK is used with hardware peak detection (50 μs per division to 0.1 s per division), updating of maximum and minimum samples also occurs within each time-base clock period. Changing any switch that affects the acquisition parameters resets ACCPEAK displays. ACCPEAK mode is valid for triggered acquisitions only and is not operational in any mode that does not allow triggers (see Table 2-2).

AVERAGE—Is used for multiple record averaging. Whenever AVERAGE is selected, SAMPLING is also selected automatically. When on, a normalized algorithm is used for continuous display of the signal at full amplitude during the averaging process. Averaging is the default for REPETITIVE Store mode only. The amplitude resolution increases with the number of weighted acquisitions included in the display. The number of weighted acquisitions included in the AVERAGE display is Menu selectable. The default weight of AVERAGE mode is 1/4. Other choices are Menu selectable. The number of sweeps (SWP LIMIT) allowed to occur before averaging stops is also Menu selectable.

REAR PANEL

Refer to Figure 2-9 for location of items 43 through 45.

(43) **EXT Z-AXIS Input Connector**—Provides an input connector allowing external signals to be applied to the Z-Axis circuit to intensity modulate the NON STORE waveform display. Applied signals do not affect the display waveshape. External signals with fast rise and fall times provide the best defined intensity modulation. Noticeable intensity modulation is produced at normal viewing intensity levels by a 5 V p-p signal. The Z-Axis signals must be time-related to the trigger signal to obtain a stable intensity-modulation pattern on the displayed waveform.

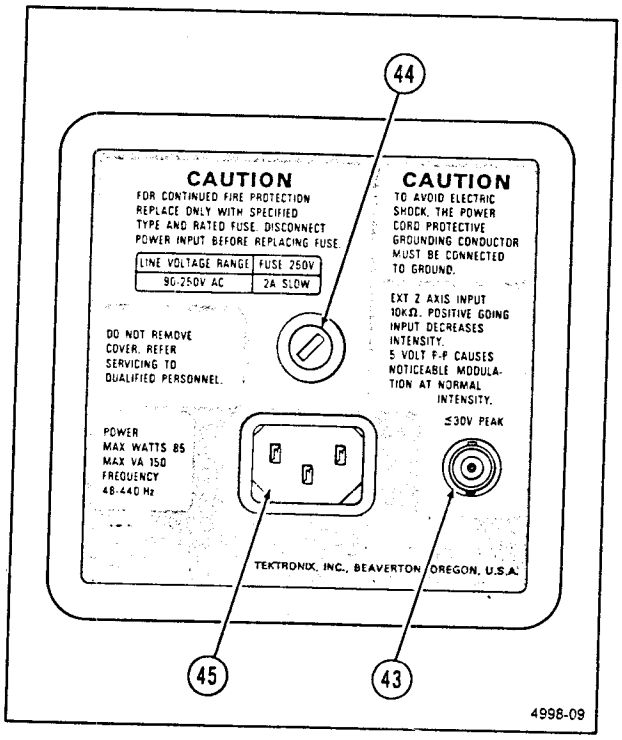


Figure 2-9. Rear Panel.

(44) **Fuse Holder**—Contains the ac-power-source fuse. See the rear panel nomenclature for fuse rating and line voltage range.

(45) **Detachable Power Cord Receptacle**—Provides the connection point for the ac-power source to the instrument.

SIDE PANEL

The standard side panel includes one AUXILIARY CONNECTOR. Refer to Figure 2-10 for the location of item 46.

(46) **AUXILIARY CONNECTOR**—Provides connections for an X-Y Plotter and an External Clock input (see Table 2-4).

NOTE

To meet EMI regulations and specifications, use the specified shielded cable and metal connector housing with the housing grounded to the cable shield for connections to the AUXILIARY CONNECTOR.

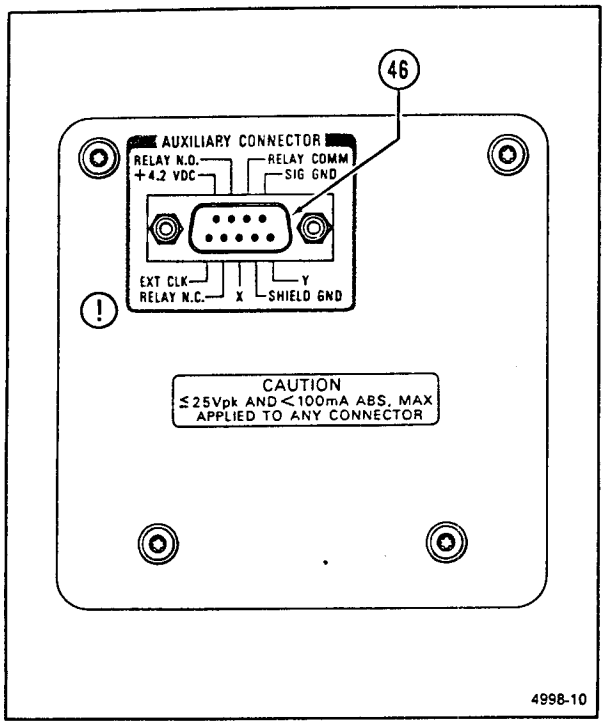


Figure 2-10. Side Panel.

X-Y Plotter Connections—Provide connections for X-Axis output, Y-Axis output, and Pen Lift control to drive an external X-Y Plotter. All displayed waveforms and the crt readout are transmitted over the Plotter Interface. The settling time allowed for each movement is approximately proportional to the distance of the movement. Connections for Signal Ground and Shield Ground are also provided for grounding between the instrument and the external X-Y Plotter. Waveforms and the Readout are plotted on the crt while a plot is in progress.

To be fully compatible, the X-Y Plotter used must have X and Y inputs with sensitivity control and penlift control.

Signals available at the AUXILIARY CONNECTOR allow the Pen Lift circuit to be wired for a plotter with either active HI or active LO drive requirements and several logic families. Examples for both an active HI and an active LO TTL drive are shown in Figure 2-11.

EXT CLK Input—Provides an input for EXT CLOCK signals (up to 1000 samples per second) to the storage acquisition circuitry in conjunction with the EXT CLK position of the A SEC/DIV switch. Samples are referenced by falling edges. Input is TTL compatible. Samples become visible by pairs, as SCAN or ROLL. Several clocks are required before the point associated with the first clock is visible.

Table 2-4

Auxiliary Connector

Pin Number	Function
1	EXT CLK Input
2	Pen Lift, Normally Closed
3	X Output
4	SHIELD GND
5	Y Output
6	+4.2 V
7	Pen Lift, Normally Open
8	Pen Lift, Relay Common
9	SIG GND

CRT READOUT

The Readout System provides an alphanumeric display of information on the crt along with the waveform displays. The readout (non MENU) is displayed in three rows of characters. Two rows are within the top graticule division, and the other row is within the bottom graticule division. The locations and types of information displayed under normal operating modes are illustrated in Figure 2-12.

NON STORE Mode

In NON STORE mode the current settings of the VOLTS/DIV and SEC/DIV switches are displayed. Greater-than symbols (>) are used to indicate uncalibrated VOLTS/DIV and SEC/DIV switch settings. A down-arrow symbol (↓) is used in front of the CH 2 VOLTS/DIV readout to indicate CH 2 INVERT. For Horizontal Display Mode of BOTH and B only, the DELAY TIME POSITION readout is also displayed. The AC-GND-DC input coupling selection is indicated in the associated VOLTS/DIV readout with a tilde symbol (~) above the volts symbol for AC, a ground symbol (⏚) for GND, and no extra symbol for DC input coupling.

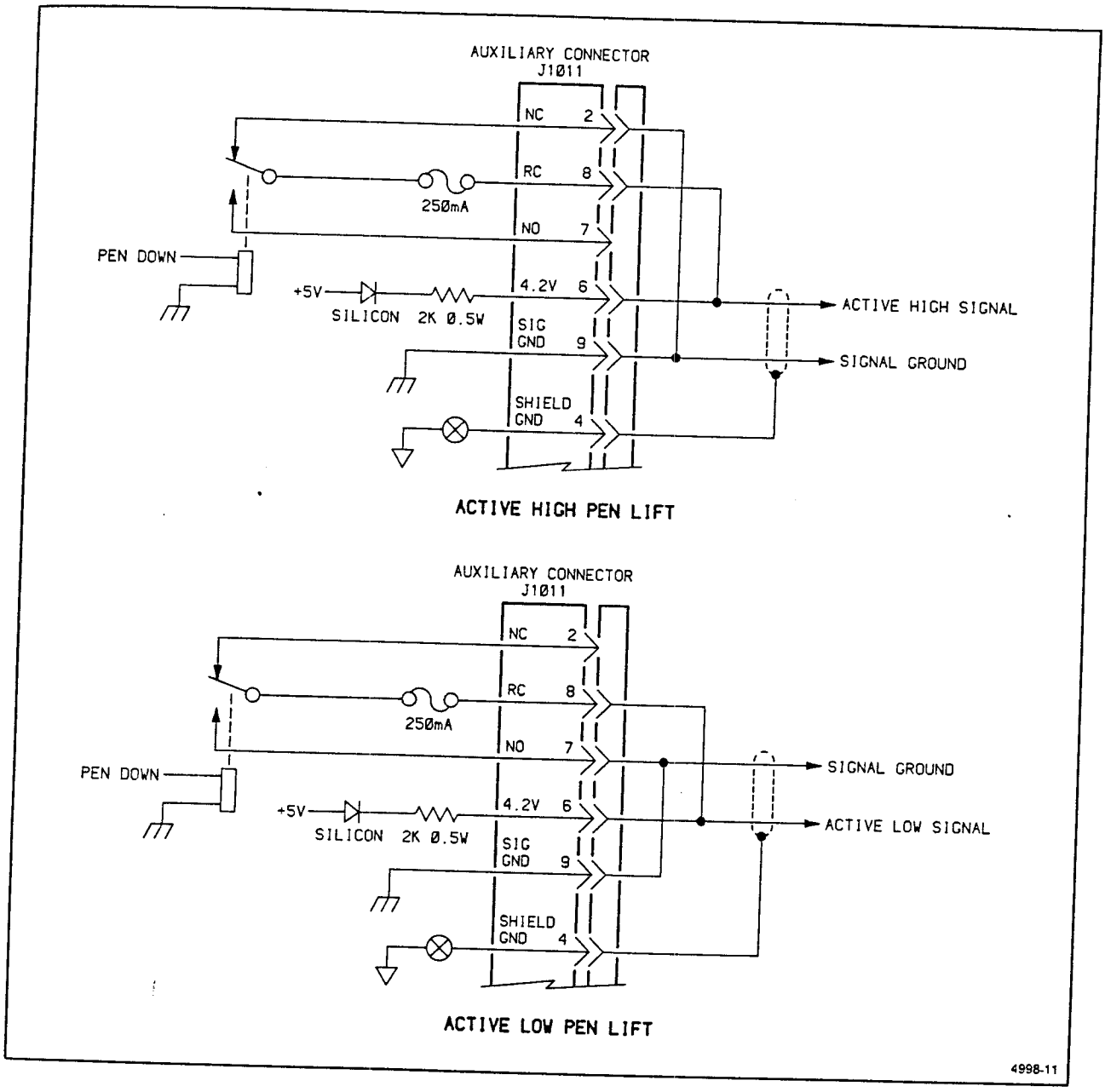


Figure 2-11. X-Y Plotter interfacing.

STORE Mode

In STORE mode, many of the crt readout displays are associated with the parameters of stored waveforms.

PARAMETER READOUT. Displays the VOLTS/DIV, SEC/DIV and B DELAY TIME settings of the displayed waveforms on which the cursors are placed. The AC-GND-DC input coupling selection is indicated in the associated VOLTS/DIV readout with a tilde symbol (~) above the volts symbol for AC, a ground symbol (⏚) for GND, and no extra symbol for DC input coupling. If the VOLTS/DIV switch is switched beyond the available expansion or compression range, the readout is tilted, indicating that the VOLTS/DIV switch setting and the VOLTS/DIV readout no longer agree. In 4K COMPRESS, a **c** is displayed in front of the SEC/DIV readout.

CURSOR READOUT. Displays the voltage difference (either ΔV 1 or ΔV 2) and the time difference between cursors. When either BOTH or B HORIZONTAL mode is selected, the DELAY TIME POSITION is displayed. Independent fields for CH 1 VOLTS/DIV, CH 2 VOLTS/DIV, A SEC/DIV, and B SEC/DIV are provided. When making ground referenced voltage measurements (ground dot displayed and cursor on ground dot) the Δ symbol is replaced by a ground symbol (⏚).

When the acquisition record length is longer than one screen, a bar graph is used to indicate the position of the display window within the acquisition record.

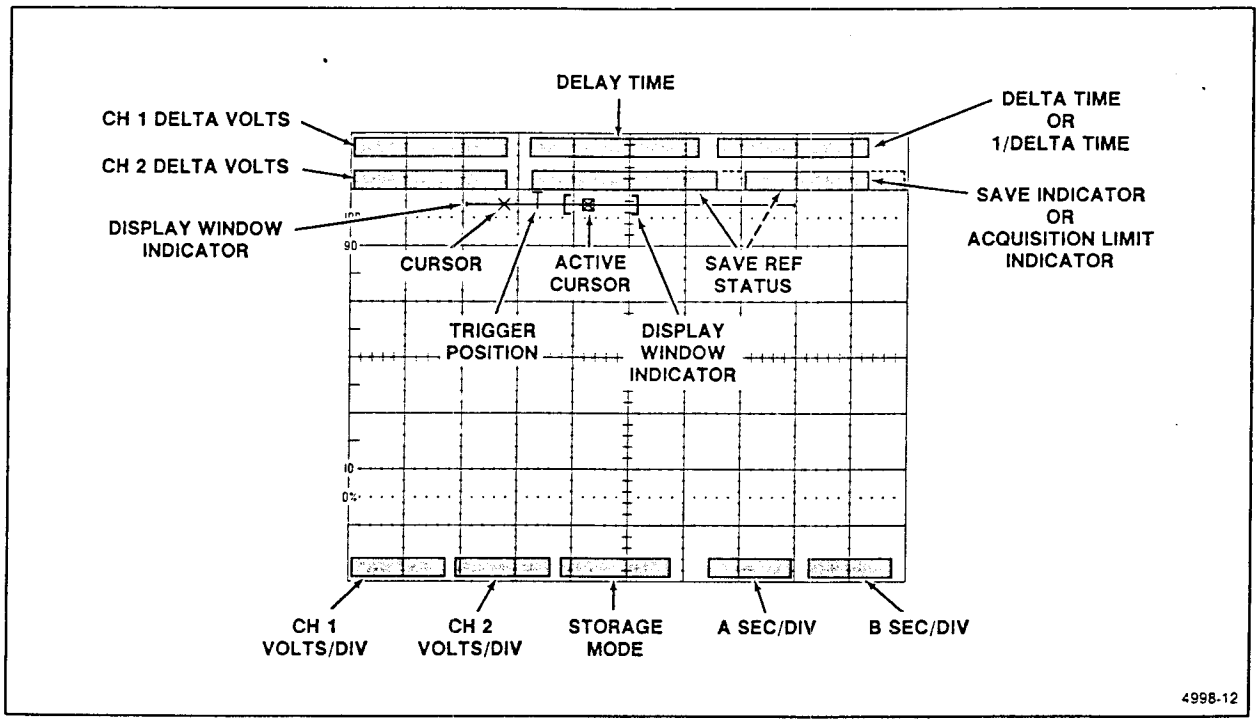


Figure 2-12. Crt readout display.

OPERATING CONSIDERATIONS

This part contains basic operating information and techniques that should be considered before attempting to make any measurements with the instrument.

GRATICULE

The graticule is internally marked on the faceplate of the crt to eliminate parallax-viewing errors and to enable measurements (see Figure 2-13). The graticule is marked with eight vertical and ten horizontal major divisions. In addition, each major division is divided into five subdivisions. The vertical deflection factors and horizontal timing are calibrated to the graticule so that accurate measurements can be made directly from the crt. Also, percentage marks for the measurement of rise and fall times are located on the left side of the graticule.

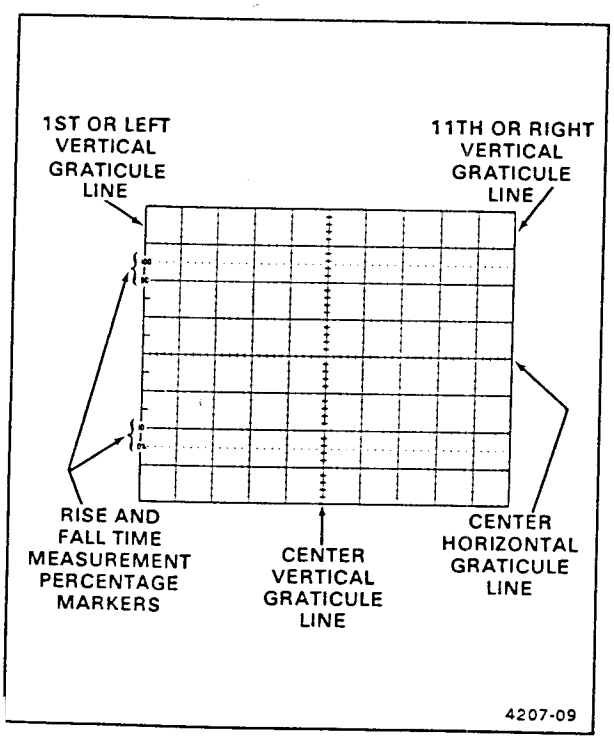


Figure 2-13. Graticule measurement markings.

GROUNDING

The most reliable signal measurements are made when the oscilloscope and the unit under test are connected by a common reference (ground lead) in addition to the signal lead or probe. The probe's ground lead provides the best grounding method for signal interconnection and ensures the maximum amount of signal-lead shielding in the probe cable. A separate ground lead can also be connected from the unit under test to the oscilloscope GND receptacle located on the oscilloscope's front panel.

SIGNAL CONNECTIONS

Probes

Generally, the accessory probes supplied with the instrument provide the most convenient means of connecting a signal to the vertical inputs of the instrument. The probe and probe lead are shielded to prevent pickup of electromagnetic interference, and the 10X attenuation factor of the probe offers a high input impedance that minimizes signal loading in the circuitry under test. The attenuation factor of the standard accessory probe is coded so that the VOLTS/DIV readout seen on the crt is automatically switched to the correct scale factor when the probe is attached.

Both the probe itself and the probe accessories should be handled carefully at all times to prevent damage to them. Avoid dropping the probe body. Striking a hard surface can cause damage to both the probe body and the probe tip. Exercise care to prevent the cable from being crushed or kinked. Do not place excessive strain on the cable by pulling.

The standard-accessory probe is a compensated 10X voltage divider. It is a resistive voltage divider for low frequencies and a capacitive voltage divider for high-frequency signal components. Inductance introduced by either a long signal or ground lead forms a series-resonant circuit. This circuit will affect system bandwidth and will ring if driven by a signal containing significant frequency

components at or near the circuit's resonant frequency. Oscillations (ringing) can then appear on the oscilloscope waveform display and distort the true signal waveshape. Always keep both the ground lead and the probe signal-input connections as short as possible to maintain the best waveform fidelity.

Misadjustment of probe compensation is a common source of measurement error. Due to variations in oscilloscope input characteristics, probe compensation should be checked and adjusted, if necessary, whenever the probe is moved from one oscilloscope to another or between channels. See the probe compensation procedure in "Operator's Check and Adjustments", or consult the instructions supplied with the probe.

Coaxial Cables

Cables may also be used to connect signals to the vertical input connectors, but they may have considerable effect on the accuracy of a displayed waveform. To maintain the original frequency characteristics of an applied signal, only high-quality, low-loss coaxial cables should be used. Coaxial cables should be terminated at both ends in their characteristic impedance. If this is not possible, use suitable impedance-matching devices.

INPUT-COUPLING CAPACITOR PRECHARGING

When the Input Coupling switch is set to the GND position, the input signal is connected to ground through the input-coupling capacitor and a high resistance value. This series combination forms a precharging circuit that allows the input-coupling capacitor to charge to the average dc voltage level of the signal applied to the input connector. Thus, any large voltage transients that may accidentally be generated are not applied to the vertical amplifier's input when the input coupling is switched from GND to AC. The precharging network also provides a measure of protection to the external circuitry by reducing the current level that is drawn from the external circuitry while the input-coupling capacitor is charging.

If AC input coupling is in use, the following procedure should be followed whenever the probe tip is connected to a signal source having a different dc level than that previously applied. This procedure becomes especially useful if the dc-level difference is more than ten times the VOLTS/DIV switch setting.

1. Set the AC-GND-DC (input coupling) switch to GND before connecting the probe tip to a signal source.

2. Touch the probe tip to the oscilloscope GND connector.

3. Wait several seconds for the input-coupling capacitor to discharge.

4. Connect the probe tip to the signal source.

5. Wait several seconds for the input-coupling capacitor to charge to the dc level of the signal source.

6. Set the AC-GND-DC switch to AC. A signal with a large dc component can now be vertically positioned within the graticule area, and the ac component of the signal can be measured in the normal manner.

OPERATOR'S CHECKS AND ADJUSTMENTS

To verify the operation and basic accuracy of your instrument before making measurements, perform the following checks and adjustment procedures. If adjustments are required beyond the scope of these operator's checks and adjustments, refer the instrument to qualified service personnel.

For new equipment checks, before proceeding with these instructions, refer to "Preparation for Use" in this manual to prepare the instrument for the initial start-up before applying power.

INITIAL SETUP

1. Verify that the POWER switch is OFF (switch is in the out position), then plug the power cord into the ac power outlet.

2. Press in the POWER switch (ON) and set the instrument controls to obtain a baseline trace:

Display

A and B INTENSITY	Midrange
STORAGE/READOUT INTENSITY	Midrange (with READOUT on)
FOCUS	Best defined display

Vertical (Both Channels)

VERTICAL MODE	CH 1
POSITION	Midrange
VOLTS/DIV	50 mV
AC-GND-DC	DC
Var Volts/Div	CAL (in detent)
BW LIMIT	Off (button out)

Horizontal

HORIZONTAL MODE	A
A SEC/DIV	0.5 ms
Var Sec/Div	CAL (in detent)
POSITION	Midrange
X10 Mag	Off (Var Sec/Div knob in)
B DELAY TIME POSITION	Fully counterclockwise

Triggers

VAR HOLDOFF	NORM (fully counterclockwise)
A&B INT	VERT MODE
A SOURCE	INT
A Mode	P-P AUTO
A LEVEL	For a stable display (with signal applied)
A SLOPE	OUT (plus—button out)
B LEVEL	B RUNS AFTER DELAY (fully clockwise)
B SLOPE	OUT (plus—button out)
HF REJECT	OFF (fully counterclockwise)

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/MENU SELECT	WAVEFORM REFERENCE (button in)

3. Adjust the INTENSITY and FOCUS controls for the desired display brightness and best focused trace.

4. Adjust the Vertical and Horizontal POSITION controls to position the trace within the graticule area.

5. Allow the instrument to warm up for 20 minutes before commencing the adjustment procedures. Reduce the INTENSITY levels during the waiting time.

TRACE ROTATION ADJUSTMENT

NOTE

Normally, the trace will be parallel to the center horizontal graticule line, and TRACE ROTATION adjustment is not required.

1. Preset the instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Use the Channel 1 POSITION control to move the baseline trace to the center horizontal graticule line.

3. If the baseline trace is not parallel to the center horizontal graticule line, use a small-bladed screwdriver or alignment tool to adjust the TRACE ROTATION control to align the trace with the graticule line.

PROBE COMPENSATION

Misadjustment of probe compensation is a source of measurement error. The attenuator probes are equipped with a compensation adjustment. To ensure optimum measurement accuracy, always check probe compensation before making measurements. Probe compensation is accomplished by:

1. Preset the instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Connect the two 10X probes (supplied with the instrument) to the CH 1 OR X and CH 2 OR Y input connectors. Observe that the CH 1 VOLTS/DIV readout changes from 5 mV to 50 mV when the 10X probe is attached to the CH 1 OR X input.

3. Remove the hook tip from the end of each probe.

NOTE

While the probe tip is in the PRB ADJ connector, use care not to to break off the probe tip.

4. Insert the Channel 1 probe tip into the PRB ADJ connector.

5. Use the CH 1 POSITION control to vertically center the display. If necessary, adjust the A TRIGGER LEVEL control to obtain a stable display on the plus (OUT) SLOPE.

6. Check the waveform display for overshoot and rounding (see Figure 2-14); if necessary, use a small-bladed screwdriver to adjust the probe compensation for a square front corner on the waveform.

7. Remove the Channel 1 probe tip from the PRB ADJ connector.

8. Insert the Channel 2 probe tip into the PRB ADJ connector.

9. Set the VERTICAL MODE to CH 2.

10. Set the A TRIGGER A&B INT switch to CH 2.

11. Use the CH 2 POSITION control to vertically center the display.

12. Check the waveform display for overshoot and rounding (see Figure 2-14); if necessary, use a small-bladed screwdriver to adjust the probe compensation for a square front corner on the waveform.

NOTE

Refer to the instruction manual supplied with the probe for more complete information on the probe and probe compensation.

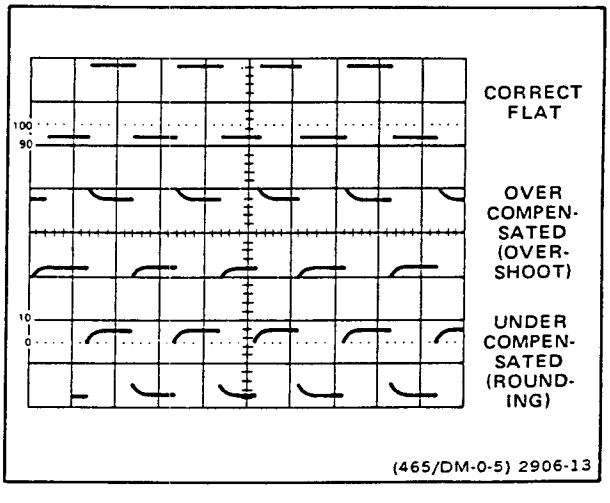


Figure 2-14. Probe compensation.

HORIZONTAL ACCURACY CHECK

A check of the horizontal timing can be made using the time measurement capability of the CURSOR measurement mode:

1. Preset instrument controls and obtain a baseline trace as described in "Initial Setup".

2. Set:

CH 1 AC-GND-DC	GND
STORE/NON STORE	STORE (button in)
A SEC/DIV	1 ms
PRETRIG/POST TRIG	POST TRIG (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)

3. Turn the Horizontal POSITION control to align the start of the trace to the first vertical graticule line.

4. Turn the Vertical POSITION control to align the baseline trace with the center horizontal graticule line.

5. Position the active cursor to the second vertical graticule line using the CURSORS Position control.

6. Push the SELECT C1/C2 switch to activate the other cursor.

7. Position the active cursor to the tenth vertical graticule line using the CURSORS Position control for a spacing of eight divisions between cursors.

8. Check that the Delta Time readout is $\geq$ 7.84 ms and $\leq$ 8.16 ms.

9. Verify that the CH 1 probe tip is in the PRB ADJ connector.

10. Set the CH 1 AC-GND-DC switch to DC.

11. Adjust the SEC/DIV switch setting for a display of at least one full period of the probe adjust signal (0.1 or 0.2 ms per division).

12. Use the Vertical and Horizontal POSITION controls to center the display.

13. Use the CURSORS Position control and the CURSORS SELECT C1/C2 button to align the cursors with the rising edges of the PRB ADJ signal (measurement is of the probe adjust signal period). Note the cursor time difference readout and the graticule measurement (horizontal distance between rising edges as taken from the graticule markings) of the signal for later reference.

14. Check that the cursor readout of the probe adjust signal period and the graticule measurement of the calibrator period are within ±2%.

15. Set the STORE/NON STORE switch to the NON STORE position (button out).

16. Determine the horizontal graticule measurement of the probe adjust signal period. Note the reading for later reference.

17. Check that the NON STORE Mode probe adjust signal period measurement obtained from the graticule markings is within ±3% of the STORE Mode probe adjust signal period obtained in step 13.

18. Set the X10 MAG switch to on (pull Var Sec/Div knob out) and set the A SEC/DIV switch setting to obtain a display of at least one full period of the probe adjust signal (0.1 or 0.2 ms per division).

19. Check that the magnified NON STORE Mode probe adjust sugnal period measurement obtained from the graticule markings is within ±4% of the STORE Mode probe adjust signal period obtained in step 13.

THEORY OF OPERATION

SECTION ORGANIZATION

This section contains a functional description of the 2230 Digital Storage Oscilloscope. The discussion begins with a summary of instrument functions. Following the general description, each major circuit is explained in detail. Functional block diagrams and schematic diagrams are used to show the interconnections between parts of the circuitry, to indicate circuit components, and to identify interrelationships with the front-panel controls.

Schematic diagrams and the overall block diagrams are located in the tabbed "Diagrams" section at the back of this manual. The schematic diagram associated with each description is identified in the text and indicated on the tab of the appropriate foldout page by a numbered diamond symbol. For best understanding of the circuit being described, refer to both the appropriate schematic diagram and the functional block diagram.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within the instrument. Functions and operation of the logic circuits are represented by logic symbology and terminology. Most logic functions are described using the positive-logic convention. Positive logic is a system where the more positive of two levels is the TRUE (or 1) state; the more negative level is the FALSE (or 0) state. In this logic description, the TRUE state is HI, and the FALSE state is LO. The specific voltages which constitute a HI or a LO state vary between specific devices. For specific device characteristics, refer to the manufacturer's data book.

Linear Devices

The operation of individual linear integrated circuit devices is described in this section using waveforms or graphic techniques to illustrate their circuit action.

GENERAL DESCRIPTION

Introduction

In the following overall functional description of the instrument, refer to the basic block diagram, Figure 3-1, and to the detailed block diagrams located in the "Diagrams" section of this manual. Each major block in the diagram represents a major circuit within the instrument. In Figure 3-1, the numbered diamond symbol in each block indicates the schematic diagram number. Much of the analog portion of the oscilloscope operates without direction from the Microprocessor circuitry. These portions of the instrument are described first, with appropriate references to areas that either provide information to the Microprocessor or are controlled by the instrument's storage circuitry. The Microprocessor and Storage circuit descriptions follow the more conventional portions of the instrument's circuitry.

Vertical

Signals to be displayed on the crt (cathode-ray tube) are applied to either or both the CH 1 OR X and the CH 2 OR Y input connectors. The signals may be coupled to the attenuator either directly (DC) or through an input-coupling capacitor (AC). The inputs may also be disconnected, and the input to the attenuators grounded, by switching to the GND position of the input coupling switch. In the GND position, the ac-coupling capacitor is allowed to precharge to the dc level present at the input connector. This precharging prevents large trace shifts of the display when switching from GND to AC coupling. The Attenuators are switched by the front-panel VOLTS/DIV switches and scale the applied signal level to obtain the desired display amplitude. Information about the Input Coupling switch and the channel VOLTS/DIV switch positions is read by the Microprocessor. These signals control the STORE mode ground-reference acquisition and the crt readout displays of the Input Coupling and VOLTS/DIV switch settings of the active channel(s).

Scaled output signals from the Attenuators are applied to the Vertical Preamplifiers for amplification. The Channel 2 Preamplifier has additional circuitry, permitting the operator to invert the Channel 2 display on the cathode-ray tube (crt). Trigger pickoffs in each channel supply a

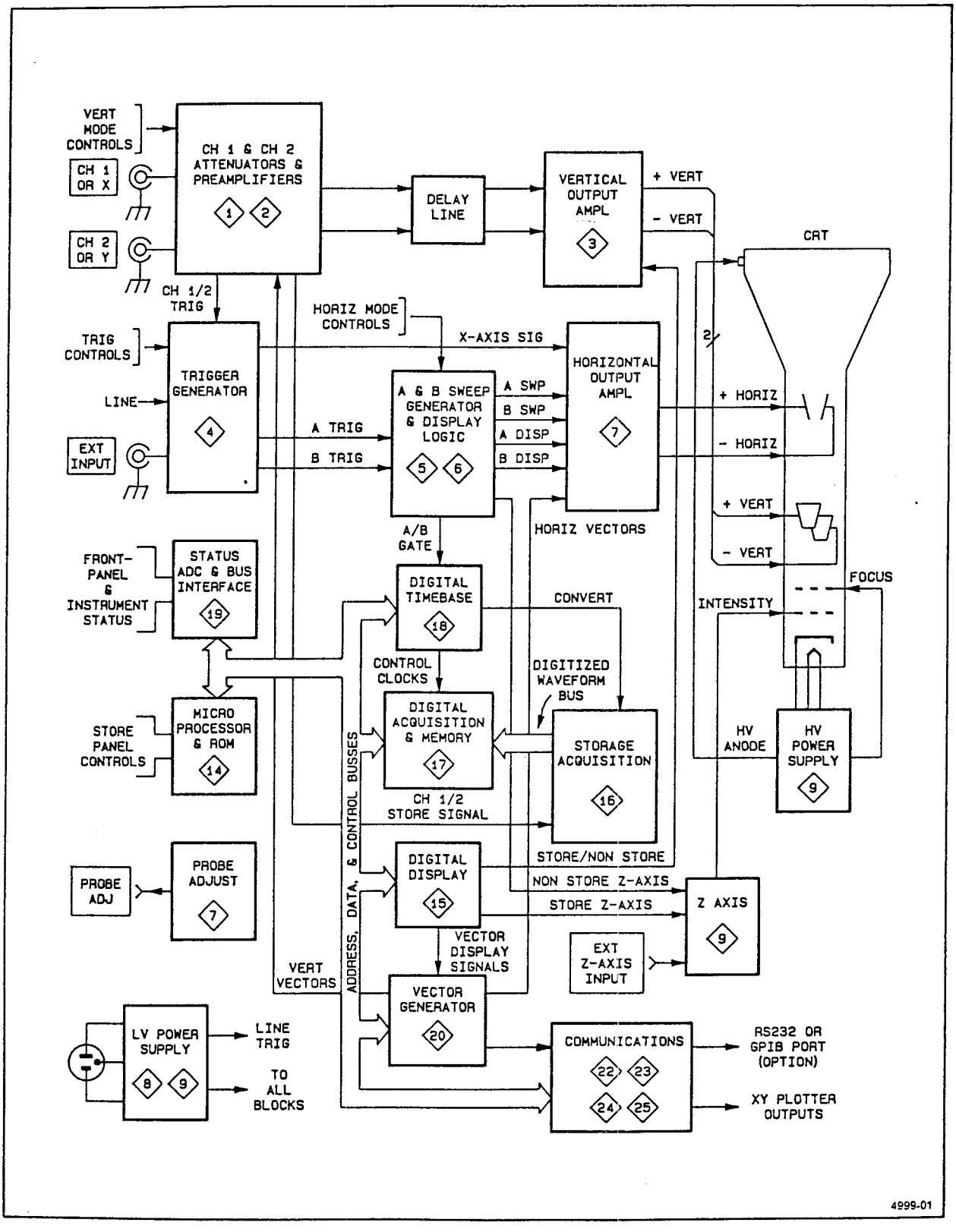


Figure 3-1. Simplified block diagram.

trigger signal to the Trigger Amplifier when internal triggering is selected. Other signal pickoffs provide vertical position information to the Position Signal Conditioning circuitry for vertically positioning the stored signal. The final stage of the Vertical Preamplifier for each channel provides one of two signals; either the vertical channel signal for the analog presentation on the crt or the vertical acquisition signal to be digitized by the storage circuitry.

Channel signals either for direct analog presentation on the crt or for application to the Storage digitizing circuitry are selected by the analog Channel Switch under control of the front-panel VERTICAL MODE switches. The switching signals from the Channel Switch Logic control a diode gate (Channel Switch) that selects the channel signal(s) to be applied to the Delay-line Driver. If ADD is selected, both channel signals are applied to the Delay-line Driver where the signals are summed together. The Delay-Line Driver provides the proper signal-driving level and impedance match to the Delay Line, where the vertical signal is delayed approximately 100 ns with respect to the trigger signal. The vertical signal delay allows time for the Horizontal circuitry to start the sweep before the vertical signal is applied to the crt.

Whenever STORE mode is selected, analog signals from the Storage circuitry are supplied to the Channel Switch circuit. Under control of the Channel Switch Logic, which is in turn switched by signals from the Display Controller, the analog display signal out of the final Vertical Preamplifier stage in each channel is biased off. The Channel 1 and Channel 2 Acquisition signals from the final preamplifiers are then biased on to pass the signals to be digitized to the Storage circuitry. At the same time, the Channel Switch (diode gate) is switched to pass the Storage vertical signal to the Delay Line Driver input.

Final amplification of the vertical signal (either STORE or NON STORE) is done by the Vertical Output Amplifier. This stage produces the signal levels that vertically deflect the crt electron beam. This amplifier stage also contains the vertical trace separation circuitry that separates the Nonstore A Intensified trace from the B Delayed trace when Alt Horizontal display mode is selected. The amount of trace separation is controlled using the front panel TRACE SEP knob. Another circuit feature in the Vertical Output Amplifier is the nonstore bandwidth limit (BW LIMIT) circuitry that follows the Delay Line. Either the full 100 MHz bandwidth or the limited 20 MHz bandwidth for the nonstore signal display may be selected. STORE mode signals are picked off in the Preamplifier and are not bandwidth limited by the BW LIMIT switch.

Triggering

The Triggering circuitry uses either the Internal Trigger signal obtained from the input signal(s), an External Trigger signal, or a Line Trigger signal derived from the ac-power-source to develop trigger signals for the Sweep Generator. The Auto Trigger circuit sets the range of the Trigger Level to conform approximately to the peak-to-peak amplitude of the selected trigger signal when either Auto or TV Field Trigger mode is selected. In Norm mode, the TRIGGER LEVEL control must be adjusted to the signal level before a sweep will be triggered. ROLL Storage (selectable at the slower sweep speeds in STORE mode) overrides the triggering circuit functions; a continuous signal acquisition is made and the signal displayed without the need of a trigger signal.

The triggering circuitry contains the TV Field Sync circuit. This circuit provides stable triggering on television vertical-sync pulses when in the TV Field triggering mode. TV Line triggering is possible using P-P AUTO trigger mode.

Signal pickoffs from the Internal Trigger circuitry provide the X-Axis signal for the nonstore X-Y display mode and the B trigger signal for triggered B Sweeps.

A Sweep

The A Sweep Generator and Logic circuits control the nonstore sweep generation and both the Store and the nonstore A Sweep timing. When the A TRIGGER mode switches are set to either P-P AUTO or TV FIELD and no trigger signal is present, the Auto Baseline circuit causes the Sweep Logic circuit to produce a sweep for reference purposes. In the NORM setting, the Auto Baseline circuit is disabled and nonstore sweeps are not generated until a trigger event occurs. NORM trigger mode is used to obtain stable triggering on low-repetition rate signals that do not provide a trigger before an auto baseline is generated. SGL SWP (single sweep) trigger mode allows only one sweep to be generated after being reset and is used to obtain the waveform from a one-shot event.

ROLL and SCAN Storage modes are useful in capturing low-frequency and low-repetition rate waveforms. In SCAN mode, receiving a trigger causes the pretrigger portion of the waveform to update as a block. The post-trigger waveform updates from the trigger point to the right edge of the screen as new data is acquired. ROLL Storage acquisitions differ from the Nonstore sweeps and SCAN Storage mode in that a trigger signal is not used for acquisition of the signal or displaying the waveform. The A Sweep Logic circuitry provides gating and holdoff signals used by the Storage circuitry to control its acquisition and display cycles for all storage modes, except ROLL.

The $\overline{\text{A Gate}}$ signal applied to the A Miller Sweep Generator circuit starts the Nonstore linear sweep with a ramp time that is controlled by the A SEC/DIV switch setting.

Switch position pickoffs supply the SEC/DIV switch setting information to the Microprocessor for use in STORE mode horizontal timing. The A SEC/DIV switch setting is also displayed on the crt for both Store and Nonstore operation.

B Sweep

The Alternate B Sweep Circuitry controls the Nonstore BOTH and B Delayed Horizontal mode displays. This circuitry includes the B Miller Sweep Generator and B Sweep Logic circuitry. STORE mode B timing is controlled by the B SEC/DIV switch. BOTH Horizontal mode is not available with STORE. In STORE mode, the BOTH selection displays an A Intensified Trace only. The intensified zone on the A trace indicates the position and approximate amount of the A trace that is displayed by the B Delayed Display.

Horizontal

Nonstore A and B Sweep signals (or the X-Axis signal from the X-Y Amplifier in the nonstore X-Y Display mode) are applied to the Horizontal Preamplifier where one is selected and amplified. Gain in the Preamplifier is switchable between X1 and X10. The X10 gain is used for Nonstore X10 Magnification. STORE mode X10 expansion is done digitally and reflected in the horizontal deflection signals supplied after the Horizontal Preamplifier. Horizontal positioning of both the Store and the nonstore display is done by applying a horizontal position dc offset to the Horizontal Preamplifier. The amplified nonstore horizontal signal is applied to the Horizontal Mux circuit where it is available for selection.

STORE mode horizontal deflection signals are also applied to the Horizontal Mux. Selection of either the nonstore sweep signals or the store deflection signals is done by control signals from the Channel Switch Logic in the Vertical circuitry. The selected horizontal deflection signals are then amplified by the Horizontal Output Amplifier to the levels needed to drive the crt's horizontal deflection plates.

Microprocessor

The Microprocessor (MPU) controls the digital storage and display sections of the oscilloscope. Under firmware control (firmware is the programmed instructions contained in read-only memory), the Microprocessor monitors the operation of the instrument and sets up the circuitry to perform as dictated by the front-panel control settings. Data transfer to and from the Microprocessor and address selection of a device to be communicated with are done over a 20-line I/O bus. The lower eight lines (AD0 through AD7) form a combined address/data bus while the remaining 12 lines (A8 through A19) are for addressing only. Timing for the execution of instructions, addressing, and data transfers is provided by an external, crystal-controlled oscillator that drives the Microprocessor clock generator. The Microprocessor clock circuit further divides the input clock frequency to generate two lower clock frequencies. The clock circuit also generates the Ready and Reset control signals to the Microprocessor.

Storage front-panel control settings are passed to the Microprocessor via eight-bit bus drivers. Settings of the analog front-panel controls and switches are also provided to the MPU, but via different bus drivers. The Status ADC and Bus Interface circuitry provides the interfaces from the analog front-panel controls to the data bus.

Status ADC and Bus Interface

Switch settings and status bits are applied directly to bus drivers. Each data bit then corresponds to a switch setting (either open or closed) or a status bit logic level (either HI or LO). Analog front-panel information is multiplexed to an analog-to-digital converter where it is converted to a digital value and applied to a bus driver. When the Microprocessor reads the bus, it obtains a data byte that represents the position value for a single control rather than the switch or status data bits of the digital-type information. The Microprocessor determines the control settings from the value of the data bytes or status bits received and sets up the digital storage circuits accordingly.

Storage Acquisition

Input signals to be digitized are selected by the Channel Switch. Either or both (for ADD) of the input signals picked off from the Vertical Preamplifier may be selected. The differential output signal from the Channel Switch is converted to a single-ended signal for application to the Sample-and-Hold amplifier. The input diode bridge in the Sample-and-Hold circuit is strobed to pass a sample of the signal to charge the hold capacitor. While the signal sample is held for conversion, the diode bridge is reverse biased, and the charge on the Hold capacitor remains at a fixed level. The sample buffer amplifier applies the voltage level on the Hold capacitor to the Analog-to-Digital Converter stage for conversion to an eight-bit digital signal. The output signals are then shifted from the emitter-coupled logic (ECL) level obtained from the ADC to the transistor-transistor-logic level (TTL) and passed to the digitized signal bus for transfer to the Acquisition Memory.

Digital Acquisition

Digitized waveforms are transferred from the ECL-to-TTL level shifters via the digitized data bus to the A/D Buffer of the Acquisition Memory circuit. The buffered data is applied to two identical registers; the Min Register and the Max Register. Data is alternately clocked into the registers by the MINCLK and MAXCLK clock signals. The

actual clocking that occurs depends on the sampling mode (Min/Max, Sampling, or X-Y). The same waveform data is also applied to opposite comparator inputs of two eight-bit magnitude comparators. Output data from the Min and Max Registers is applied to the other comparator's input pins, with the Min Register data going to the Min Comparator and the Max Register data going to the Max Comparator.

In Min/Max mode, the first data byte taken in a sample window (set by the SEC/DIV switch setting) is clocked into both registers. That data byte is then compared with the next data sample or samples (determined by the sample window) being applied to the inputs of the Min and Max Registers. If the data byte is either smaller in magnitude than the last clocked minimum or greater in magnitude than the last clocked maximum, a NEWMIN or a NEWMAX signal is generated. The signal is routed through the Min/Max Clock Selector back to the clock input of the Min or Max Register (Min if it is a new minimum amplitude or Max if it is a new Maximum amplitude) and the new signal is clocked into the register. At the end of a Min/Max sample window, the data present at the output of the Min and Max Registers is clocked into the Swap Registers to be transferred to the Acquisition Memory.

When record sampling mode is selected, each waveform sample is successively clocked into the Min and Max Registers on alternate ODDCLK and $\overline{\text{ODDCLK}}$ signals. When X-Y mode is selected, the Channel 1 and Channel 2 waveforms are sampled in a chopped manner, with samples of the two channel signals being taken with less time between the samples than in normal record sampling mode. Channel 1 data is clocked into the Min Register, and Channel 2 data is clocked into the Max Register.

Four eight-bit Swap Registers are used to reorder the Max and Min data obtained from each sample window. The Max Register data is clocked into two of the registers in parallel, and the Min Register data is clocked into the other two registers in parallel. The Min and Max data output from one of the Swap Registers in each set of two is applied to two busses going to the Acquisition Memory. If the Max and Min data is to be reversed to maintain the correct time order of the samples before being stored, the alternate swap register in each set of two is enabled, and the Max and Min data is applied to the opposite busses to memory.

Acquisition mode is controlled in part by the Microprocessor via data latched into the Acquisition Mode Register (see also, "Time Base Mode Register" in this section). These data bits select the channel or channels to be acquired, enable the XY mode, enable MIN/MAX acquisition, control the Swap function for reordering data, and select the Test function for diagnostics. Acquisition clock signals generated by the Acquisition Clock Decoder transfer the data from stage to stage in the digital acquisition circuitry in a pipe-line fashion.

A Diagnostics Code Generator is included as a troubleshooting aid. When in the Test mode, the A/D Buffer is disabled, and the Code Generator places its counter-output bytes on the input bus to the Max and Min Registers.

Acquisition Memory

The Acquisition Memory is composed of two, 2-K by 8-bit random-access memory devices. One memory stores the Odd data bytes and the other stores the Even data bytes. The Odd and Even data can be swapped between the Swap Registers and the Acquisition Memory.

A programmable address counter is loaded with the number that is the amount of pretrigger data bytes needed to fill the pretrigger portion of the waveform acquisition. The PREFULL signal is sent to the Trigger Mux circuitry when the pretrigger count is full. That signal enables the Trigger Mux circuitry to accept a trigger signal. The remaining output bits from the Address Counter select the storage location for waveform data storage in the Acquisition Memory.

When waveform data is to be read out of the Acquisition Memory, the Address Counter is loaded with the address of the data for the waveform. The Microprocessor sequences through the addresses reading out the data bytes. Data transceivers allow data to be read from the memory to the bus or written from the bus to the memory.

Memory Address Registers place the address count on the bus along with bits that indicate the trigger status (TRIGD), the B trigger status (BTRIGD), the end-of-record status (ENDREC), and the byte-interrupt status (BYTEINT). These accompanying bits are used in establishing display attributes.

Memory writes, memory reads, and address counter load enabling and clocking are controlled by a quad, two-line-to-one-line multiplexer (Memory Control). Read and write signals from the Microprocessor control bus and write clocks are used to transfer the waveform data between the devices.

Digital Time Base

An accurate frequency source for synchronizing the Microprocessor with the other digital devices on the bus is provided by a 40 MHz oscillator. That frequency is divided

down by the Clock Generator to produce the various clocking rates. The Time Base Mode Register latches control data bits from the Microprocessor data bus to set the operating mode of the time base. These control bits switch the Trigger Mux circuit to either A or B Trigger, enable the trigger logic circuit, switch the clock multiplexer to change the clocking rate, start a storage acquisition, and enable interrupts to the Microprocessor. The programmable Time Base Divider, under control of the Microprocessor via the Time Base Divider Register, generates a sampling rate that corresponds to the front-panel SEC/DIV switch setting.

A Clock multiplexer at the end of the Time Base Divider chain selects the output of the Time Base Divider, the $\overline{\text{WRITECLK}}$, the $\overline{\text{CONV}}$ clock, or an external clock signal to generate the SAVECLK signal.

The Digital Time Base Trigger Logic circuit looks at whether the pretrigger data portion of the record has been filled. If the pretrigger portion is full, then the A or B Gate generates the trigger. When a trigger is generated in Repetitive Storage mode, the Clock Delay Timer measures the time delay between the arrival of the trigger and the convert clock. The time difference value is used by the Microprocessor to accurately position the acquired data with respect to the actual trigger point.

The delay difference between the start of the acquisition and the occurrence of the B trigger is also measured. This value is only used in BOTH HORIZONTAL MODE when running the B Horizontal display in Triggerable After Delay to provide a readout of the time delay between the A Trigger and the B Trigger points.

Acquisitions are counted to determine when a full record of data has been stored (ENDREC) and to keep track of the beginning and ending memory locations of the record. The Record Counter is also programmable to provide for the different record lengths for one-channel or two-channel acquisitions, different Pretrigger selections, and either 4K-byte or 1K-byte record length.

Digital Display

A custom IC handles the digital display generation. The Display Controller functions as an interface between the processor bus, display memory (RAM), and vector generators to form waveform and character displays on the crt. The controller reads a display list from the Display Memory and drives X- and Y-Vector Generators to create the waveform and readout displays. Z-Axis control signals are also generated to drive the crt Z-Axis Amplifier for Stored waveform and Readout intensity control. Control signals to the Microprocessor and Display Memory are generated in response to a processor read/write request.

Digital-to-analog converters take the digital data bytes supplied from the Display Memory via the Display Controller and change them to the X- and Y-Axis analog signals that drive the Horizontal and Vertical Vector Generators. The vector signals are applied to the Horizontal and Vertical Output Amplifiers to produce the STORE mode deflection signals and NON STORE mode character readout.

The Display Memory is six 16-K X 4-bit dynamic random access memories (RAM). Four of the RAMs provide the 8-bit data bytes of the stored waveform, and the remaining RAMs store each data-byte's intensity and Status attributes. A 4-bit word in each RAM is selected by latching a row address followed by a column address. Data is either stored or read out (as the operation in progress requires).

Vector Generator

X- and Y-Axis analog signals from the Digital Display are converted by the Vector Generators into the vector signals used to drive the crt deflection plates. Vector signals are produced for the stored waveforms, the menu displays, and the readouts. The Vector Generator is switched to the dot-display mode for equivalent-time sampling waveforms and X-Y displays.

The X-Y Plotter driver circuit is included in this portion of the circuitry. When the X-Y Plotter is enabled, x-axis and y-axis signals are switched via the plot multiplexer to the x-axis and y-axis plot amplifiers. The $\overline{\text{VECT SMPL}}$ signal is switched via the same multiplexer to drive the Pen-Down amplifier.

Z-Axis

The Z-Axis Amplifier has input signals from multiple sources that control the crt intensity on a time-shared basis. Nonstore intensity signals are the level inputs from the A and B INTENSITY controls that are controlled by the Alternate Display switching and B Z-Axis Logic circuits. Additional Z-Axis drive current is supplied during the intensified portion of an A trace during the B Sweep when BOTH Horizontal display mode is selected. The remaining nonstore signals that have control of the display brightness are the EXT Z-AXIS INPUT signal, the CHOP mode blanking signal, and the $\overline{\text{XY}}$ control signal. All of these sources are added to provide the time-shared nonstore displays.

For the Store waveform and the Menu and Readout character displays, an additional Z-Axis drive signal from the STORAGE/READOUT INTENSITY control is switched on and off by the Display Controller. The controller signals determine when the stored waveforms and the readout

button is pressed in; the READY LED is turned on when the filling is completed. The storage acquisition system is then ready to accept a triggering event. The READY LED is turned off after an acquisition is completed.

(29) **A TRIGGER LEVEL Control**—Selects the amplitude point on the A Trigger signal that produces triggering. The trigger point for STORE mode is identified by a T on the acquired waveform.

(30) **HF REJECT Switch**—Rejects (attenuates) the high-frequency components (above 40 kHz) of the trigger signal when the control is in the ON posiltion.

(31) **A TRIGGER SLOPE Switch**—Selects either the positive or negative slope of the trigger signal to start the NON STORE A Sweep or to reference the next STORE mode acquisition cycle.

(32) **A&B INT Switch**—Determines the source of the internal trigger signal for both the A and the B Trigger Generator circuits.

CH 1—Trigger signal is obtained from the CH 1 input.

VERT MODE—Trigger signal is obtained alternately from the CH 1 and CH 2 input signals if the VERTICAL MODE is ALT. In the CHOP VERTICAL MODE, the trigger signal is the sum of the CH 1 and CH 2 input signals.

CH 2—Trigger signal is obtained from the CH 2 input. The CH 2 INVERT switch also inverts the polarity of the internal CH 2 trigger signal so the displayed slope agrees with the Trigger SLOPE switch.

(33) **A SOURCE Switch**—Determines if the SOURCE of the A Trigger signal is internal, external, or from line.

INT—Routes the internal trigger signal selected by the A&B INT switch to the A Trigger circuit.

LINE—Routes a sample of the ac power source to the A Trigger circuit.

EXT—Routes the signal applied to the EXT INPUT connector to the A Trigger circuit.

(34) **A EXT COUPLING Switch**—Determines the method of coupling the signal applied to the EXT INPUT connector to the input of the A Trigger circuit.

AC—Input signal is capacitively coupled, and the dc component is blocked.

DC—All frequency components of the external signal are coupled to the A Trigger circuit.

DC÷10—Attenuates the external signal by a factor of 10 before application to the A Trigger circuit. As with DC COUPLING, all frequency components of the input signal are passed.

(35) **EXT INPUT Connector**—Provides for connection of external signals to the A Trigger circuit.

(36) **B TRIGGER (INT SOURCE ONLY) SLOPE Switch**—Selects either the positive or the negative slope of the B Trigger signal that starts the NON STORE sweep or completes the STORE acquisition.

(37) **B TRIGGER LEVEL Control**—Selects the amplitude point on the B Trigger signal where triggering occurs in Triggerable After Delay mode. The B Trigger point is displayed as a T on the STORE mode waveform display when in B Horizontal mode. The fully clockwise position of the B TRIGGER LEVEL Control selects the Runs After Delay mode of operation for the B Trigger circuitry. Out of the cw position, B Sweep is triggerable after the delay time.

(38) **VAR HOLDOFF Control**—Adjusts the NON STORE Variable Holdoff time over a 10 to 1 range. NON STORE Variable Holdoff starts at the end of the A Sweep. STORE mode Holdoff starts at the end of the acquisition cycle, and ends after the waveform data has been transferred from the acquisition to the display memory and the pretrigger portion of the acquisition memory has been filled. After STORE mode Holdoff ends, the next acquisition can be triggered after the next (or current, if one is in progress) NON STORE Variable Holdoff ends. STORE mode Holdoff may be many times the length of the A Sweep time so that several NON STORE Holdoffs may occur during STORE Holdoff time. This ensures that STORE mode triggering is controllable by the VAR HOLDOFF control and will be stable if the NON STORE display is stable.

STORAGE CONTROLS

See Figure 2-8 for the location of items 38 through 42.

(39) **STORE/NON STORE Switch**—Selects either the NON STORE or the STORE waveforms for display. The STORE acquisition system is turned off while NON STORE is selected, keeping the last-acquired STORE waveform in memory. Selects NON STORE when out and STORE when pressed in.

(40) **ACQUISITION Controls**—Determine the method of acquiring and displaying the acquired STORE waveform.

1K/4K Switch (Record Length)—Selects an acquisition record length of either one screen (1K) or four screens (4K). Pressing the button in selects 1K record length, and pressing it again to release it returns to 4K record length acquisitions. In either case, the displayed waveform has 100 data points per horizontal graticule division (50 if two channels are acquired).

When a waveform is acquired using the B time base, switching between record lengths also changes the delay time position setting by the same factor of four. The B DELAY TIME POSITION control must be repositioned to obtain the same delay.

When the 4K record length is selected, a one-screen (1K) window of the acquisition is displayed, and a bar graph is used to indicate the position of the displayed window within the record. Turn the CURSORS Position control to move the display window to any position within the record.

The 4K acquisition record can be compressed to a length of 1K by rotating the Variable SEC/DIV control out of the CAL detent position. The SEC/DIV readout is adjusted to reflect the correct time per division of the displayed waveform. The acquisition record may be magnified using the X10 Magnifier.

PRETRIG/POST TRIG Switch—Positions the trigger point for acquisitions either near the end (PRETRIG) or the beginning (POST TRIG) of the waveform. A T is displayed on the waveform to indicate the trigger point. Pressing the button in sets the trigger point to PRETRIG; out is the POST TRIG position.

ROLL/SCAN Switch—Selects either ROLL or SCAN acquisition and display mode. When pressed in (ROLL mode), at SEC/DIV switch settings from 0.1 s per division to 5 s per division the triggers are disabled for NORM and P-P AUTO Trigger modes, and the signals are continuously acquired and displayed. The waveform display scrolls from right to left across the crt with the latest samples appearing at the right edge of the crt. At SEC/DIV switch settings from 0.1 s per division to 5 s per division in SGL SWP Trigger mode, SCAN/ROLL/SCAN storage mode is selected.

At SEC/DIV switch settings of 0.05 s per division and faster, the ROLL/SCAN switch is not functional, and waveform samples require a triggering event to complete the acquisition before the display is updated.

When the ROLL/SCAN switch is in the out position (SCAN mode), the A TRIGGER Mode controls are functional. For NORM Trigger mode, the pretrigger waveform is updated by the trigger and the post trigger scans from the trigger position to the right. For SGL SWP, SCAN mode is overridden by SCAN/ROLL/SCAN. Triggers are disabled in P-P AUTO and TV FIELD Trigger modes.

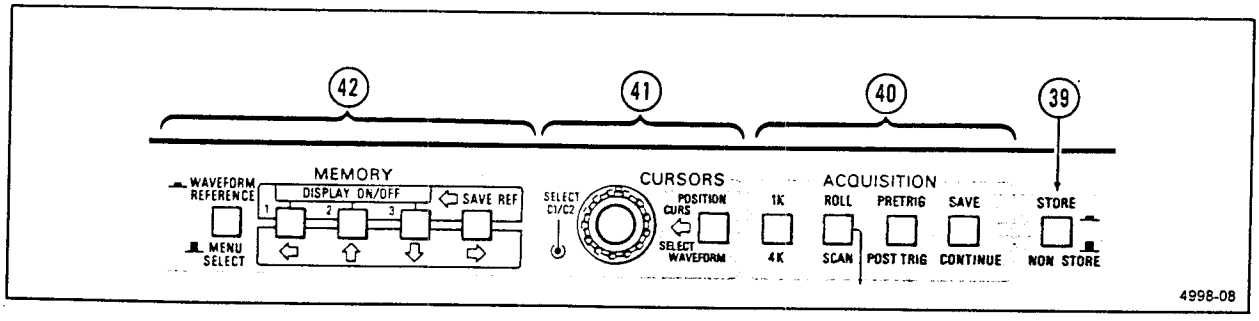


Figure 2-8. Storage controls.

SAVE/CONTINUE Switch—Stops the current acquisition and display update in progress when pressed in. Pressing the SAVE/CONTINUE switch a second time releases it and restarts (CONTINUE) the acquisition process. If the SEC/DIV switch setting is 0.1 s per division or slower, the SAVE state is entered immediately upon pressing the button. At SEC/DIV settings of 50 ms per division and faster, if an acquisition has been triggered, the acquisition is allowed to complete before the SAVE state is entered.

The pretrigger portion of an untriggered acquisition stops filling in SAVE mode. When leaving SAVE, a new acquisition is started, and a trigger is not accepted until the pretrigger portion again refills.

(41) **CURSORS Controls**—These controls apply to all displayed STORE mode waveforms. Delta Volts, Delta Time, One Over Delta Time, and Delay Time measurements of the STORE displays are made using the CURSORS controls. Positioning of the display window within a 4K acquisition record length is done using the CURSORS Position control. See the "Crt Readout" description for the cursor readout display.

POSITION CURS/SELECT WAVEFORM Switch—Determines the function of the CURSORS Position control. When pressed in (POSITION CURSORS mode), the CURSORS Position control functions as a cursor horizontal positioning control. When the push button is in the out position (SELECT WAVEFORM mode), the CURSORS Position control or the C1/C2 switch may be used to position the cursor to the desired waveform(s).

CURSORS Position Control—Provides for either horizontal positioning of the active cursor (or active cursors when there are two waveforms displayed in a display set) or for switching the cursors between waveform display sets. When cursors are positioned to a new waveform set, they return to the position that they had when they were last on that waveform set. Cursor positioning continues to function during SAVE mode, and measurements can be made on any displayed waveform. When an acquisition control is changed, the cursors return to the acquisition waveform set.

Cursors are placed on all waveforms in a display set. A display set is one or both waveforms from the following: Acquisition, CH 1 and CH 2; Reference 1, CH 1 and CH 2; Reference 2, CH 1 and CH 2; and Reference 3, CH 1 and CH 2. Cursors move to the acquisition waveform if they were on a SAVE REF waveform that is turned off. The acquisition parameters of the waveform set in which the cursors are located are displayed in the crt readout. Cursors movable by the CURSORS Position control are enclosed in a box.

When the displayable acquisition record length is greater than one screen, a one-screen window of the record is displayed. A bar graph indicates the position of the display window within the acquisition record. The position of the display window is adjusted to provide a display of the cursor position. If the displayed cursor is positioned to either edge of the display window, further positioning starts the waveform display scrolling in the opposite direction as the display-window position moves. Display-window positioning can be continued to the ends of the record, allowing observations and measurements to be made over the entire acquisition record.

SELECT C1/C2 (Cursor-Select) Switch—In Position CURS mode this switch selects the cursor(s) that can be positioned by the CURSORS Position control. Cursors are activated alternately with each press of the C1/C2 button. Each selected cursor is enclosed in a box. In Select Waveform mode, pressing the C1/C2 switch moves the cursor set between displayed waveforms.

(42) **MEMORY and Menu Controls**—These switches control MENU operation while the MENU is displayed, and they control the storage and display of the SAVE Reference waveforms when the MENU is not displayed.

WAVEFORM REFERENCE/MENU SELECT Switch—Selects either the MENU or SAVE REF MEMORY displays. In Waveform Reference mode, the MEMORY switches control the Save Reference Memory. In MENU mode, the MEMORY switches control the Menu, allowing selection of alternate parameters and modes that override the default front-panel settings.

SAVE REF MEMORY CONTROL—When the WAVEFORM REFERENCE/MENU SELECT switch is in the WAVEFORM REFERENCE position (button in), the MEMORY switches control the Save Reference Memory.

SAVE REF/→ Switch—Pressing this button just prior to pressing one of the DISPLAY ON/OFF buttons writes the displayed acquisition waveform into the selected Save

Reference memory. The written waveform remains displayed on the crt. A control change or a delay of five seconds between pressing the SAVE REF button and selecting a memory location cancels the SAVE request.

In 4K acquisition mode, a choice may be made to save the entire 4K acquisition or the 1K display window. To save a 4K acquisition, press SAVE REF, then press DISPLAY ON/OFF 1 twice. The 4K record fills MEMORY 1, 2, and 3. To save only the 1K displayed window, press SAVE REF, then press DISPLAY ON/OFF 1, then DISPLAY ON/OFF 2. The 1K display window may also be saved in MEMORY 2 or 3 by pressing SAVE REF, then the desired DISPLAY ON/OFF button.

Menu Select/DISPLAY ON/OFF Switches—These buttons select one of three memories that is either written to for saving a 1K acquisition waveform (if SAVE REF has been pressed) or toggles the reference memory display on or off (if the SAVE button has not been pressed). The stored waveforms of all three memories can be displayed at the same time. Two channels acquired in CHOP or ALT may be stored in a SAVE REF memory.

MENU CONTROL—When the WAVEFORM REFERENCE/MENU SELECT switch is in the MENU SELECT position (button out), the MEMORY switches control Menu Operation. Waveforms are only displayed with menus when a menu choice requires a waveform be displayed in order to perform the selected change. The Menu allows selection of alternate parameters and modes that override the default front-panel settings.

SAVE REF/→ Switch—When pressed, the next (to the right) Menu level is entered.

Menu Select/DISPLAY ON/OFF Switches—These three buttons select choices presented in the MENU. The ← button recalls the previous (to the left, higher) Menu level. The ↑ button selects the previous entry in the **current** Menu level. The ↓ button selects the next entry in the current Menu level.

MENU SELECTED FUNCTIONS

This part describes the Menu selected functions that provide selection of parameters, settings, and features not controlled by the front-panel switches.

ACQ MODE SETUP TABLE

ACQ MODE SETUP TABLE controls the acquisition mode setup using a table.

SELECT MODE—Displays the acquisition modes in a table. The desired modes for each sweep speed may be selected using the SEC/DIV switch to select the column, the CURSORS Position control selects the row, and the SELECT C1/C2 switch toggles the choice for the table position that is enclosed in a box.

SWP LIMIT—Selects the number of acquisitions before the acquisition system halts. SWP LIMIT may be reset by changing any control that affects acquisition parameters.

WEIGHT—Selects the weight of the last sample in AVERAGE mode.

A TRIG POS

A TRIG POS selects the number of points acquired prior to or following the trigger.

DISPLAY

DISPLAY controls the selection of display parameters.

DELTA T MODE—Selects either DELTA TIME or ONE OVER DELTA TIME for display in the readout.

VECTORS ON/OFF—Selects either DOTS or VECTORS as the waveform display mode. Vectors are not allowed in REPETITIVE mode.

SMOOTH ON/OFF—Selects the process with which the vector displays are produced when in PEAKDET or ACCPEAK.

With SMOOTH OFF, no reordering of the data points is done, and vectors are drawn between all of the minimum and maximum data points.

With SMOOTH ON, data points are reordered for correct slope and interpolated for drawing a smooth waveform. Smoothing looks at the change in value of

reordered data points between adjacent sample intervals. If the change in value does not exceed certain limits, the values are interpreted as a continuous slope for drawing either vectors or dots. If the value change exceeds the interpreted "no-change" limit, the data point value is not modified, and the vectors drawn in the display show a discontinuity in the waveform. This method of display of the waveform data provides a smoothed display of the waveform, yet retains the glitch-catching capabilities of PEAKDET or ACCPEAK modes.

DEFAULT

Selects the default acquisition modes for all sweep speeds (see Table 2-2 for the default modes).

FORMATTING

FORMATTING selects a SAVE REF memory for formatting. The vertical gain, horizontal gain, and vertical position of the selected reference waveform may be changed. The acquisition mode used to store the waveform may also be displayed.

TARGET REFERENCE—Selects one of the SAVE REF memories for formatting.

VGAIN—Allows adjustment of the vertical gain of SAVE REF memories.

VPOSITION—Allows adjustment of the vertical position of SAVE REF memories.

HMAG—Turns X10 horizontal magnification of SAVE REF memories on or off.

MODE—Displays the parameters used to acquire a SAVE REF memory.

PLOT

PLOT controls the transmission of waveforms over the X-Y Plotter output.

START—Initiates the transmission of a waveform over the X-Y Plotter output.

GRATICULE ON/OFF—Enables or disables plotting of the graticule.

SET UP—Allows calibration of analog plotter gain and offset.

SPEED—Allows selection of plotter pen speed.

ADVANCED FUNCTIONS

REFERENCE—Allows a SAVE REF memory to be Erased or Copied when one of the communication options is installed.

ERASE—Selects and erases a nonvolatile SAVE REF memory.

COPY—Selects and copies one nonvolatile SAVE REF memory to another SAVE REF memory.

COMM—Allows the selection of parameters for optional communications options, when they are present.

ACQ MODE SETUP TREE—Controls the acquisition mode setup using a tree. This provides control of the same functions as the ACQ MOD SETUP TABLE.

DEFAULT—Selects the default acquisition modes for all sweep speeds (see Table 2-2 for the default modes).

REPETITIVE—Selects the acquisition modes for sweep speeds from 0.05 μs to 2 μs per division.

FAST RECORD—Selects the acquisition modes for sweep speeds from 5 μs to 10 μs per division.

SLOW RECORD—Selects the acquisition modes for sweep speeds from 20 μs to 50 ms per division.

SLOW TRIGGERED—Selects the triggered acquisition modes for sweep speeds from 0.1 to 5 s per division or EXT CLOCK.

SLOW UNTRIGGERED—Selects the untriggered acquisition modes for sweep speeds from 0.1 to 5 s per division or EXT CLOCK.

DIAGNOSTICS—Controls the selection of diagnostic TESTS, EXERCISERS, and PICTURES.

Acquisition Modes

PEAK DETECT (PEAKDET) and SAMPLE—Select how samples are processed on successive acquisitions. See Table 2-2 for the default modes set by the SEC/DIV switch.

In Peak Detect mode, the minimum and maximum levels of the input signal within the time represented by 1/50 of a division unmagnified (1/25 of a division in CHOP or ALT) are digitized and stored in acquisition memory as a data pair. The displayed data points are connected by vectors.

In Sample mode, the signal is sampled at a rate that produces 100 samples per graticule division. In RECORD sampling, the displayed sample points are connected by either vectors or dots. For REPETITIVE Storage mode, the sample points are displayed as dots.

ACCPEAK—Will cause displays to accumulate. The largest maximum and smallest minimum sample acquisitions are retained for each trigger-referenced sample record over multiple acquisition cycles. When ACCPEAK is used with hardware peak detection (50 μs per division to 0.1 s per division), updating of maximum and minimum samples also occurs within each time-base clock period. Changing any switch that affects the acquisition parameters resets ACCPEAK displays. ACCPEAK mode is valid for triggered acquisitions only and is not operational in any mode that does not allow triggers (see Table 2-2).

AVERAGE—Is used for multiple record averaging. Whenever AVERAGE is selected, SAMPLING is also selected automatically. When on, a normalized algorithm is used for continuous display of the signal at full amplitude during the averaging process. Averaging is the default for REPETITIVE Store mode only. The amplitude resolution increases with the number of weighted acquisitions included in the display. The number of weighted acquisitions included in the AVERAGE display is Menu selectable. The default weight of AVERAGE mode is 1/4. Other choices are Menu selectable. The number of sweeps (SWP LIMIT) allowed to occur before averaging stops is also Menu selectable.

REAR PANEL

Refer to Figure 2-9 for location of items 43 through 45.

(43) **EXT Z-AXIS Input Connector**—Provides an input connector allowing external signals to be applied to the Z-Axis circuit to intensity modulate the NON STORE waveform display. Applied signals do not affect the display waveshape. External signals with fast rise and fall times provide the best defined intensity modulation. Noticeable intensity modulation is produced at normal viewing intensity levels by a 5 V p-p signal. The Z-Axis signals must be time-related to the trigger signal to obtain a stable intensity-modulation pattern on the displayed waveform.

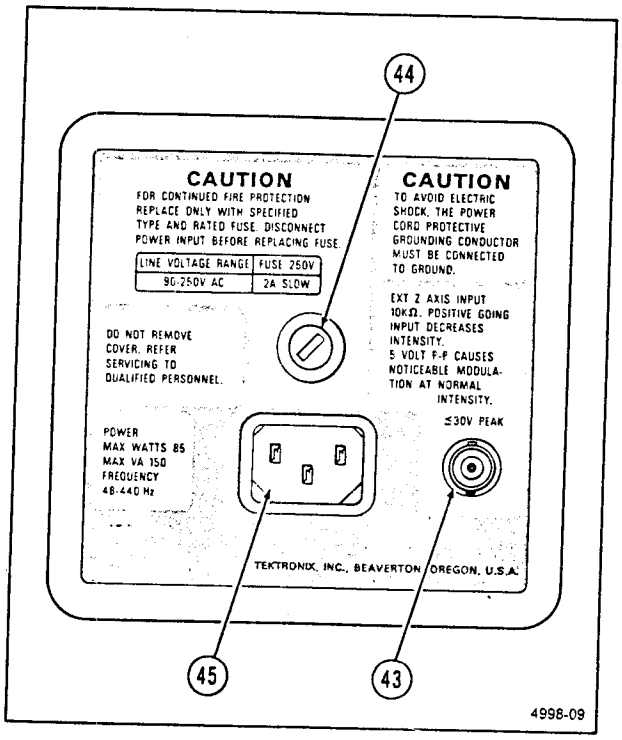


Figure 2-9. Rear Panel.

(44) **Fuse Holder**—Contains the ac-power-source fuse. See the rear panel nomenclature for fuse rating and line voltage range.

(45) **Detachable Power Cord Receptacle**—Provides the connection point for the ac-power source to the instrument.

SIDE PANEL

The standard side panel includes one AUXILIARY CONNECTOR. Refer to Figure 2-10 for the location of item 46.

(46) **AUXILIARY CONNECTOR**—Provides connections for an X-Y Plotter and an External Clock input (see Table 2-4).

NOTE

To meet EMI regulations and specifications, use the specified shielded cable and metal connector housing with the housing grounded to the cable shield for connections to the AUXILIARY CONNECTOR.

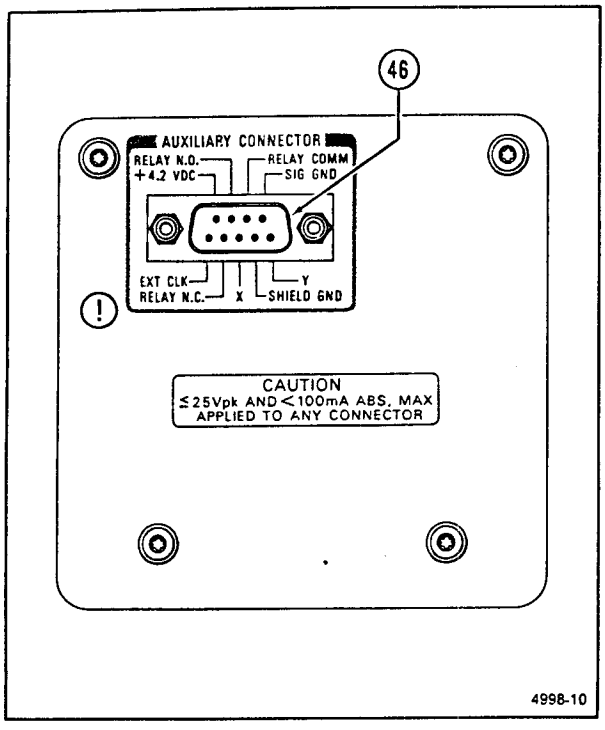


Figure 2-10. Side Panel.

X-Y Plotter Connections—Provide connections for X-Axis output, Y-Axis output, and Pen Lift control to drive an external X-Y Plotter. All displayed waveforms and the crt readout are transmitted over the Plotter Interface. The settling time allowed for each movement is approximately proportional to the distance of the movement. Connections for Signal Ground and Shield Ground are also provided for grounding between the instrument and the external X-Y Plotter. Waveforms and the Readout are plotted on the crt while a plot is in progress.

To be fully compatible, the X-Y Plotter used must have X and Y inputs with sensitivity control and penlift control.

Signals available at the AUXILIARY CONNECTOR allow the Pen Lift circuit to be wired for a plotter with either active HI or active LO drive requirements and several logic families. Examples for both an active HI and an active LO TTL drive are shown in Figure 2-11.

EXT CLK Input—Provides an input for EXT CLOCK signals (up to 1000 samples per second) to the storage acquisition circuitry in conjunction with the EXT CLK position of the A SEC/DIV switch. Samples are referenced by falling edges. Input is TTL compatible. Samples become visible by pairs, as SCAN or ROLL. Several clocks are required before the point associated with the first clock is visible.

Table 2-4

Auxiliary Connector

Pin Number	Function
1	EXT CLK Input
2	Pen Lift, Normally Closed
3	X Output
4	SHIELD GND
5	Y Output
6	+4.2 V
7	Pen Lift, Normally Open
8	Pen Lift, Relay Common
9	SIG GND

CRT READOUT

The Readout System provides an alphanumeric display of information on the crt along with the waveform displays. The readout (non MENU) is displayed in three rows of characters. Two rows are within the top graticule division, and the other row is within the bottom graticule division. The locations and types of information displayed under normal operating modes are illustrated in Figure 2-12.

NON STORE Mode

In NON STORE mode the current settings of the VOLTS/DIV and SEC/DIV switches are displayed. Greater-than symbols (>) are used to indicate uncalibrated VOLTS/DIV and SEC/DIV switch settings. A down-arrow symbol (↓) is used in front of the CH 2 VOLTS/DIV readout to indicate CH 2 INVERT. For Horizontal Display Mode of BOTH and B only, the DELAY TIME POSITION readout is also displayed. The AC-GND-DC input coupling selection is indicated in the associated VOLTS/DIV readout with a tilde symbol (~) above the volts symbol for AC, a ground symbol (⏚) for GND, and no extra symbol for DC input coupling.

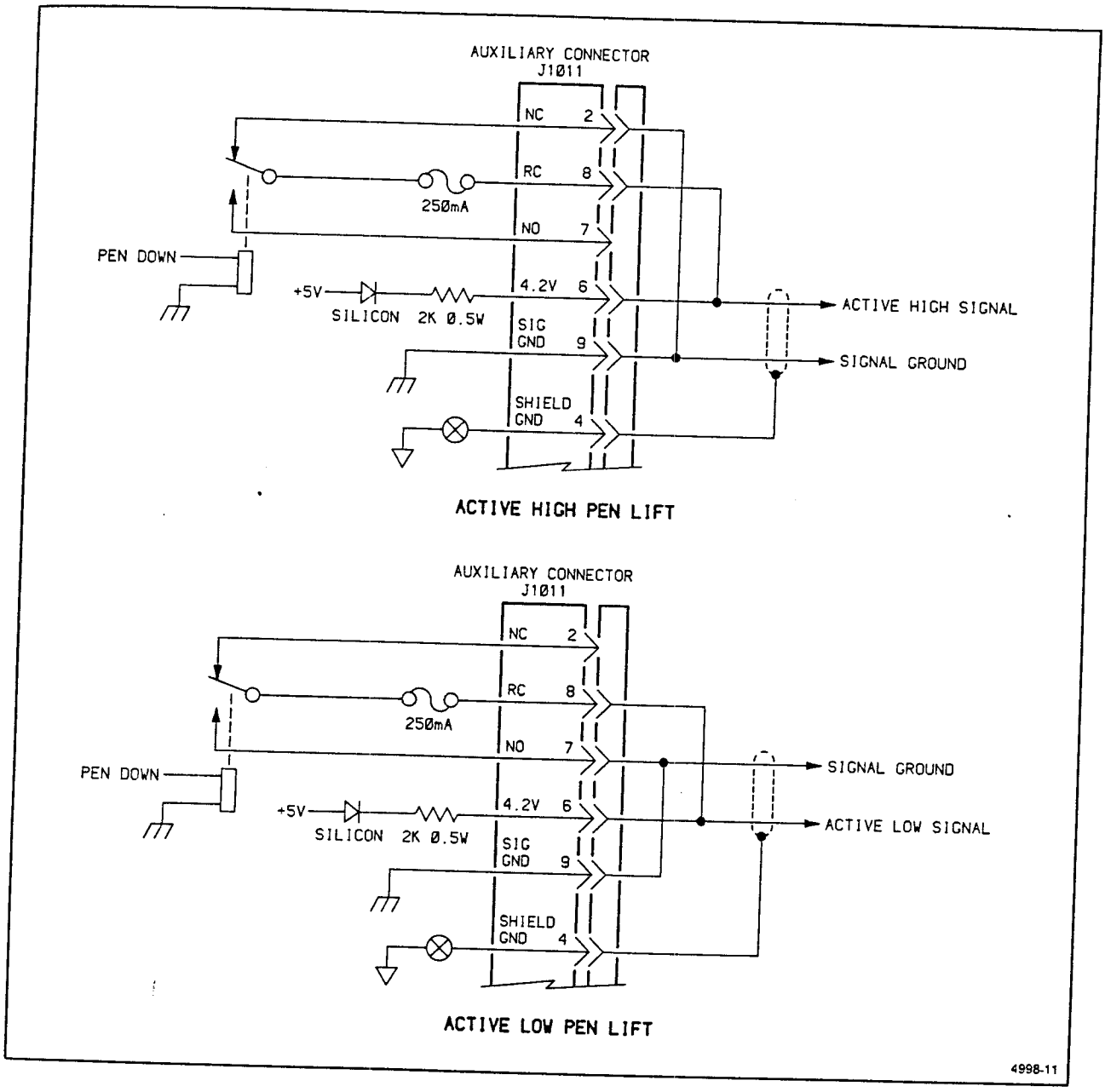


Figure 2-11. X-Y Plotter interfacing.

STORE Mode

In STORE mode, many of the crt readout displays are associated with the parameters of stored waveforms.

PARAMETER READOUT. Displays the VOLTS/DIV, SEC/DIV and B DELAY TIME settings of the displayed waveforms on which the cursors are placed. The AC-GND-DC input coupling selection is indicated in the associated VOLTS/DIV readout with a tilde symbol (~) above the volts symbol for AC, a ground symbol (⏚) for GND, and no extra symbol for DC input coupling. If the VOLTS/DIV switch is switched beyond the available expansion or compression range, the readout is tilted, indicating that the VOLTS/DIV switch setting and the VOLTS/DIV readout no longer agree. In 4K COMPRESS, a **c** is displayed in front of the SEC/DIV readout.

CURSOR READOUT. Displays the voltage difference (either ΔV 1 or ΔV 2) and the time difference between cursors. When either BOTH or B HORIZONTAL mode is selected, the DELAY TIME POSITION is displayed. Independent fields for CH 1 VOLTS/DIV, CH 2 VOLTS/DIV, A SEC/DIV, and B SEC/DIV are provided. When making ground referenced voltage measurements (ground dot displayed and cursor on ground dot) the Δ symbol is replaced by a ground symbol (⏚).

When the acquisition record length is longer than one screen, a bar graph is used to indicate the position of the display window within the acquisition record.

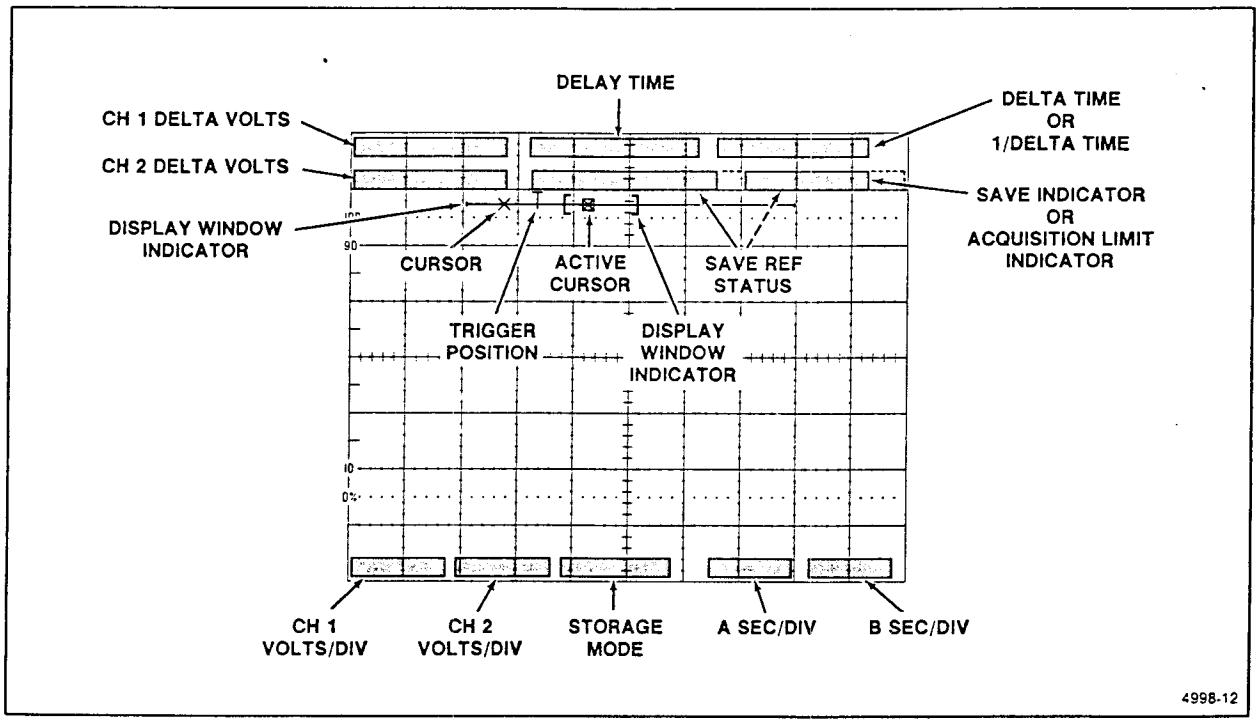


Figure 2-12. Crt readout display.

OPERATING CONSIDERATIONS

This part contains basic operating information and techniques that should be considered before attempting to make any measurements with the instrument.

GRATICULE

The graticule is internally marked on the faceplate of the crt to eliminate parallax-viewing errors and to enable measurements (see Figure 2-13). The graticule is marked with eight vertical and ten horizontal major divisions. In addition, each major division is divided into five subdivisions. The vertical deflection factors and horizontal timing are calibrated to the graticule so that accurate measurements can be made directly from the crt. Also, percentage marks for the measurement of rise and fall times are located on the left side of the graticule.

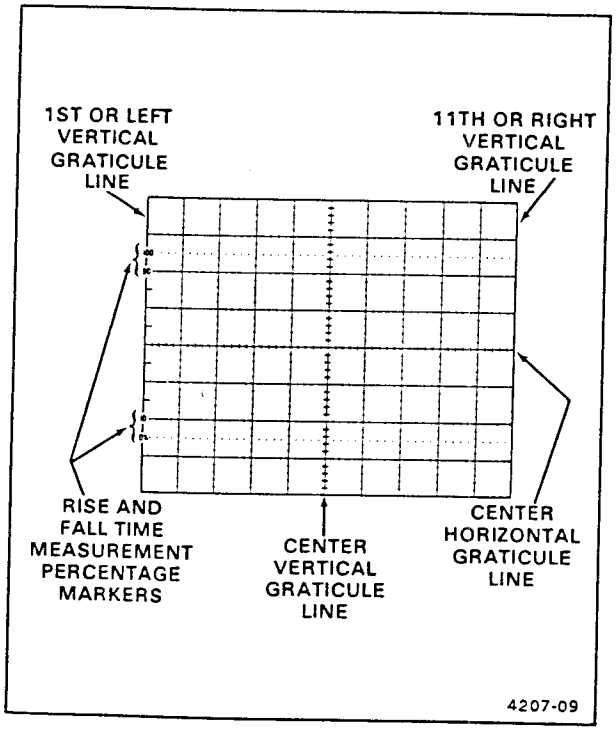


Figure 2-13. Graticule measurement markings.

GROUNDING

The most reliable signal measurements are made when the oscilloscope and the unit under test are connected by a common reference (ground lead) in addition to the signal lead or probe. The probe's ground lead provides the best grounding method for signal interconnection and ensures the maximum amount of signal-lead shielding in the probe cable. A separate ground lead can also be connected from the unit under test to the oscilloscope GND receptacle located on the oscilloscope's front panel.

SIGNAL CONNECTIONS

Probes

Generally, the accessory probes supplied with the instrument provide the most convenient means of connecting a signal to the vertical inputs of the instrument. The probe and probe lead are shielded to prevent pickup of electromagnetic interference, and the 10X attenuation factor of the probe offers a high input impedance that minimizes signal loading in the circuitry under test. The attenuation factor of the standard accessory probe is coded so that the VOLTS/DIV readout seen on the crt is automatically switched to the correct scale factor when the probe is attached.

Both the probe itself and the probe accessories should be handled carefully at all times to prevent damage to them. Avoid dropping the probe body. Striking a hard surface can cause damage to both the probe body and the probe tip. Exercise care to prevent the cable from being crushed or kinked. Do not place excessive strain on the cable by pulling.

The standard-accessory probe is a compensated 10X voltage divider. It is a resistive voltage divider for low frequencies and a capacitive voltage divider for high-frequency signal components. Inductance introduced by either a long signal or ground lead forms a series-resonant circuit. This circuit will affect system bandwidth and will ring if driven by a signal containing significant frequency

components at or near the circuit's resonant frequency. Oscillations (ringing) can then appear on the oscilloscope waveform display and distort the true signal waveshape. Always keep both the ground lead and the probe signal-input connections as short as possible to maintain the best waveform fidelity.

Misadjustment of probe compensation is a common source of measurement error. Due to variations in oscilloscope input characteristics, probe compensation should be checked and adjusted, if necessary, whenever the probe is moved from one oscilloscope to another or between channels. See the probe compensation procedure in "Operator's Check and Adjustments", or consult the instructions supplied with the probe.

Coaxial Cables

Cables may also be used to connect signals to the vertical input connectors, but they may have considerable effect on the accuracy of a displayed waveform. To maintain the original frequency characteristics of an applied signal, only high-quality, low-loss coaxial cables should be used. Coaxial cables should be terminated at both ends in their characteristic impedance. If this is not possible, use suitable impedance-matching devices.

INPUT-COUPLING CAPACITOR PRECHARGING

When the Input Coupling switch is set to the GND position, the input signal is connected to ground through the input-coupling capacitor and a high resistance value. This series combination forms a precharging circuit that allows the input-coupling capacitor to charge to the average dc voltage level of the signal applied to the input connector. Thus, any large voltage transients that may accidentally be generated are not applied to the vertical amplifier's input when the input coupling is switched from GND to AC. The precharging network also provides a measure of protection to the external circuitry by reducing the current level that is drawn from the external circuitry while the input-coupling capacitor is charging.

If AC input coupling is in use, the following procedure should be followed whenever the probe tip is connected to a signal source having a different dc level than that previously applied. This procedure becomes especially useful if the dc-level difference is more than ten times the VOLTS/DIV switch setting.

1. Set the AC-GND-DC (input coupling) switch to GND before connecting the probe tip to a signal source.

2. Touch the probe tip to the oscilloscope GND connector.

3. Wait several seconds for the input-coupling capacitor to discharge.

4. Connect the probe tip to the signal source.

5. Wait several seconds for the input-coupling capacitor to charge to the dc level of the signal source.

6. Set the AC-GND-DC switch to AC. A signal with a large dc component can now be vertically positioned within the graticule area, and the ac component of the signal can be measured in the normal manner.

OPERATOR'S CHECKS AND ADJUSTMENTS

To verify the operation and basic accuracy of your instrument before making measurements, perform the following checks and adjustment procedures. If adjustments are required beyond the scope of these operator's checks and adjustments, refer the instrument to qualified service personnel.

For new equipment checks, before proceeding with these instructions, refer to "Preparation for Use" in this manual to prepare the instrument for the initial start-up before applying power.

INITIAL SETUP

1. Verify that the POWER switch is OFF (switch is in the out position), then plug the power cord into the ac power outlet.

2. Press in the POWER switch (ON) and set the instrument controls to obtain a baseline trace:

Display

A and B INTENSITY	Midrange
STORAGE/READOUT INTENSITY	Midrange (with READOUT on)
FOCUS	Best defined display

Vertical (Both Channels)

VERTICAL MODE	CH 1
POSITION	Midrange
VOLTS/DIV	50 mV
AC-GND-DC	DC
Var Volts/Div	CAL (in detent)
BW LIMIT	Off (button out)

Horizontal

HORIZONTAL MODE	A
A SEC/DIV	0.5 ms
Var Sec/Div	CAL (in detent)
POSITION	Midrange
X10 Mag	Off (Var Sec/Div knob in)
B DELAY TIME POSITION	Fully counterclockwise

Triggers

VAR HOLDOFF	NORM (fully counterclockwise)
A&B INT	VERT MODE
A SOURCE	INT
A Mode	P-P AUTO
A LEVEL	For a stable display (with signal applied)
A SLOPE	OUT (plus—button out)
B LEVEL	B RUNS AFTER DELAY (fully clockwise)
B SLOPE	OUT (plus—button out)
HF REJECT	OFF (fully counterclockwise)

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/MENU SELECT	WAVEFORM REFERENCE (button in)

3. Adjust the INTENSITY and FOCUS controls for the desired display brightness and best focused trace.

4. Adjust the Vertical and Horizontal POSITION controls to position the trace within the graticule area.

5. Allow the instrument to warm up for 20 minutes before commencing the adjustment procedures. Reduce the INTENSITY levels during the waiting time.

TRACE ROTATION ADJUSTMENT

NOTE

Normally, the trace will be parallel to the center horizontal graticule line, and TRACE ROTATION adjustment is not required.

1. Preset the instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Use the Channel 1 POSITION control to move the baseline trace to the center horizontal graticule line.

3. If the baseline trace is not parallel to the center horizontal graticule line, use a small-bladed screwdriver or alignment tool to adjust the TRACE ROTATION control to align the trace with the graticule line.

PROBE COMPENSATION

Misadjustment of probe compensation is a source of measurement error. The attenuator probes are equipped with a compensation adjustment. To ensure optimum measurement accuracy, always check probe compensation before making measurements. Probe compensation is accomplished by:

1. Preset the instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Connect the two 10X probes (supplied with the instrument) to the CH 1 OR X and CH 2 OR Y input connectors. Observe that the CH 1 VOLTS/DIV readout changes from 5 mV to 50 mV when the 10X probe is attached to the CH 1 OR X input.

3. Remove the hook tip from the end of each probe.

NOTE

While the probe tip is in the PRB ADJ connector, use care not to to break off the probe tip.

4. Insert the Channel 1 probe tip into the PRB ADJ connector.

5. Use the CH 1 POSITION control to vertically center the display. If necessary, adjust the A TRIGGER LEVEL control to obtain a stable display on the plus (OUT) SLOPE.

6. Check the waveform display for overshoot and rounding (see Figure 2-14); if necessary, use a small-bladed screwdriver to adjust the probe compensation for a square front corner on the waveform.

7. Remove the Channel 1 probe tip from the PRB ADJ connector.

8. Insert the Channel 2 probe tip into the PRB ADJ connector.

9. Set the VERTICAL MODE to CH 2.

10. Set the A TRIGGER A&B INT switch to CH 2.

11. Use the CH 2 POSITION control to vertically center the display.

12. Check the waveform display for overshoot and rounding (see Figure 2-14); if necessary, use a small-bladed screwdriver to adjust the probe compensation for a square front corner on the waveform.

NOTE

Refer to the instruction manual supplied with the probe for more complete information on the probe and probe compensation.

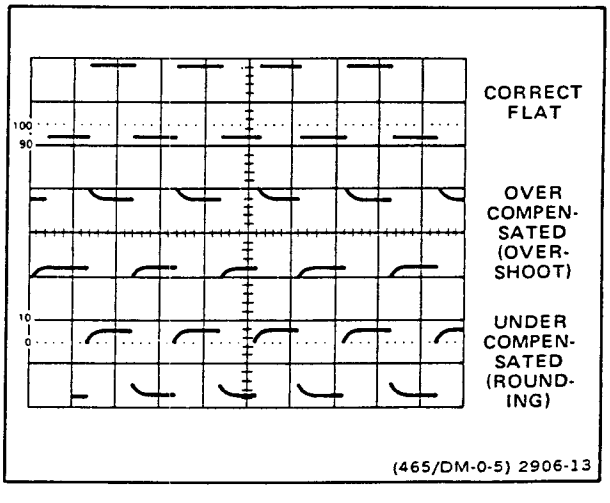


Figure 2-14. Probe compensation.

HORIZONTAL ACCURACY CHECK

A check of the horizontal timing can be made using the time measurement capability of the CURSOR measurement mode:

1. Preset instrument controls and obtain a baseline trace as described in "Initial Setup".

2. Set:

CH 1 AC-GND-DC	GND
STORE/NON STORE	STORE (button in)
A SEC/DIV	1 ms
PRETRIG/POST TRIG	POST TRIG (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)

3. Turn the Horizontal POSITION control to align the start of the trace to the first vertical graticule line.

4. Turn the Vertical POSITION control to align the baseline trace with the center horizontal graticule line.

5. Position the active cursor to the second vertical graticule line using the CURSORS Position control.

6. Push the SELECT C1/C2 switch to activate the other cursor.

7. Position the active cursor to the tenth vertical graticule line using the CURSORS Position control for a spacing of eight divisions between cursors.

8. Check that the Delta Time readout is $\geq$ 7.84 ms and $\leq$ 8.16 ms.

9. Verify that the CH 1 probe tip is in the PRB ADJ connector.

10. Set the CH 1 AC-GND-DC switch to DC.

11. Adjust the SEC/DIV switch setting for a display of at least one full period of the probe adjust signal (0.1 or 0.2 ms per division).

12. Use the Vertical and Horizontal POSITION controls to center the display.

13. Use the CURSORS Position control and the CURSORS SELECT C1/C2 button to align the cursors with the rising edges of the PRB ADJ signal (measurement is of the probe adjust signal period). Note the cursor time difference readout and the graticule measurement (horizontal distance between rising edges as taken from the graticule markings) of the signal for later reference.

14. Check that the cursor readout of the probe adjust signal period and the graticule measurement of the calibrator period are within ±2%.

15. Set the STORE/NON STORE switch to the NON STORE position (button out).

16. Determine the horizontal graticule measurement of the probe adjust signal period. Note the reading for later reference.

17. Check that the NON STORE Mode probe adjust signal period measurement obtained from the graticule markings is within ±3% of the STORE Mode probe adjust signal period obtained in step 13.

18. Set the X10 MAG switch to on (pull Var Sec/Div knob out) and set the A SEC/DIV switch setting to obtain a display of at least one full period of the probe adjust signal (0.1 or 0.2 ms per division).

19. Check that the magnified NON STORE Mode probe adjust sugnal period measurement obtained from the graticule markings is within ±4% of the STORE Mode probe adjust signal period obtained in step 13.

THEORY OF OPERATION

SECTION ORGANIZATION

This section contains a functional description of the 2230 Digital Storage Oscilloscope. The discussion begins with a summary of instrument functions. Following the general description, each major circuit is explained in detail. Functional block diagrams and schematic diagrams are used to show the interconnections between parts of the circuitry, to indicate circuit components, and to identify interrelationships with the front-panel controls.

Schematic diagrams and the overall block diagrams are located in the tabbed "Diagrams" section at the back of this manual. The schematic diagram associated with each description is identified in the text and indicated on the tab of the appropriate foldout page by a numbered diamond symbol. For best understanding of the circuit being described, refer to both the appropriate schematic diagram and the functional block diagram.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within the instrument. Functions and operation of the logic circuits are represented by logic symbology and terminology. Most logic functions are described using the positive-logic convention. Positive logic is a system where the more positive of two levels is the TRUE (or 1) state; the more negative level is the FALSE (or 0) state. In this logic description, the TRUE state is HI, and the FALSE state is LO. The specific voltages which constitute a HI or a LO state vary between specific devices. For specific device characteristics, refer to the manufacturer's data book.

Linear Devices

The operation of individual linear integrated circuit devices is described in this section using waveforms or graphic techniques to illustrate their circuit action.

GENERAL DESCRIPTION

Introduction

In the following overall functional description of the instrument, refer to the basic block diagram, Figure 3-1, and to the detailed block diagrams located in the "Diagrams" section of this manual. Each major block in the diagram represents a major circuit within the instrument. In Figure 3-1, the numbered diamond symbol in each block indicates the schematic diagram number. Much of the analog portion of the oscilloscope operates without direction from the Microprocessor circuitry. These portions of the instrument are described first, with appropriate references to areas that either provide information to the Microprocessor or are controlled by the instrument's storage circuitry. The Microprocessor and Storage circuit descriptions follow the more conventional portions of the instrument's circuitry.

Vertical

Signals to be displayed on the crt (cathode-ray tube) are applied to either or both the CH 1 OR X and the CH 2 OR Y input connectors. The signals may be coupled to the attenuator either directly (DC) or through an input-coupling capacitor (AC). The inputs may also be disconnected, and the input to the attenuators grounded, by switching to the GND position of the input coupling switch. In the GND position, the ac-coupling capacitor is allowed to precharge to the dc level present at the input connector. This precharging prevents large trace shifts of the display when switching from GND to AC coupling. The Attenuators are switched by the front-panel VOLTS/DIV switches and scale the applied signal level to obtain the desired display amplitude. Information about the Input Coupling switch and the channel VOLTS/DIV switch positions is read by the Microprocessor. These signals control the STORE mode ground-reference acquisition and the crt readout displays of the Input Coupling and VOLTS/DIV switch settings of the active channel(s).

Scaled output signals from the Attenuators are applied to the Vertical Preamplifiers for amplification. The Channel 2 Preamplifier has additional circuitry, permitting the operator to invert the Channel 2 display on the cathode-ray tube (crt). Trigger pickoffs in each channel supply a

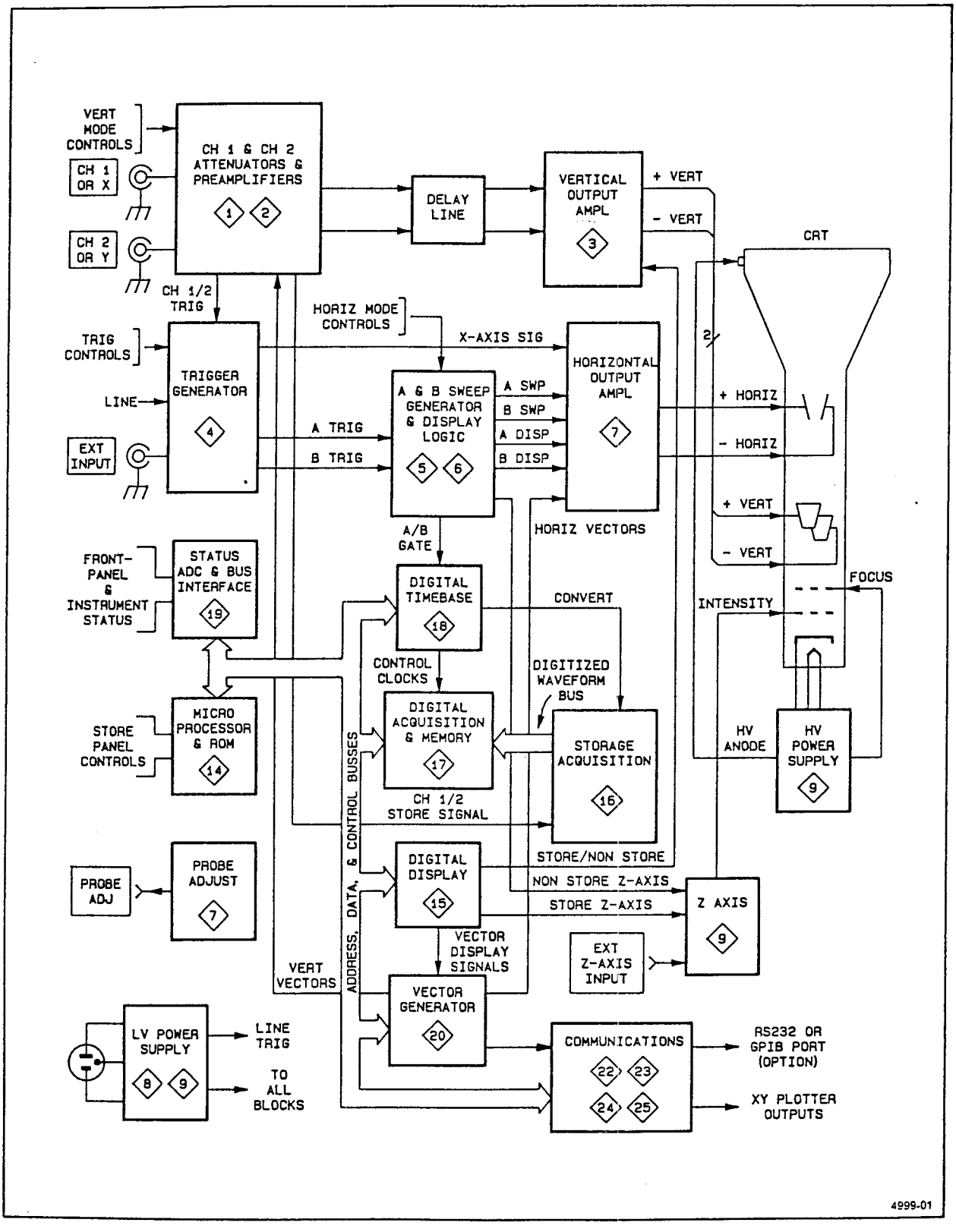


Figure 3-1. Simplified block diagram.

trigger signal to the Trigger Amplifier when internal triggering is selected. Other signal pickoffs provide vertical position information to the Position Signal Conditioning circuitry for vertically positioning the stored signal. The final stage of the Vertical Preamplifier for each channel provides one of two signals; either the vertical channel signal for the analog presentation on the crt or the vertical acquisition signal to be digitized by the storage circuitry.

Channel signals either for direct analog presentation on the crt or for application to the Storage digitizing circuitry are selected by the analog Channel Switch under control of the front-panel VERTICAL MODE switches. The switching signals from the Channel Switch Logic control a diode gate (Channel Switch) that selects the channel signal(s) to be applied to the Delay-line Driver. If ADD is selected, both channel signals are applied to the Delay-line Driver where the signals are summed together. The Delay-Line Driver provides the proper signal-driving level and impedance match to the Delay Line, where the vertical signal is delayed approximately 100 ns with respect to the trigger signal. The vertical signal delay allows time for the Horizontal circuitry to start the sweep before the vertical signal is applied to the crt.

Whenever STORE mode is selected, analog signals from the Storage circuitry are supplied to the Channel Switch circuit. Under control of the Channel Switch Logic, which is in turn switched by signals from the Display Controller, the analog display signal out of the final Vertical Preamplifier stage in each channel is biased off. The Channel 1 and Channel 2 Acquisition signals from the final preamplifiers are then biased on to pass the signals to be digitized to the Storage circuitry. At the same time, the Channel Switch (diode gate) is switched to pass the Storage vertical signal to the Delay Line Driver input.

Final amplification of the vertical signal (either STORE or NON STORE) is done by the Vertical Output Amplifier. This stage produces the signal levels that vertically deflect the crt electron beam. This amplifier stage also contains the vertical trace separation circuitry that separates the Nonstore A Intensified trace from the B Delayed trace when Alt Horizontal display mode is selected. The amount of trace separation is controlled using the front panel TRACE SEP knob. Another circuit feature in the Vertical Output Amplifier is the nonstore bandwidth limit (BW LIMIT) circuitry that follows the Delay Line. Either the full 100 MHz bandwidth or the limited 20 MHz bandwidth for the nonstore signal display may be selected. STORE mode signals are picked off in the Preamplifier and are not bandwidth limited by the BW LIMIT switch.

Triggering

The Triggering circuitry uses either the Internal Trigger signal obtained from the input signal(s), an External Trigger signal, or a Line Trigger signal derived from the ac-power-source to develop trigger signals for the Sweep Generator. The Auto Trigger circuit sets the range of the Trigger Level to conform approximately to the peak-to-peak amplitude of the selected trigger signal when either Auto or TV Field Trigger mode is selected. In Norm mode, the TRIGGER LEVEL control must be adjusted to the signal level before a sweep will be triggered. ROLL Storage (selectable at the slower sweep speeds in STORE mode) overrides the triggering circuit functions; a continuous signal acquisition is made and the signal displayed without the need of a trigger signal.

The triggering circuitry contains the TV Field Sync circuit. This circuit provides stable triggering on television vertical-sync pulses when in the TV Field triggering mode. TV Line triggering is possible using P-P AUTO trigger mode.

Signal pickoffs from the Internal Trigger circuitry provide the X-Axis signal for the nonstore X-Y display mode and the B trigger signal for triggered B Sweeps.

A Sweep

The A Sweep Generator and Logic circuits control the nonstore sweep generation and both the Store and the nonstore A Sweep timing. When the A TRIGGER mode switches are set to either P-P AUTO or TV FIELD and no trigger signal is present, the Auto Baseline circuit causes the Sweep Logic circuit to produce a sweep for reference purposes. In the NORM setting, the Auto Baseline circuit is disabled and nonstore sweeps are not generated until a trigger event occurs. NORM trigger mode is used to obtain stable triggering on low-repetition rate signals that do not provide a trigger before an auto baseline is generated. SGL SWP (single sweep) trigger mode allows only one sweep to be generated after being reset and is used to obtain the waveform from a one-shot event.

ROLL and SCAN Storage modes are useful in capturing low-frequency and low-repetition rate waveforms. In SCAN mode, receiving a trigger causes the pretrigger portion of the waveform to update as a block. The post-trigger waveform updates from the trigger point to the right edge of the screen as new data is acquired. ROLL Storage acquisitions differ from the Nonstore sweeps and SCAN Storage mode in that a trigger signal is not used for acquisition of the signal or displaying the waveform. The A Sweep Logic circuitry provides gating and holdoff signals used by the Storage circuitry to control its acquisition and display cycles for all storage modes, except ROLL.

The $\overline{\text{A Gate}}$ signal applied to the A Miller Sweep Generator circuit starts the Nonstore linear sweep with a ramp time that is controlled by the A SEC/DIV switch setting.

Switch position pickoffs supply the SEC/DIV switch setting information to the Microprocessor for use in STORE mode horizontal timing. The A SEC/DIV switch setting is also displayed on the crt for both Store and Nonstore operation.

B Sweep

The Alternate B Sweep Circuitry controls the Nonstore BOTH and B Delayed Horizontal mode displays. This circuitry includes the B Miller Sweep Generator and B Sweep Logic circuitry. STORE mode B timing is controlled by the B SEC/DIV switch. BOTH Horizontal mode is not available with STORE. In STORE mode, the BOTH selection displays an A Intensified Trace only. The intensified zone on the A trace indicates the position and approximate amount of the A trace that is displayed by the B Delayed Display.

Horizontal

Nonstore A and B Sweep signals (or the X-Axis signal from the X-Y Amplifier in the nonstore X-Y Display mode) are applied to the Horizontal Preamplifier where one is selected and amplified. Gain in the Preamplifier is switchable between X1 and X10. The X10 gain is used for Nonstore X10 Magnification. STORE mode X10 expansion is done digitally and reflected in the horizontal deflection signals supplied after the Horizontal Preamplifier. Horizontal positioning of both the Store and the nonstore display is done by applying a horizontal position dc offset to the Horizontal Preamplifier. The amplified nonstore horizontal signal is applied to the Horizontal Mux circuit where it is available for selection.

STORE mode horizontal deflection signals are also applied to the Horizontal Mux. Selection of either the nonstore sweep signals or the store deflection signals is done by control signals from the Channel Switch Logic in the Vertical circuitry. The selected horizontal deflection signals are then amplified by the Horizontal Output Amplifier to the levels needed to drive the crt's horizontal deflection plates.

Microprocessor

The Microprocessor (MPU) controls the digital storage and display sections of the oscilloscope. Under firmware control (firmware is the programmed instructions contained in read-only memory), the Microprocessor monitors the operation of the instrument and sets up the circuitry to perform as dictated by the front-panel control settings. Data transfer to and from the Microprocessor and address selection of a device to be communicated with are done over a 20-line I/O bus. The lower eight lines (AD0 through AD7) form a combined address/data bus while the remaining 12 lines (A8 through A19) are for addressing only. Timing for the execution of instructions, addressing, and data transfers is provided by an external, crystal-controlled oscillator that drives the Microprocessor clock generator. The Microprocessor clock circuit further divides the input clock frequency to generate two lower clock frequencies. The clock circuit also generates the Ready and Reset control signals to the Microprocessor.

Storage front-panel control settings are passed to the Microprocessor via eight-bit bus drivers. Settings of the analog front-panel controls and switches are also provided to the MPU, but via different bus drivers. The Status ADC and Bus Interface circuitry provides the interfaces from the analog front-panel controls to the data bus.

Status ADC and Bus Interface

Switch settings and status bits are applied directly to bus drivers. Each data bit then corresponds to a switch setting (either open or closed) or a status bit logic level (either HI or LO). Analog front-panel information is multiplexed to an analog-to-digital converter where it is converted to a digital value and applied to a bus driver. When the Microprocessor reads the bus, it obtains a data byte that represents the position value for a single control rather than the switch or status data bits of the digital-type information. The Microprocessor determines the control settings from the value of the data bytes or status bits received and sets up the digital storage circuits accordingly.

Storage Acquisition

Input signals to be digitized are selected by the Channel Switch. Either or both (for ADD) of the input signals picked off from the Vertical Preamplifier may be selected. The differential output signal from the Channel Switch is converted to a single-ended signal for application to the Sample-and-Hold amplifier. The input diode bridge in the Sample-and-Hold circuit is strobed to pass a sample of the signal to charge the hold capacitor. While the signal sample is held for conversion, the diode bridge is reverse biased, and the charge on the Hold capacitor remains at a fixed level. The sample buffer amplifier applies the voltage level on the Hold capacitor to the Analog-to-Digital Converter stage for conversion to an eight-bit digital signal. The output signals are then shifted from the emitter-coupled logic (ECL) level obtained from the ADC to the transistor-transistor-logic level (TTL) and passed to the digitized signal bus for transfer to the Acquisition Memory.

Digital Acquisition

Digitized waveforms are transferred from the ECL-to-TTL level shifters via the digitized data bus to the A/D Buffer of the Acquisition Memory circuit. The buffered data is applied to two identical registers; the Min Register and the Max Register. Data is alternately clocked into the registers by the MINCLK and MAXCLK clock signals. The

actual clocking that occurs depends on the sampling mode (Min/Max, Sampling, or X-Y). The same waveform data is also applied to opposite comparator inputs of two eight-bit magnitude comparators. Output data from the Min and Max Registers is applied to the other comparator's input pins, with the Min Register data going to the Min Comparator and the Max Register data going to the Max Comparator.

In Min/Max mode, the first data byte taken in a sample window (set by the SEC/DIV switch setting) is clocked into both registers. That data byte is then compared with the next data sample or samples (determined by the sample window) being applied to the inputs of the Min and Max Registers. If the data byte is either smaller in magnitude than the last clocked minimum or greater in magnitude than the last clocked maximum, a NEWMIN or a NEWMAX signal is generated. The signal is routed through the Min/Max Clock Selector back to the clock input of the Min or Max Register (Min if it is a new minimum amplitude or Max if it is a new Maximum amplitude) and the new signal is clocked into the register. At the end of a Min/Max sample window, the data present at the output of the Min and Max Registers is clocked into the Swap Registers to be transferred to the Acquisition Memory.

When record sampling mode is selected, each waveform sample is successively clocked into the Min and Max Registers on alternate ODDCLK and $\overline{\text{ODDCLK}}$ signals. When X-Y mode is selected, the Channel 1 and Channel 2 waveforms are sampled in a chopped manner, with samples of the two channel signals being taken with less time between the samples than in normal record sampling mode. Channel 1 data is clocked into the Min Register, and Channel 2 data is clocked into the Max Register.

Four eight-bit Swap Registers are used to reorder the Max and Min data obtained from each sample window. The Max Register data is clocked into two of the registers in parallel, and the Min Register data is clocked into the other two registers in parallel. The Min and Max data output from one of the Swap Registers in each set of two is applied to two busses going to the Acquisition Memory. If the Max and Min data is to be reversed to maintain the correct time order of the samples before being stored, the alternate swap register in each set of two is enabled, and the Max and Min data is applied to the opposite busses to memory.

Acquisition mode is controlled in part by the Microprocessor via data latched into the Acquisition Mode Register (see also, "Time Base Mode Register" in this section). These data bits select the channel or channels to be acquired, enable the XY mode, enable MIN/MAX acquisition, control the Swap function for reordering data, and select the Test function for diagnostics. Acquisition clock signals generated by the Acquisition Clock Decoder transfer the data from stage to stage in the digital acquisition circuitry in a pipe-line fashion.

A Diagnostics Code Generator is included as a troubleshooting aid. When in the Test mode, the A/D Buffer is disabled, and the Code Generator places its counter-output bytes on the input bus to the Max and Min Registers.

Acquisition Memory

The Acquisition Memory is composed of two, 2-K by 8-bit random-access memory devices. One memory stores the Odd data bytes and the other stores the Even data bytes. The Odd and Even data can be swapped between the Swap Registers and the Acquisition Memory.

A programmable address counter is loaded with the number that is the amount of pretrigger data bytes needed to fill the pretrigger portion of the waveform acquisition. The PREFULL signal is sent to the Trigger Mux circuitry when the pretrigger count is full. That signal enables the Trigger Mux circuitry to accept a trigger signal. The remaining output bits from the Address Counter select the storage location for waveform data storage in the Acquisition Memory.

When waveform data is to be read out of the Acquisition Memory, the Address Counter is loaded with the address of the data for the waveform. The Microprocessor sequences through the addresses reading out the data bytes. Data transceivers allow data to be read from the memory to the bus or written from the bus to the memory.

Memory Address Registers place the address count on the bus along with bits that indicate the trigger status (TRIGD), the B trigger status (BTRIGD), the end-of-record status (ENDREC), and the byte-interrupt status (BYTEINT). These accompanying bits are used in establishing display attributes.

Memory writes, memory reads, and address counter load enabling and clocking are controlled by a quad, two-line-to-one-line multiplexer (Memory Control). Read and write signals from the Microprocessor control bus and write clocks are used to transfer the waveform data between the devices.

Digital Time Base

An accurate frequency source for synchronizing the Microprocessor with the other digital devices on the bus is provided by a 40 MHz oscillator. That frequency is divided

down by the Clock Generator to produce the various clocking rates. The Time Base Mode Register latches control data bits from the Microprocessor data bus to set the operating mode of the time base. These control bits switch the Trigger Mux circuit to either A or B Trigger, enable the trigger logic circuit, switch the clock multiplexer to change the clocking rate, start a storage acquisition, and enable interrupts to the Microprocessor. The programmable Time Base Divider, under control of the Microprocessor via the Time Base Divider Register, generates a sampling rate that corresponds to the front-panel SEC/DIV switch setting.

A Clock multiplexer at the end of the Time Base Divider chain selects the output of the Time Base Divider, the $\overline{\text{WRITECLK}}$, the $\overline{\text{CONV}}$ clock, or an external clock signal to generate the SAVECLK signal.

The Digital Time Base Trigger Logic circuit looks at whether the pretrigger data portion of the record has been filled. If the pretrigger portion is full, then the A or B Gate generates the trigger. When a trigger is generated in Repetitive Storage mode, the Clock Delay Timer measures the time delay between the arrival of the trigger and the convert clock. The time difference value is used by the Microprocessor to accurately position the acquired data with respect to the actual trigger point.

The delay difference between the start of the acquisition and the occurrence of the B trigger is also measured. This value is only used in BOTH HORIZONTAL MODE when running the B Horizontal display in Triggerable After Delay to provide a readout of the time delay between the A Trigger and the B Trigger points.

Acquisitions are counted to determine when a full record of data has been stored (ENDREC) and to keep track of the beginning and ending memory locations of the record. The Record Counter is also programmable to provide for the different record lengths for one-channel or two-channel acquisitions, different Pretrigger selections, and either 4K-byte or 1K-byte record length.

Digital Display

A custom IC handles the digital display generation. The Display Controller functions as an interface between the processor bus, display memory (RAM), and vector generators to form waveform and character displays on the crt. The controller reads a display list from the Display Memory and drives X- and Y-Vector Generators to create the waveform and readout displays. Z-Axis control signals are also generated to drive the crt Z-Axis Amplifier for Stored waveform and Readout intensity control. Control signals to the Microprocessor and Display Memory are generated in response to a processor read/write request.

Digital-to-analog converters take the digital data bytes supplied from the Display Memory via the Display Controller and change them to the X- and Y-Axis analog signals that drive the Horizontal and Vertical Vector Generators. The vector signals are applied to the Horizontal and Vertical Output Amplifiers to produce the STORE mode deflection signals and NON STORE mode character readout.

The Display Memory is six 16-K X 4-bit dynamic random access memories (RAM). Four of the RAMs provide the 8-bit data bytes of the stored waveform, and the remaining RAMs store each data-byte's intensity and Status attributes. A 4-bit word in each RAM is selected by latching a row address followed by a column address. Data is either stored or read out (as the operation in progress requires).

Vector Generator

X- and Y-Axis analog signals from the Digital Display are converted by the Vector Generators into the vector signals used to drive the crt deflection plates. Vector signals are produced for the stored waveforms, the menu displays, and the readouts. The Vector Generator is switched to the dot-display mode for equivalent-time sampling waveforms and X-Y displays.

The X-Y Plotter driver circuit is included in this portion of the circuitry. When the X-Y Plotter is enabled, x-axis and y-axis signals are switched via the plot multiplexer to the x-axis and y-axis plot amplifiers. The $\overline{\text{VECT SMPL}}$ signal is switched via the same multiplexer to drive the Pen-Down amplifier.

Z-Axis

The Z-Axis Amplifier has input signals from multiple sources that control the crt intensity on a time-shared basis. Nonstore intensity signals are the level inputs from the A and B INTENSITY controls that are controlled by the Alternate Display switching and B Z-Axis Logic circuits. Additional Z-Axis drive current is supplied during the intensified portion of an A trace during the B Sweep when BOTH Horizontal display mode is selected. The remaining nonstore signals that have control of the display brightness are the EXT Z-AXIS INPUT signal, the CHOP mode blanking signal, and the $\overline{\text{XY}}$ control signal. All of these sources are added to provide the time-shared nonstore displays.

For the Store waveform and the Menu and Readout character displays, an additional Z-Axis drive signal from the STORAGE/READOUT INTENSITY control is switched on and off by the Display Controller. The controller signals determine when the stored waveforms and the readout

characters are turned on and if any portions of the display will be intensified more than the rest. Further amplification of the combined signal sources provides the amplitude levels required to drive the crt.

The Z-Axis signal is applied to the crt DC Restorer circuit where it is shifted to the large negative potential used by the crt. The potential controls the amount of current supplied by the electron beam to the crt phosphors.

Power Supply

Operating potentials for the instrument are obtained from a power supply that consists of the Preregulator, Inverter and Transformer, and Rectifiers and Filters. Approximately +42 V is supplied by the Preregulator to drive the 20 kHz Inverter stage through the Transformer primary windings. The transformer secondary windings produce the various ac levels that are rectified and filtered to provide the supply voltages for the instrument's circuitry. A High Voltage Multiplier circuit produces the accelerating, focus, and cathode potentials used by the crt.

Probe Adjust

A front-panel PROBE ADJUST output is provided for use in adjusting probe compensation. The voltage at the PROBE ADJUST connector is a negative-going square wave that has a peak-to-peak amplitude of approximately 0.5 V with a repetition rate of approximately 1 kHz.

Communications Options

Options for this instrument provide a choice of either an IEEE-488 GPIB (General Purpose Interface Bus) or an RS-232-C serial output port. The options allow the transfer of stored waveforms and the control of certain instrument functions.

DETAILED CIRCUIT DESCRIPTION

The detailed circuit description of the 2230 first describes the analog operating portion of the oscilloscope followed by the digital portion. During the description of the analog circuitry, references are made to circuitry that either provides information to the Microprocessor or is controlled by the instrument's storage circuitry.

ANALOG CIRCUITRY

The instrument has full conventional oscilloscope capabilities with all the associated analog circuitry. Signal pickoff points and signal insertion points connect the analog portion of the instrument to the digital operating system to acquire and display the stored waveforms. The digital circuitry enhances the analog display by providing crt readouts of the VOLTS/DIV, SEC/DIV, and Delay Time Position control settings.

VERTICAL ATTENUATORS

The Channel 1 and Channel 2 Attenuator circuits, shown on Diagram 1, are identical with the exception of the additional Invert circuitry in the Channel 2 Paraphase Amplifier. Therefore, only the Channel 1 Attenuator is described, with the Invert circuitry of Channel 2 discussed separately.

The Attenuator circuit and switches (see Figure 3-2) provide control of the input coupling, the vertical deflection factor, and the variable volts/division gain. Vertical input signals for display on the crt or for acquisition by the storage circuitry may be connected to either or both the CH 1 OR X and the CH 2 OR Y input connectors. In the X-Y mode of operation, the signal applied to the CH 1 OR X connector provides horizontal (X-axis) deflection for the display, and the signal applied to the CH 2 OR Y connector provides the vertical (Y-axis) deflection for the display.

Switch contacts on the A14 CH 1 Logic board are read by the Microprocessor to find the CH 1 VOLTS/DIV switch and Input Coupling switch settings. A switch contact associated with CH 1 CAL control R43 (Variable Volts/Div) is also read to see whether that control is in or out of the calibrated (CAL) detent.

Input Coupling (AC-GND-DC)

A signal from the CH 1 OR X input connector may be ac or dc coupled to the High-Impedance Attenuator circuit or disconnected completely by the Input Coupling Switch. Signals from the CH 1 OR X input connector are routed through resistor R1 to Input Coupling switch S1. When S1 is set for dc coupling, the Channel 1 signal goes directly to the input of the High-Impedance Attenuator stage. When

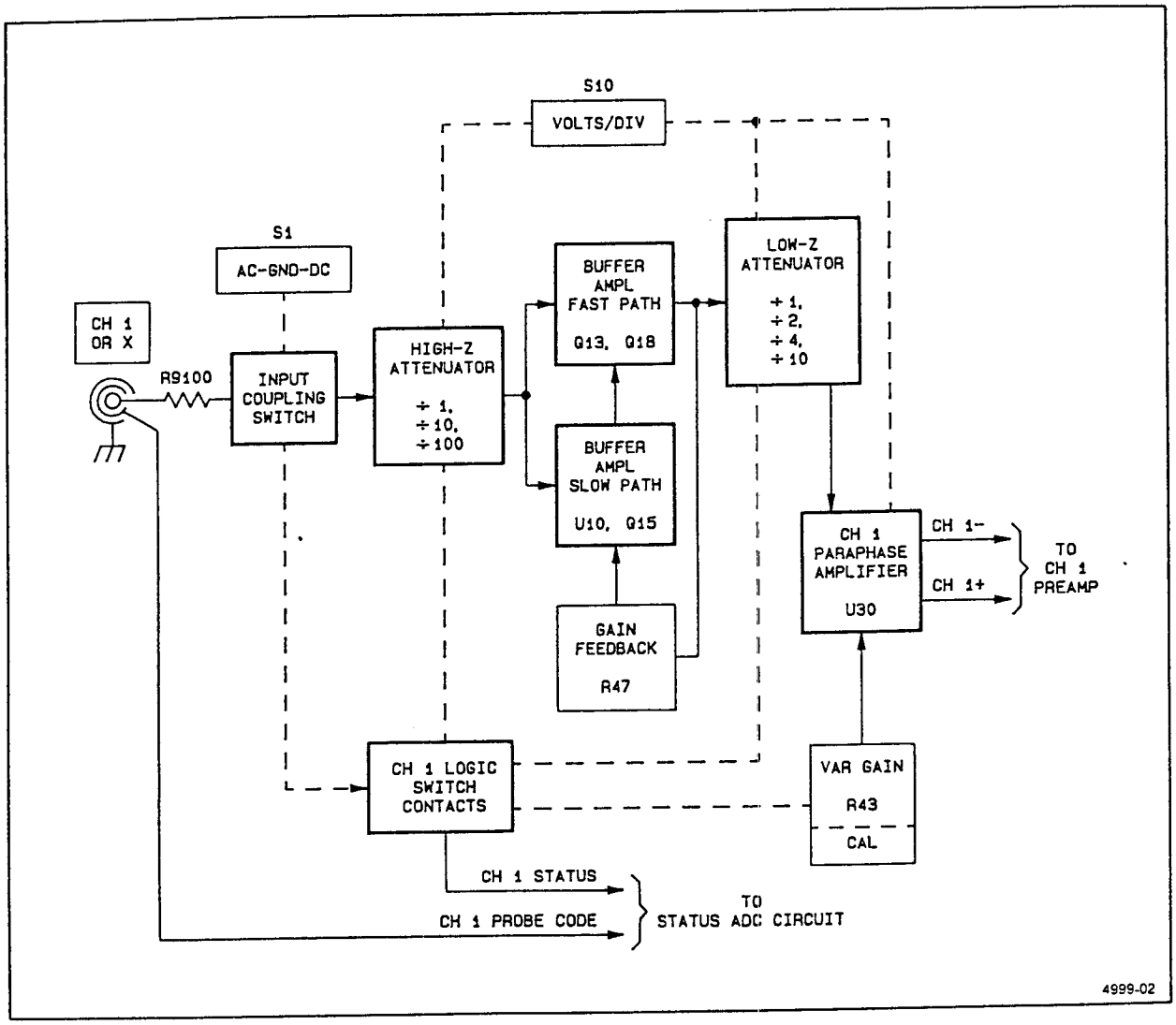


Figure 3-2. Block diagram of the Channel 1 Attenuator circuit.

ac coupled, the input signal must go through dc-blocking capacitor C2. The blocking capacitor stops the dc component of the input signal from reaching the Attenuator circuit. When switched into the signal path, attenuators AT1 and AT2 attenuate the input signal by factors of 100 and 10 respectively. When S1 is set to GND, the input of the Buffer Amplifier is connected to ground. This provides a ground reference for the analog display and the Microprocessor without removing the applied signal from the input connector. The coupling capacitor precharges through R2, R4, and R8 to prevent large trace shifts when switching from GND to AC.

A probe coding ring on the CH 1 OR X input connector is used to read the attenuation factor of the attached probe to automatically adjust the VOLTS/DIV scale factors in the readout. The default setting is for X1 attenuation when either coaxial cables or uncoded probes are connected to the vertical inputs.

Buffer Amplifier and Low-Impedance Attenuator

The Buffer Amplifier presents a high-impedance, low-capacitance load to the signal from the High-Impedance Attenuator and a low output impedance to the Low-Impedance Attenuator. The dual-path buffer amplifier (slow path and fast path) combines good dc stability with high-speed performance.

The input signal goes to the gate of source-follower Q13 through R6 and C6, the fast path, and to the inverting input of operational amplifier U10 from the resistive voltage divider formed by R3 and R5, the slow path. Source-follower Q13 and emitter-follower Q18 have high-impedance inputs that isolate the applied signal from the loading effects of the Low-Impedance Attenuator. A voltage divider formed by R46, R47, and R48 at the emitter output of Q18 applies feedback to the noninverting input of slow-path amplifier U10. The two input voltages to amplifier U10 are compared, and the conductivity of current-source transistor Q15 is changed to correct for any frequency-gain error at the source of Q13. The bandwidth of U10 is limited by capacitor C10 so that the slow path responds only to frequencies below 100 kHz. Input offset voltage compensation for U10, provided by R10, eliminates trace shift between VOLTS/DIV switch settings. Gain in both paths is matched by adjusting MF/LF Gain Bal potentiometer R47. The path gains then remain matched by the corrective action of U10 and Q15 if gain differences in the two paths start to develop.

Low-Impedance Attenuator R19 divides down the Buffer Amplifier output signal for application to Paraphase Amplifier U30. The attenuator's output impedance is 75 ohms at all VOLTS/DIV switch settings. The VOLTS/DIV switch (S10) determines whether the Paraphase Amplifier receives a signal attenuated by a factor of 1 (no attenuation), 2, 4, or 10.

Paraphase Amplifier

Paraphase Amplifier U30 converts the single-ended signal from the Low-Impedance Attenuator into a differential signal for the Vertical Preamplifier. Included in the circuitry is switching that provides extra gain for the 2 mV position of the VOLTS/DIV switch, adjustments for amplifier dc balance, and circuitry for the Variable Volts/Div function. Additionally, Channel 2 Paraphase Amplifier U80 contains circuitry to invert the Channel 2 display.

The signal from the Low-Impedance Attenuator goes to the base of one transistor in U30. The other input transistor is biased by the divider network formed by R30, R31, and R33 to a level that produces a null between the outputs of U30 (no trace shift on the crt screen) when the VOLTS/DIV control is switched between 5 mV and 2 mV. Emitter current for the two input transistors is supplied by R21, R22, R23, and VAR-BAL potentiometer R25. Resistor R29 is the gain-setting resistor between the two emitters. High-frequency compensation of the amplifier is provided by the series combination of R27 and C27 shunting R29. In the 2 mV position, amplifier gain is increased because contact 15 of S10 is closed to place 2 mV Gain potentiometer R26 and compensating capacitor C26 in parallel with R29.

The collector current from the two input transistors serves as emitter current for the two differential output transistor pairs. Base-bias voltages for the two output pairs are developed by the divider network formed by R39, R41, R42, and Variable Volts/Div potentiometer R43. The transistors of U30 have matched characteristics, so the ratio of currents in the two IC diodes connected to pin 11 determines the current ratios in the output transistor pairs. As Variable Volts/Div potentiometer R43 is rotated from calibrated to uncalibrated, the conduction level of the transistors connected to R35 increases. Since the transistor pairs are cross-connected, the increased conduction in one pair subtracts from the output current produced by the transistor pair connected to R38, and the overall gain of the amplifier decreases. VAR-BAL potentiometer R25 is adjusted to balance the amplifier for minimal dc trace shift as the Variable Volts/Div control is rotated.

Incorporated in the Channel 2 Paraphase Amplifier is circuitry that allows the user to invert the polarity of the Channel 2 signal. When INVERT switch S90 is out, the transistor pairs in U80 are biased as they are in U30, and CH 2 trace is not inverted. For the IN position of S90, connections to the bases of the output transistor pairs are

reversed, reversing the polarity of the output signal to produce an inverted Channel 2 trace and Channel 2 storage acquisition signal. The inverted/noninverted state is read by the Microprocessor, and an indicator is displayed in the crt readout adjacent to the CH 2 VOLTS/DIV readout to indicate to the user when INVERT is in effect. Invert Bal potentiometer R75 is adjusted for minimal dc trace shift when the INVERT button is changed between IN and OUT.

VERTICAL PREAMPLIFIERS

The Channel 1 and Channel 2 Vertical Preamplifiers, shown on Diagram 2, are identical in operation. Operation of the Channel 1 amplifier is described. Differential signal current from the Paraphase Amplifier is amplified to produce drive current to the Delay Line Driver and supply the Channel 1 signal to the Storage Acquisition circuitry. Internal trigger signals for the Trigger circuitry are picked off prior to the Vertical Preamplifier. The Channel Switch circuitry controls channel selection for the Nonstore crt display. STORE mode signal acquisition and display, and the selection of either STORE or NON STORE, is controlled by the Display Controller circuitry.

Common-base transistors Q102 and Q103, which complete the Paraphase Amplifier portion of the circuitry shown on Diagram 1, convert differential current from the Paraphase Amplifier into level-shifted voltages that drive the bases of the input transistors of Vertical Preamplifier U130. Differential internal trigger signals are picked off at this point from the collector signals of Q102 and Q103 before Vertical POSITION dc offset is added to the input signals.

The collector current of each input transistor of U130 is the emitter current for two of the differential output transistors. One of the collectors of each output pair supplies one side of the differential Nonstore signal to the Delay Line Driver, and the other collector in each pair supplies one side of the differential Channel signal to the Storage Acquisition circuitry. The base bias voltages of the output transistors are controlled by the Channel Switch Logic circuitry. The switching circuitry determines which channel is active (CH 1, CH 2 or both for ADD) in NON STORE, and which channel supplies the Storage Acquisition signal in STORE.

Vertical POSITION control R112 adds an offset voltage to the pair of differential transistors, Q114 and Q115, that supply the emitter current to the Preamplifier input transistors. Unequal collector currents from Q114 and Q115 go to the input transistors to introduce the vertical position offset to the Channel 1 NON STORE signal. Output signals from Q114 and Q115 are applied to a Storage Vertical Position conditioning circuit where dc offset adjustments provide tracking corrections between the vertical positions of the NON STORE and the STORE signals.

When Channel 1 is selected to drive the Delay Line Driver, the Q output (pin 5) of U540A is HI. That HI is switched through U7201 to the bases of the nonstore signal transistors (connected to pin 14 of U130). These transistors are then forward-biased, and the Channel 1 signal is conducted to the Channel Switch circuit. If Channel 1 is not selected, then the Q output of U540A is LO, and the nonstore signal transistors are reverse-biased to prevent the Channel 1 nonstore signal from being displayed. The gain of the Preamplifier is set by adjusting R145 to control the signal current that is shunted between the two differential outputs. Amplifier gain is reduced by the current shunted between the two halves of the Preamplifier.

Channel Switch Logic

The Channel Switch Logic circuitry, shown on Diagram 2, utilizes the front-panel VERTICAL MODE and STORE/NON STORE mode switches to select the crt display format. See Figure 3-3 for a block diagram of the circuit.

When any display mode other than X-Y is selected, the XY line connected to S550 is at ground potential. VERTICAL MODE switches S545 and S550 control the connection between the XY control line and the Set and Reset inputs of flip-flop U540A for the nonstore display formats.

CHANNEL 1 DISPLAY ONLY. The CH 1 position of S550 grounds the Set input (pin 4) of U540A while the Reset input (pin 1) is held HI by pull-up resistor R539. This produces a HI and a LO on the Q and $\overline{Q}$ outputs of U540A respectively. The levels are selected by multiplexer U7201, biasing on the Channel 1 nonstore output transistors in U130, allowing the Channel 1 input signal to drive the Delay Line Driver. The Channel 2 Preamplifier nonstore output transistors in U180 are biased off.

CHANNEL 2 DISPLAY ONLY. The CH 2 position of S550 holds the Reset input of U540A LO through CR538, and the Set input is held HI by pull-up resistor R538. The outputs of U540A are then Q LO and $\overline{Q}$ HI biasing on the Channel 2 Preamplifier nonstore output transistors (in U180) and biasing off the Channel 1 Preamplifier nonstore output transistors (in U130). Channel 2 then supplies the signal to drive the Delay Line Driver.

To display the ADD, ALT, or CHOP formats, S550 must be in the BOTH position to ground the A, C, and F pins of S545.

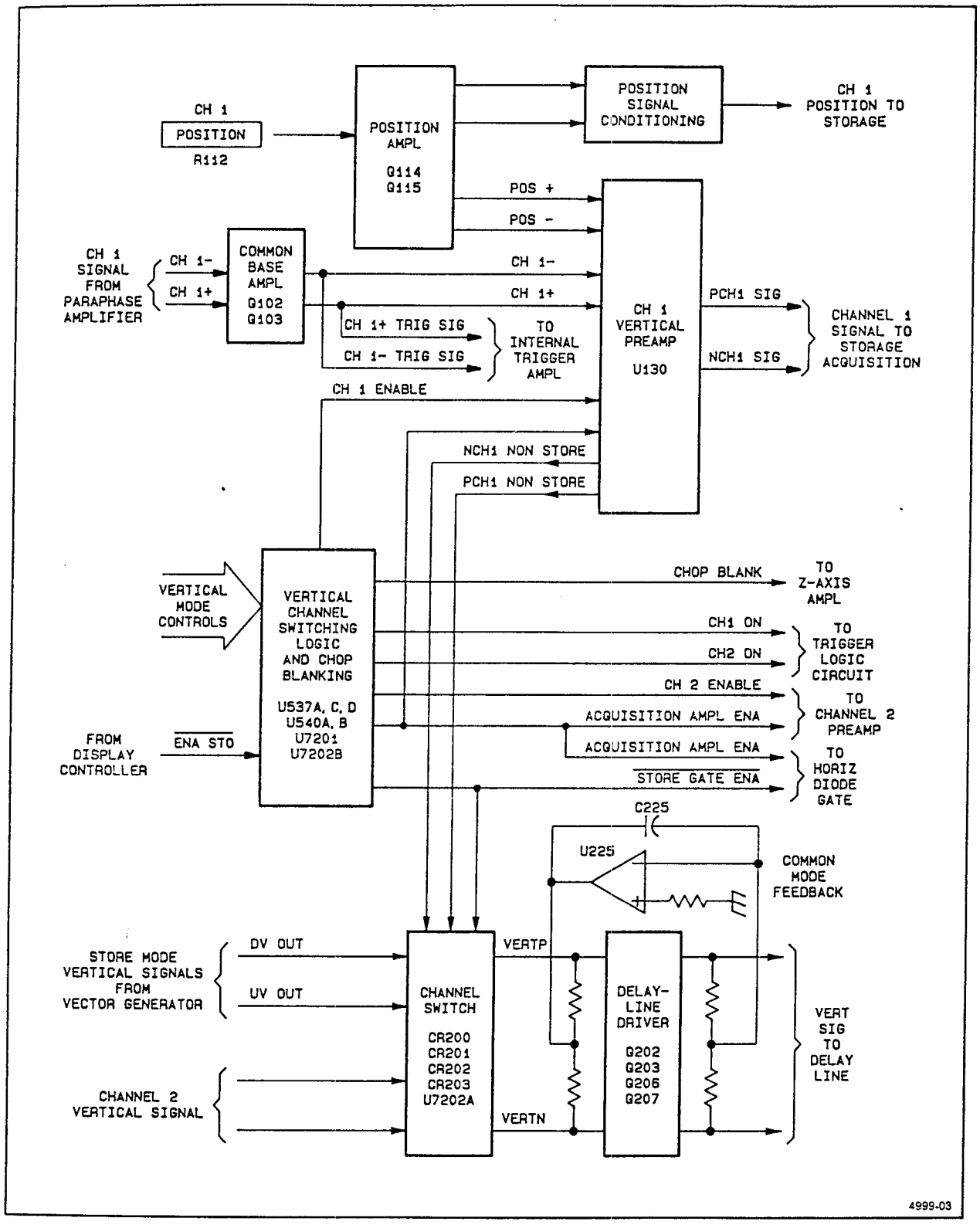


Figure 3-3. Store-Non Store Vertical Switching.

ADD DISPLAY. In the ADD position of S545, both the Set and Reset inputs of U540A are held LO by CR534 and CR537. The Q and $\overline{Q}$ outputs of U540A are then both HI, and signal currents from the Channel 1 and Channel 2 Preamplifiers add together to drive the Delay Line Driver.

CHOP DISPLAY. In the CHOP position, the $\overline{\text{CHOP ENABLE}}$ line is held LO, keeping the Q output of flip-flop U540B HI. This enables CHOP multivibrator U537D to begin switching. The switching rate is determined primarily by the component values of R544, R545, and C545. The output of U537C (the inverted output of the multivibrator circuit) drives U537A and supplies the CHOP clock to flip-flop U540A. The output of U537C also drives U537B, the CHOP Blanking Pulse Generator (see Diagram 9).

Coupling capacitor C547 and resistors R547 and R548 on pin 5 of U537B (see Diagram 9) form a differentiating circuit that produces short duration pulses during the switching of U540A. These pulses are inverted by U537B to generate the Chop Blank signal to the Z-Axis Amplifier. The pulses blank the crt during CHOP switching times.

The Alt Sync signal on pin 2 of U537A (see Diagram 2) is HI except during hold off. While pin 2 is HI, the output of U537C is inverted and passed by U537A to the clock input (pin 3) of U540A. Since the $\overline{Q}$ output of U540A is connected back to the D input, and both the Set and Reset inputs are HI, the outputs of U540A switch (change states) with each clock input. The Delay Line Driver is then supplied alternately from the Channel 1 and Channel 2 Preamplifiers at the CHOP rate.

ALTERNATE DISPLAY. In ALT, the $\overline{\text{CHOP ENABLE}}$ line is held HI, disabling CHOP multivibrator U537D. The output of U537C, the chop blanking signal, is HI. Input signals to U537A are the HI from U537C and ALT SYNC from the Hold-Off circuitry in the A Sweep Generator. The output of U537A is then the inverted ALT SYNC signal that clocks Channel Select flip-flop U540A. The $\overline{\text{ALT SYNC}}$ clock toggles the outputs of U540A at the end of each sweep so that the Channel 1 and Channel 2 Preamplifiers alternately drive the Delay Line Driver.

STORE MODE DISPLAYS. Under direction from the Display Controller, multiplexer U7201 selects either nonstore or store signals to drive the Delay Line Driver. In NON STORE, the multiplexer switches the Q and $\overline{Q}$ outputs of U540A to the Channel Switch to allow the switching sequences just described. However, when STORE is selected, the nonstore analog signal to the Channel Switch is turned off, and the store vertical deflection analog signals are applied to the Delay Line Driver input. The store waveform display is determined by the Display Controller.

The nonstore output transistors are biased off by setting pins 9 and 12 of U7201 LO. The forward bias is removed, and the nonstore path is disabled. Pin 7 of U7201 is switched LO in STORE mode. Inverter U7202B inverts the LO, supplying forward bias to the store output transistors in both Preamplifiers. Selection of either channel signal for digitizing is done by a channel switch IC in the Storage Acquisition circuit (Diagram 10).

The HI STORE ENABLE signal from U7202B also goes to the Sweep Sep circuit to disable that circuit during STORE mode and to Horizontal Diode Gate circuit (Diagram 7) to block the nonstore sweep signals from going to the Horizontal Output Amplifier. To complete the switching to STORE mode, Pin 4 of U7201 is switched HI and applied to Inverter U7202B. The LO output signal from U7202B (STORE) is applied to the Vertical Channel Switch circuit to pass the STORE mode vertical deflection signal to the Delay Line Driver. That same LO signal also goes to the Horizontal Mux to pass the STORE mode horizontal deflection signal to the Horizontal Output Amplifier.

A Z-Axis disabling signal $\overline{\text{DIS Z}}$ applied to NAND-gate U537B (see Diagram 9) disables the Chop Blanking circuitry for STORE mode displays. ($\overline{\text{DIS Z}}$) holds the output of the Chop Blanking circuit HI to block the nonstore Z-axis signals from the Z-Axis Amplifier.

VERTICAL OUTPUT AMPLIFIER

Vertical Output Amplifier circuitry, shown on Diagram 3, amplifies the vertical signal and drives the crt deflection plates. The Delay Line Driver converts the signal into a signal voltage to drive the Delay Line. Delay Line DL9210 delays the vertical signal so that the leading edge of the triggering signal can be viewed. The BW LIMIT switch reduces the bandwidth of the Amplifier when required by the application. The Vertical Output Amplifier drives the vertical deflection plates of the crt. The A/B Sweep Separation circuit vertically positions the Nonstore B trace with respect to the Nonstore A trace in Alt Horizontal mode displays.

Delay Line Driver

The Delay Line Driver converts the signal current from the Vertical Preamplifiers or the Store mode Vector Generator circuitry into a signal voltage to drive the Delay Line. Transistors Q202, Q203, Q206, and Q207 form a differential shunt feedback amplifier with the gain controlled by feedback resistors R216 and R217. Amplifier compensation is provided by C210 and R210, and output common-mode dc stabilization is provided by U225. Should the dc voltage at the junction of R222 and R223 move off zero, U225 changes the base current supplied to

Q202 and Q203 through R202 and R203 to return the output of the Delay Line Driver to an average dc voltage of zero.

Delay Line DL9210 adds about 90 ns of delay to the vertical signal. In that time, the Sweep Generator has sufficient time to start producing a sweep before the vertical signal that triggered the sweep reaches the crt. This permits viewing the leading edge of the triggering signal.

Bandwidth Limit

BW LIMIT switch S226, C228, C229, and the diode bridge formed by CR226, CR227, CR228, and CR229 reduce the bandwidth of the amplifier when desired. With full 100 MHz bandwidth, R226 is grounded through BW LIMIT switch S226, and the nonconducting diode bridge isolates C228 and C229 from the vertical signal. With limited bandwidth on, R226 is connected to the +8.6 V supply, and the diode bridge is forward biased. The two bandwidth limiting capacitors are then in the vertical signal path, and high-frequency signals (above about 20 MHz) are attenuated.

Vertical Output Amplifier

The Vertical Output Amplifier drives the vertical deflection plates of the crt. Signals from the Delay Line go to a differential amplifier formed by Q230 and Q231 with low- and high-frequency compensation provided by the RC networks between the emitters. Thermal compensation is provided by thermistor RT236, and overall circuit gain is set by R233. The output stage of the Amplifier is two totem-pole transistor pairs, Q254-Q256 and Q255-Q257, that convert the collector currents of Q230 and Q231 to proportional output voltages. Resistors R256, R258, R257, and R259 are feedback elements and bias voltage dividers. Biasing is set so each transistor in a pair develops one-half the final output voltage on a side. The amplifier output signals drive the Vertical crt deflection plates.

Beam Find is used to keep the vertical trace within the graticule area for locating off-screen and over-scanned traces. When the front-panel BEAM FIND switch opens the contacts of S390 (found on Diagram 9), the direct −8.6 V supply to R261 is removed, and emitter current goes through R261 and R262 in series. The added series resistance reduces the amount of available emitter current and limits the amplifier's dynamic range. In normal amplifier operation, S390 connects the −8.6 V supply directly to R261, and full emitter current is possible in the output transistors.

A/B Sweep Separation Circuit

The circuit formed by Q283, Q284, Q285, and associated components acts to vertically position the Nonstore B trace with respect to the Nonstore A trace in BOTH Horizontal mode. In the B Sweep interval, the $\overline{\text{SEP}}$ signal from the Alternate Display Switching circuit (Diagram 6) is LO, and Q283 is biased off. This puts A/B SWP SEP potentiometer R280 in the circuit where it can affect the bias level on one side of the differential current source formed by Q284 and Q285. Changing the bias adds a dc offset current to the Vertical Output Amplifier that moves the B trace vertically with respect to the A trace.

During the Nonstore A sweep interval, the $\overline{\text{SEP}}$ signal is HI, and Q283 is turned on to isolate potentiometer R280 from the biasing circuit of Q284. The base voltages of Q284 and Q285 are then equal. With the same bias to both sides of the Vertical Output Amplifier, no offset is added to the A trace. In STORE mode, the HI STORE signal placed on the base of Q282 keeps Q283 off, and the A/B Sweep Sep circuit on.

TRIGGERING

The Trigger Amplifiers, shown on Diagram 4, provide trigger signals to the Sweep Generators from either the Vertical Preamplifiers, the EXT INPUT connector, or the power line. The A&B INT switch selects either Channel 1 or Channel 2 as the trigger source, and the A SOURCE switch selects between internal, line, or external trigger sources. See Figure 3-4 for the block diagram of the trigger amplifiers and switching circuitry.

Internal Trigger Pickoff

Signals from the Vertical Preamplifiers drive the CH1 and CH2 Internal Trigger Amplifiers with channel selection determined by the VERTICAL and HORIZONTAL MODE switches. Trigger signal pickoff from Channel 1 is done by Q302 and Q303, and Q327 and Q328 pick off the Channel 2 internal trigger signal. The circuitry associated with Channel 2 is the same as that for Channel 1 except for a trigger offset adjustment. Channel 1 trigger signal circuitry is described; equivalent components in Channel 2 perform identically.

Differential vertical signals from the Channel 1 Preamplifier go to Q302 and Q303. These emitter-follower transistors each drive one input transistor in trigger preamplifier IC U310. The collectors of the U310 input transistors in turn supply emitter current to a pair of two current-steering transistors. A compensation and biasing network is connected between the emitters of the input transistors. Trigger Offset potentiometer R309 in the emitter circuit adjusts the bias levels of the two input transistors of U310 to match the dc offsets of the Channel 1 and Channel 2 Trigger Amplifiers.

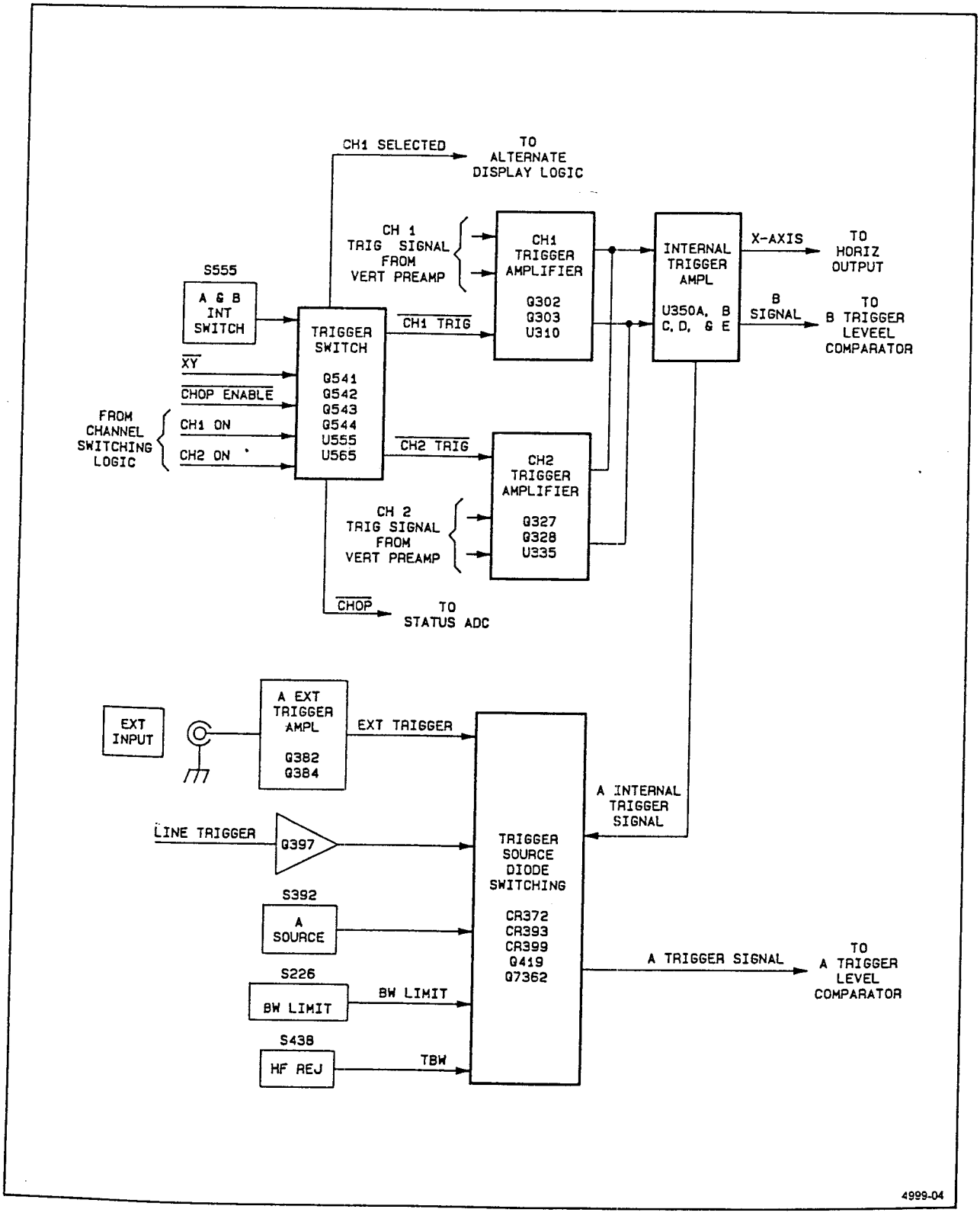


Figure 3-4. Block diagram of Trigger Amplifiers and Switching.

One transistor in each side of the output differential amplifier pairs of U310 has its base bias set to a fixed level by the divider network formed by R321 and R322. The bias voltage of the other transistor in each pair is controlled by the $\overline{\text{CH1 TRIG}}$ signal from the Trigger Switch circuitry. When the $\overline{\text{CH1 TRIG}}$ signal is HI, the transistors in each output pair with the collectors connected together (pin 6 and pin 14) are biased on, and the other transistors in the output pairs are off. The collector signal currents of the conducting transistors are equal in amount but of opposing polarity, so the signal is canceled. When the $\overline{\text{CH1 TRIG}}$ signal is LO, the other transistors in each pair are biased on, and a differential signal is developed across output load resistors R314 and R315 to drive the Internal Trigger Amplifier.

Internal Trigger Amplifier

The Internal Trigger Amplifier converts the differential trigger signals from the Vertical Preamplifiers into a single-ended signal that drives the X-Axis Amplifier and the A and B Trigger Level Comparators.

Differential signal current is applied to the emitters of U350D and U350E. The collector current of U350D is changed to a voltage signal and inverted by U350C. The opposite-phase collector current of U350E produces a voltage drop across R359 which is in phase with and adds to the voltage across R360 at the collector of U350C. The summed voltages appear at the base of U350A. Feedback resistor R357 provides thermal bias stabilization for U350C.

Emitter-follower U350A buffers the signal and shifts the dc level back to 0 V. The emitter output signal of U350A drives the X-Axis Amplifier, the B Trigger Level Comparator, and the base of emitter-follower U350B. The emitter signal of U350B in turn supplies the A Internal Trigger signal. The circuit arrangement of U350A and U350B, with the common collector current path through R363, produces thermal bias stabilization of the two transistors.

Trigger Switching Logic

Either Channel 1, Channel 2, or VERT MODE Internal Trigger signals may be selected by A&B INT switch S555 when A SOURCE switch S392 is set to INT. The INT position of the A SOURCE switch applies a voltage that reverse biases both CR393 and CR399 to stop the external trigger signal and the line trigger signal from reaching the A Trigger Level Comparator. The A Internal Trigger Signal from the emitter of U350B is passed to the A Trigger Level Comparator through forward-biased diode CR372.

CHANNEL 1. For triggering from Channel 1, the A&B INT switch is set to CH 1. The XY line connected to S555 is at ground potential, holding pin 4 of U555B LO. The output of U555B is then also LO, and the Channel 1 signal has a path through U310. At the same time, the Channel 2 signal path through U335 is shut off by the outputs of U555C and U565B both being HI.

CHANNEL 2. For triggering from Channel 2, the A&B INT switch is set to CH 2, and U555C pin 10 and U555D pin 12 are LO. The outputs of both AND-gates are then forced LO. A LO output from U555C enables the Channel 2 signal path through U335, and the HI outputs from U555B and U565C disable the Channel 1 path through U310.

VERT MODE. When the A&B INT switch is set to VERT MODE, the trigger source is selected by the two VERTICAL MODE switches. For all VERTICAL MODE switch combinations except BOTH-CHOP, the base of Q541 is HI. The inputs and outputs of U555B, U555C, and U555D are then all HI, and trigger signal selection is done by flip-flop U540A in the Channel Switch Logic circuit (Diagram 2) using the CH1 ON and CH2 ON control signals going to U565B and U565C.

With Channel 1 selected (VERTICAL MODE switch set to CH 1), both inputs to NAND-gate U565C are HI. The output of U565C is then LO, and U310 is biased on to select Channel 1 as the Internal Trigger signal source. The LO CH2 ON signal from the $\overline{\text{Q}}$ output of U540A is applied to U565B, and the $\overline{\text{CH2 TRIG}}$ line at the output of U565B is forced HI to shut off the Channel 2 Trigger signal path.

When Channel 2 is selected (VERTICAL MODE switch set to CH 2), the outputs of U540A, U565B, and U565C will be the reverse of the states described for Channel 1 selection. The Channel 2 signal is then selected as the Internal Trigger signal source, and the Channel 1 Trigger signal path through U310 is shut off.

With ALT VERTICAL MODE selected, the inputs of NAND-gates U565B and U565C toggle (change state) with each sweep. The outputs of the two gates also toggle, and U310 and U335 are alternately biased on to select the displayed channel signal as the Internal Trigger source.

In the ADD VERTICAL MODE position, both inputs to U565B and to U565C are HI, making the outputs of both gates LO. Both the Channel 1 and the Channel 2 signal path are turned on by biasing on U310 and U335 together. The output currents of both Trigger Preamplifiers are summed in the Internal Trigger Amplifier to produce the Internal Trigger signal.

The CHOP VERTICAL MODE position grounds the base of Q541 and puts a LO on an input of both U555B and U555C. The outputs of these two gates are then LO, and the signal to the Internal Trigger Amplifier is the summed Channel 1 and Channel 2 trigger signals, the same as with ADD VERTICAL MODE.

A External Trigger Amplifier

The A External Trigger Amplifier buffers signals from the EXT INPUT connector to drive the A Trigger Level Comparator. Input signal coupling is determined by A EXT COUPLING switch S380 which selects AC, DC, or DC ÷ 10 coupling.

When S380 is in the AC position, the input signal is ac-coupled through C376. In the DC position, the input signal is connected directly to the Amplifier. The DC ÷ 10 position attenuates the input signal by a factor of 10 through the compensated divider formed by R377, R378, C380, and C381.

Line Trigger Amplifier

The Line Trigger Amplifier supplies a line-frequency trigger signal to the A Trigger Level Comparator when the A SOURCE switch is in the LINE position. Transformer T390 in the Power Supply (Diagram 8) provides the line-frequency trigger signal through R397 to Q397. Diode CR399 is forward biased when S392 is in the LINE position, and the emitter signal of Q397 drives the A Trigger Level Comparator.

Trigger Signal BW Limit and HF REJ

The upper frequency of the trigger signal and the vertical channel bandpass are limited to 20 MHz when the front-panel BW LIMIT switch is pressed in. The BW Limit signal voltage forward biases Q419, and capacitor C419 shunts the higher trigger signal frequencies to ground through the transistor. With full 100 MHz bandwidth, Q419 is biased off to remove the shunting effect from the trigger signal line.

An additional bandwidth limiting circuit provides high-frequency rejection of the trigger signal. HF REJ is enabled when the center knob of the A TRIGGER LEVEL control is rotated clockwise. With HF REJ, Q7362 is biased on, and capacitor C7362 shunts trigger signal frequencies above about 50 kHz to ground through the transistor.

P-P Auto Trigger Level

The P-P Auto Trigger Level circuit sets voltage levels at the ends of the A TRIGGER LEVEL potentiometer (R438) as a function of the A Trigger mode selection and the trigger signals selected by the A SOURCE switch.

In the P-P AUTO and TV FIELD Trigger modes, Q413 is biased off, and CR414 and CR415 are reverse biased. Trigger signals selected by the A SOURCE switch are sent to peak detector circuits formed by Q420-Q422 and Q421-Q423 via R420. These peak detectors track dc levels and have high voltage-transfer efficiency. The circuit arrangement of the transistors produces very low thermal drift and reduces the effect of differences in transistor characteristics.

The positive- and negative-peak signal levels are stored by hold capacitors C414 and C415. The charge on the capacitors is held near the peak voltage levels between trigger signal peaks by the long time constant discharge path through R426 and R427. Amplifiers U426A and U426B are voltage followers with feedback supplied by transistors Q428 and Q429. These feedback transistors compensate the P-P Auto Trigger Level circuit for any thermal drift of Q420 and Q421 and shift the output levels of the voltage followers back to the original dc levels of the input trigger signal peaks. The output of U426A is the positive peak voltage of the input trigger signal, and the output of U426B is the negative peak voltage. Auto Level Adjustment potentiometers R434 and R435 provide dc offset corrections to make certain that the output voltages applied to the ends of LEVEL potentiometer R438 remain at or just below the actual peaks of the input trigger signal. In this way, the range of the LEVEL control is held within the peak-to-peak limits of the applied trigger signal for ease in triggering the oscilloscope.

In NORM Trigger mode, +8.6 V is applied to the junction of R411 and R414. Diode CR414 is forward biased. Transistor Q413 is also turned on inverting the applied signal and forward biasing CR415. Input transistors Q420 and Q421 are then biased off, and no trigger signals reach the P-P Auto Trigger Level circuit. In this case, the inputs to U426A and U426B are fixed voltages, and the voltage levels applied to the ends of the LEVEL potentiometer are independent of trigger-signal amplitude. The user must then adjust the LEVEL control to the correct level to obtain triggering.

The Microprocessor is informed of the trigger mode by Q7440 and its associated biasing resistors. When the $\overline{\text{P-P}}$ signal line is a LO at −8.3 V (indicating that the P-P AUTO Trigger mode is in effect), Q7440 is biased off, and its collector (and the PP signal line to the I/O circuit board) is pulled up to the +5 V supply via R7442. When the $\overline{\text{P-P}}$ signal is a HI at +8.5 V for NORM Trigger mode, Q7440 is biased on, and the PP signal is pulled LO by the conducting transistor.

A Trigger Level Comparator and Schmitt Trigger

The A Trigger Level Comparator compares the level of trigger signals selected by the A TRIGGER SOURCE

switch to the voltage set by the A TRIGGER LEVEL control and produces an output trigger signal at the correct level. Rising or falling slope triggering is selected by the front-panel A TRIGGER SLOPE switch.

Integrated circuit U460, contains the A Trigger Level Comparator and Schmitt Trigger circuitry. The output voltage of the trigger amplifiers are applied to U460 pin 4. The other input to the comparator is the wiper voltage on the A Trigger LEVEL control, applied to pin 2 of U460. The resistor R452 and the voltage at pin 5 of U460 sets the emitter current for the comparator.

The Trigger Slope is determined by the relative voltages on U460 pins 7 and 8. If pin 8 is at a higher level than pin 7, the plus output of U460 will change to a HI state when a positive-going input signal crosses the threshold at pin 2 of U460. With pin 8 more negative than pin 7, the Schmitt fires on a negative-going input. The voltage at pin 7 is fixed, while that at pin 8 is selected by the A TRIGGER SLOPE switch S460 through R459, R461, and R462.

The sensitivity of the Schmitt Trigger is controlled by the current at pin 9. The setting of R471 determines the circuit hysteresis.

The outputs of the Schmitt Trigger are at pins 10 and 12 of U460. The outputs are at ECL levels and are from emitter followers internal to U460. Collector voltage to U460 is supplied through pins 11 and 14. When TV Field is not selected, the $\overline{SS}$ line connected to CR476 and R473 is LO. Transistors Q473 and Q474 are biased off which also biases Q487 off. Resistor R477 biases CR467 and CR477 on and the +Out Trigger signal from pin 10 of U460 passes through the diodes to U506-6 of the A Sweep Generator.

TV Trigger Circuit

When TV FIELD mode is selected the $\overline{SS}$ line is HI. This disconnects the high-speed trigger path by reverse-biasing CR467 and CR477. Setting the A Trigger level threshold near the center of the horizontal-sync-pulse swing establishes the untriggered level. This in combination with the peak detectors makes the circuit insensitive to the video information. The A TRIGGER and LEVEL controls are set to provide a pulse-train corresponding to the sync pulses of the TV signal. This pulse train is filtered by R467, C467, R468, R469, C469, and R470, resulting in dc levels at the bases of Q473 and Q474. The untriggered level (horizontal pulses) turns Q474 on, which causes Q487 to conduct, providing a LO to the sweep generator. When the TV-Vertical-Sync block occurs the polarity reverses, turning Q487 off and providing a positive-going signal to U506 pin 6 to initiate a sweep.

A SWEEP GENERATOR AND LOGIC

The A Sweep Generator and Logic circuitry, shown on Diagram 5, produces a linear voltage ramp that drives the Horizontal Preamplifier in the Nonstore mode. The Sweep Generator circuits also produce gate signals that time the crt unblanking and intensity levels for viewing the Nonstore displays. In STORE mode, the A Sweep Generator and Logic circuitry continues to produce timing gates used by the Storage circuitry for triggering the analog signal acquisitions. See Figure 3-5 for the block diagram of the A Sweep Generator and Logic circuitry.

The Sweep Logic circuitry controls the Nonstore hold-off time and generates gating signals that start the sweep when a trigger signal occurs and end the sweep at the proper level. When using P-P AUTO or TV FIELD triggering, the Sweep Logic circuitry causes the Sweep Generator to free run if a trigger signal is not received or does not come often enough.

A Miller Sweep Generator and SEC/DIV Switching

The A Miller Sweep Generator is an integrator circuit that produces a linear voltage ramp to drive the Horizontal Amplifier for the Nonstore A Sweep deflection. It produces the ramp voltage by maintaining a constant current through timing capacitors, causing a linear voltage rise across them as they charge.

Field-effect transistors Q704A and Q704B are matched devices with Q704B acting as the current source for Q704A. Since the gate and source of Q704B are connected together with no voltage difference between them, the source current available to Q704A is just enough so that there is no voltage drop across the gate-source junction of Q704A.

When the sweep is not running, Q701 is biased on, holding the selected timing capacitors discharged. The low impedance of Q701 in the feedback path holds the A Miller Sweep output (A SWEEP) near ground potential. The voltage across Q701, in addition to the base-emitter voltage of Q706, prevents Q706 from becoming saturated.

A sweep ramp is started when Q576 is biased off. The $\overline{A\ GATE}$ signal going to the base of Q701 from the Sweep Logic circuit turns Q701 off. The timing capacitors then begin charging at a rate set by timing resistors R701, R702, and the selected timing capacitors. Due to feedback from the circuit output through the timing capacitors, the integrator input voltage at the gate of Q704A remains fixed and sets a constant voltage across the timing resistors. This constant voltage produces a constant charging

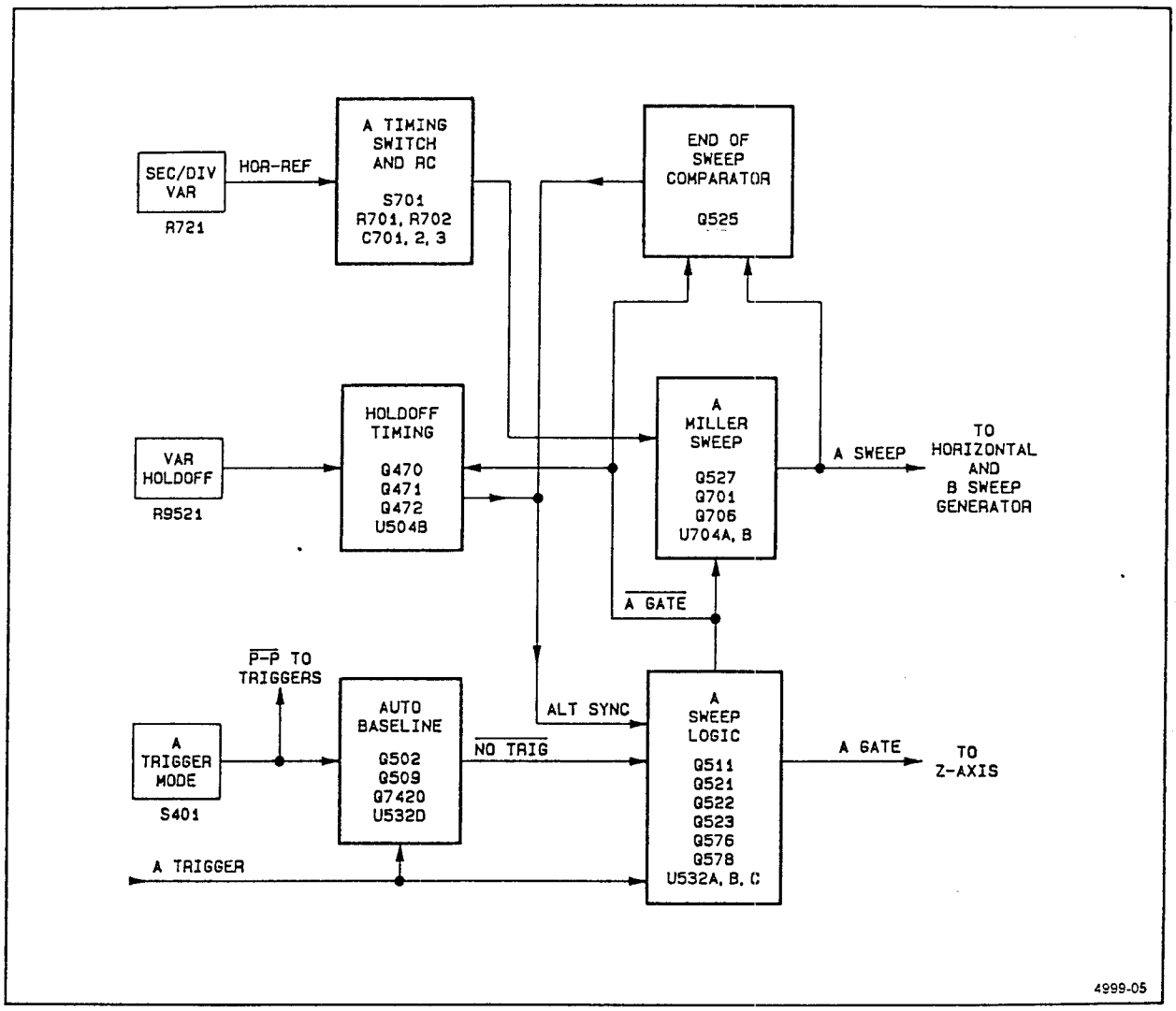


Figure 3-5. A Sweep Generator and Logic circuitry.

current through the timing capacitors, which results in a linearly increasing voltage ramp as they charge. The ramp is the A SWEEP output signal at the collector of Q706.

Parallel timing capacitors C702 and C703 remain in the charging circuit for all SEC/DIV switch settings and are used mostly for high sweep speeds. Capacitors C701A and C701B are added in series at medium sweep speeds, and C701B alone is added to the charging path for slow sweep speeds.

When the ramp reaches approximately 12 V, the End-of-Sweep Comparator transistor (Q525) becomes forward biased. This action switches the $\overline{\text{A GATE}}$ HI and starts the analog hold-off period. During hold off the A Sweep Generator is reset. The $\overline{\text{A GATE}}$ signal going HI biases on Q701, and the timing capacitors are fully discharged before another sweep starts.

One end of timing resistor array R701 is connected to the HOR REF signal, and the other end is connected to the input of the Miller integrator by the SEC/DIV switch contacts. The voltage applied to the timing resistor array via the HOR REF signal varies with the setting of the front-panel Variable SEC/DIV control (R721, located on Diagram 7). The STORE mode time base is not affected by the variable potentiometer setting. In the CAL position of R721, a fixed reference level is applied to R701 to produce the calibrated Nonstore sweep speed ranges. Switch contacts actuated using the knob of R721 control the STORE mode 4K/1K Compress and the X10 MAG features. The X10 MAG feature works in both NONSTORE and STORE.

Coded analog signals developed by circuitry connected to the SEC/DIV switch contacts inform the Microprocessor of the A SEC/DIV switch setting. The Microprocessor then directs the Digital Time Base circuitry to set the correct STORE mode sampling rate.

A Sweep Logic

The A Sweep Logic circuitry controls sweep generation, as a function of incoming trigger signals and the A Trigger mode selected.

Incoming trigger signals from the output of U460 clock U502, a one-shot multivibrator, and cause the Q output of U502 to go HI. If another trigger signal is not received by U502 within the time limit determined by R503 and C501, the Q output (U502 pin 3) will go LO. Whenever trigger signals are being received, the $\overline{\text{Q}}$ output of U502 biases on Q509 to turn on DS518, the TRIG'D LED. The output of U502 is also used in the Auto Baseline circuit as described in the "P-P AUTO and TV FIELD" part of the discussion that follows.

NORM. When NORM Trigger mode is selected, input pin 12 of U532D is held HI by S401B, causing the gate output to also be HI. The output of U532C is then LO, and U506 pin 3 is not held HI. Input pin 4 of U532A is held HI by S401C, causing the output to be LO, placing a LO on input pin 7 of dual flip-flop U506. Trigger signals received at input pin 6 (a clock input) of U506 then clock this LO to the Q output (pin 2).

During the previous hold-off period, U506 pin 2 was set HI by U532B. This made the $\overline{\text{Q}}$ output (pin 3) LO. The LO biased Q576 on, preventing the A Miller Sweep from running. Whenever U506 pin 6 is clocked by a trigger signal following hold off, the LO on the D input (pin 7) is transferred to the Q output (pin 2), and the $\overline{\text{Q}}$ output (pin 3) goes HI. This biases Q576 off, and the A Miller Sweep generates the sweep ramp as described in the previous "A Miller Sweep Generator" discussion. When the ramp voltage reaches about 12 V, End-of-Sweep transistor Q525 is biased on. The output of U532B then changes from LO to HI, setting U506 pin 2 HI and biasing on $\overline{\text{A GATE}}$ transistor Q576. This triggers Hold-off One-shot U504B to start the hold-off period, turning off Q525. Transistor Q701 in the A Miller Sweep generator is also biased on to discharge the timing capacitors during hold-off time.

With U504B triggered, output pin 10 changes from LO to HI, where it stays for a time set by the Hold-Off Timing circuitry and the A SEC/DIV switch position. VAR HOLD-OFF potentiometer R9521 sets the amount of current that is available to charge C518, C519, or C520 to the threshold voltage on pin 14. During the time pin 10 is HI, pin 5 (the set input) of U506 is held HI so that trigger pulses cannot start a new sweep. When pin 15 of U504B reaches the threshold level on pin 14, pin 10 goes LO to end hold off and release U506 from the set condition. The circuit is then reset to start another sweep on the next trigger pulse that appears at the clock input (pin 6) of U506. The holdoff capacitors are switched by transistors Q7470 and Q7471 according to the states of the timing switch. Q7472 serves as a dual diode to carry the discharge current. Logic signals AC-1 and AC-2 provide part of the timing switch information for the I/O board, where their states are read at an input port.

P-P AUTO and TV FIELD. When P-P Auto or TV Field trigger is in use, the Auto Baseline circuitry is active. Pin 12 of U532D is held LO by R569, and the output at pin 9 follows the signal provided by the Q output of U502.

If trigger signals are being received, U502 remains set. As long as U502 is set, the output of U532D is HI, causing the output of U532C to be LO. Dual flip-flop U506 then responds to trigger signals at Clock input pin 6 as described in the "NORM" part of this discussion. If trigger signals are not being received by U502, its output and the output of U532D are both LO. With a LO on pin 10 of U532C, its output is the inverse of the input signal applied to pin 11. At the end of hold-off, that output goes HI, making U506 pin 2 LO and pin 3 HI. This automatically generates the A Gate and $\overline{\text{A Gate}}$ signals, generating a sweep. The Auto Baseline continues holding NOR-gate U532C enabled so that new sweeps are generated at the end of hold-off as long as trigger signals are not received at U502.

SGL SWP. The following discussion presumes Nonstore mode. In Sgl Swp mode, both the P-P AUTO and NORM front-panel buttons are in their out position. This results in a LO at the output of U532C that does not permit flip-flop U506 pin 3 to be held HI. A LO is also on input pin 4 of U532A.

During hold-off, U532B makes U506 pin 14 HI and pin 15 LO, causing pin 7 (the D input) of U506 to be HI. After hold-off ends, clock signals (triggers) to U506 pin 6 keep U506 pin 3 LO, keeping the sweep generator held off. When the SGL SWP button is pushed in, pin 7 of U504A goes LO for a time period determined by the time constant of R504 and C504 and then returns HI. The HI clocks the HI on input pin 10 of U506 to output pin 15. Consequently the output of U532A goes LO, and CR514 is reverse biased to bias Q511 on, lighting the READY LED. The next trigger pulse applied to input pin 6 of U506 starts a sweep as described previously. At the end of the sweep, U506 pin 15 goes LO and pin 14 goes HI, causing the TRIG'D LED to go out and placing a HI on the input pin 7 of U506. A new sweep cannot be started until the SGL SWP button is again pressed, resetting the sweep.

In STORE mode, the major difference is that the STO-RDY line is not true until the processor recognizes that a trigger has occurred. This prevents the SGL SWP button from affecting the circuit directly. Instead, the processor determines the button was depressed, releases STO-RDY, causing the effect described above when a button is depressed in Nonstore mode.

X-Y. In the Nonstore X-Y mode, the $\overline{\text{XY}}$ signal is LO and Q522 is biased on, pulling pin 7 of U532B LO. The output of U532B holds U506 pin 3 LO and pin 2 HI, and no sweeps can be started during X-Y mode. Nonstore X-Axis deflection (horizontal) is determined by the CH 1 OR X input signal. In STORE mode, the A Sweep Logic circuit must run to produce the gating required to synchronize the Storage signal acquisition. The Store signal forward biases CR7140 to override the $\overline{\text{XY}}$ signal, and the A Sweep Logic circuitry operates as in Y-T Nonstore mode.

B TIMING AND ALTERNATE B SWEEP

The Alternate B Sweep circuitry, shown on Diagram 6, produces a linear voltage ramp that drives the Horizontal Preamplifier for Nonstore B Sweeps. The Alternate B Sweep circuitry also produces the sweep-switching signals that control the display of the A and B Nonstore Sweeps and the gate signals used by the Intensity and Z-Axis circuits to set the crt unblanking and intensity levels for the Nonstore A Intensified and the B Sweep displays. The B Gate signal goes to the Digital Time Base circuitry and is the Storage trigger signal for B Delayed Horizontal Display mode.

The B Sweep ramp is started by the B Sweep Logic circuit either at the end of the set delay time (RUNS AFTER DELAY) or when the first trigger signal occurs after the delay time has elapsed (Trigger After Delay). This delay time is a function of the B Delay Time Position Comparator circuit and the A Sweep.

B Miller Sweep Generator

The B Miller Sweep Generator is an integrator circuit formed by Q709, Q710A, Q710B, Q712, and associated timing components. This circuit produces the B Sweep signal and works the same as the A Miller Sweep Generator. See the "A Miller Sweep Generator" section for a description of circuitry operation. The output at the collector of Q712 drives the Horizontal Amplifier for Nonstore B Sweeps and is applied to the B end-of-sweep transistor, Q643.

B Trigger Level Comparator and Schmitt Trigger

The B Trigger Level Comparator and Schmitt Trigger are contained in U605. This circuit determines both the trigger level and slope at which the B triggering signal is produced. It functions in the same manner as the A Trigger Level Comparator and Schmitt Trigger with the exclusion of the TV trigger circuitry. See the "A Trigger Level Comparator and Schmitt Trigger" section for a description of circuit operation. The +OUT terminal of U605 is directly connected to the clock input of U670A to initiate the B Sweep when the B Trigger is utilized.

Run After Delay

The Run After Delay circuit lets the B Sweep Logic start a B Sweep without the need for a B Trigger signal. For the RUNS AFTER DELAY mode, B TRIGGER LEVEL

control R602 is rotated fully clockwise. In this position of R602, transistor Q637 is biased off, and a LO is present at its collector. Inverter U660D then has a HI output at pin 8. Resistor R640 provides positive feedback to obtain rapid switching of the transistor. This HI output reverse biases CR626 so that the state of U670A is determined by the level at U660F pin 12.

If the B TRIGGER LEVEL control is not fully clockwise, Q637 is biased on, and the B Sweep is in the triggerable-after-delay mode. The output of U660D is then LO which keeps the S input of U670A LO, preventing the flip-flop from being set by the output of U660F.

Operation of the B Sweep Logic circuitry under both triggering modes is described in the "B Sweep Logic" part of the following discussion.

Delay Time Position Comparator

The Delay Time Position Comparator circuit compares the amplitude of the A Sweep voltage ramp to the dc voltage level set by the position of B DELAY TIME POSITION potentiometer R9644. The output of the comparator enables the B Sweep Logic circuit to start the B Sweep after the end of the delay time.

The input voltages to Comparator U655 to be compared are the voltage from the wiper of B Delay Time Position potentiometer R9644 and the A Sweep voltage from the divider formed by R651, Delay Dial Gain potentiometer R652, and R653. Maximum and minimum input voltages are established by VR645 and R646 respectively for the noninverting input and by R652 for the inverting input. Delay Start potentiometer R646 is adjusted in conjunction with Delay End potentiometer R652 to set the B DELAY TIME POSITION crt readout calibration.

The comparator is controlled by the $\overline{\text{A ONLY}}$ gate signal connected to pin 6. When the $\overline{\text{A ONLY}}$ signal is HI, the comparator is able to make a comparison. While the A Sweep signal on pin 3 is below the wiper voltage on pin 2, the comparator output is at a HI level. When the A Sweep ramp reaches the comparison level, the output at pin 7 goes LO. If $\overline{\text{A ONLY}}$ is LO, the comparator is switched to a high impedance output state. The comparator output level is then a HI that goes to pin 9 of NAND-gate latch U680C and U680D.

B Sweep Logic

The B Sweep Logic circuitry utilizes signals from associated B Sweep circuitry to generate control signals for both the B Miller Sweep and the B Z-Axis Switching Logic circuits.

In the RUNS AFTER DELAY mode, the Run After Delay circuit holds the D input of flip-flop U670A LO via U660B. At the start of hold off when the A Sweep is reset, U680D pin 13 is strobed with an Alt Sync pulse negative transition. The output of the NAND-gate latch formed by U680C and U680D is latched HI, and the output of U660F goes LO. This places a LO on the S input of U670A and a HI on the R input causing the flip-flop to reset. The LO on pin 2 and a HI on pin 3 of U670A are converted to TTL levels by Q630 and Q631. The resulting HI on the collector of Q630 turns Q709 on. This discharges the B Miller Sweep timing capacitors to reset the B Sweep Generator and keeps a new B Sweep from starting. During the next A Sweep ramp when the voltage at U655 pin 3 exceeds the voltage at pin 2, the comparator output goes LO. The NAND-gate latch changes output states and causes the Set input of U670A to go HI. The LO on the Set input then controls the flip-flop, and the $\overline{\text{Q}}$ output of U670A goes LO. Shunting transistor Q709 shuts off, and the B Miller Sweep Generator runs to produce a sweep ramp.

When the ramp voltage reaches a level of about 12 V, B end-of-sweep transistor Q643 turns on and blanks the rest of the B Sweep trace by reverse biasing CR817 in the Z-Drive signal line (Diagram 9). The B Sweep Generator continues to run either until the ramp reaches about 13 V, at which time VR712 conducts to prevent the ramp voltage from increasing further, or until the A Sweep ends. In either case, the B Sweep generator is reset when the A Sweep ends.

The B Sweep Generator becomes reset when the the ALT SYNC signal goes from HI to LO to switch the output state of the U680C-U680D latch. The Reset input of U670A then goes LO, causing the $\overline{\text{Q}}$ output to switch HI and reset the Sweep Generator. Depending on the settings of the A and B SEC/DIV switches, the A Sweep may end before the B Sweep. In that case, the ALT SYNC signal going LO at the end of the A Sweep immediately resets the B Sweep Generator even if the sweep ramp has not reached its maximum amplitude. A new B Sweep starts the next time the B Delay Time Comparator goes LO.

When not in the Runs After Delay mode, the output of U660A is HI, and U670A has a HI on both the Set and the D input. The circuitry connected to the Reset input of U670A functions as described before. When the output of U660F goes HI, U670A is no longer held reset. In this case, the first B Trigger signal from the collector of Q630 after the end of the delay time clocks through the HI on the D input, setting flip-flop U670A. The $\overline{\text{Q}}$ output of U670A is then LO, and a B Sweep is started by reverse biasing Q709 in the B Miller Sweep as before.

Alternate Display Switching Logic

The Alternate Display Switching Logic circuitry controls both the Nonstore Horizontal Amplifier sweep switching and the Nonstore Z-Axis Logic switching for A Inten and B Only traces. The B Sweep ramp and gates are produced for every A Sweep when the HORIZONTAL MODE is set to either ALT or B. In ALT, the intensified zone on the A Sweep trace is shown for one B Sweep interval, and during the next A Sweep interval, a B Sweep trace is displayed during the B Sweep interval. For B Only traces, the A Sweep must still run to produce the A gating signals used throughout the circuitry for timing, but it is not displayed.

HORIZONTAL MODE switch S648 selects the input logic levels that drive the display switching circuitry. In the A Horizontal mode, the Set input of U670B is LO, and the Reset input is HI. This holds U670B reset with the A DISP signal HI, passing only the A Sweep to the Horizontal Amplifier (by the A Sweep selection transistor, Q742, located on Diagram 7). In the B Horizontal mode, the set input of U670B is HI, and the reset input is LO. This holds U670B set with the B DISP signal HI, allowing only the B Sweep to reach the Horizontal Amplifier (via the B Sweep selection transistor, Q732).

With S648 set to ALT, and for all settings of the VERTICAL MODE switches except BOTH-ALT, the $\overline{\text{VALT}}$ signal applied to U660E is HI and the Set and Reset inputs of U670B are both LO. The LO out of U660E causes the output of U680B to be HI. Each HI to LO transition of the ALT SYNC signal applied to pin 1 of U680A causes the NAND-gate output at pin 3 to change from LO to HI, clocking U670B. The Q and $\overline{\text{Q}}$ outputs of U670B therefore toggle, and the A DISP and B DISP signals cause the sweep selection transistors (Diagram 7) to alternately pass the A and B Sweep signals to the Horizontal Amplifier.

When the CH 1-BOTH-CH 2 VERTICAL MODE switch (S550) is set to BOTH, the ADD-ALT-CHOP switch (S545) becomes active. In the ALT VERTICAL MODE position, the $\overline{\text{VALT}}$ signal is LO, the HALT signal is HI, and the CH 1 SELECTED signal is a TTL square-wave signal that switches states at the end of the A Sweep. Input pin 4 of U680B is HI, and the gate output is the inverted CH 1 SELECTED signal. This output signal is combined with the ALT SYNC signal by NAND-gate U680A to clock U670B. Whenever the ALT SYNC signal goes LO at the end of a sweep and the CH 1 SELECTED signal (at U680B pin 5) switches from LO to HI, U670B is clocked. Since only positive transitions on the clock input causes the flip-flop to change output states, two A Sweeps must occur to cause the flip-flop output levels to switch. Switching this way, the crt first displays two A Intensified Sweeps, then two Alternate B Sweeps.

SWP SEP. Whenever the B Sweep is selected to drive the Horizontal Amplifier, the Q output of U670B is HI. This HI goes to U665C pin 10 through Q683 and Q687, and since pin 9 is also HI, the $\overline{\text{SEP}}$ signal from U665C is LO to enable the A/B Sweep Separation circuitry (located on Diagram 3).

B Z-Axis Logic

The B Z-Axis Logic circuitry switches signal current levels to drive the Z-Axis Amplifier for the Nonstore B Sweep and the A Intensified Sweep displays. The current supplied is summed with the other signal inputs on the Z-DRIVE line to set the Nonstore display intensity levels.

With the HORIZONTAL MODE switch in the ALT position, pin 5 of U665B is HI. Then, the Q and $\overline{\text{Q}}$ outputs of U670B, the $\overline{\text{B GATE}}$ signal from the output of U665D, and the B INTENSITY potentiometer, set the intensity levels of the Nonstore A Intensified and B Sweep traces. When the A Sweep trace is displayed, the $\overline{\text{Q}}$ output of U670B is HI, and the Q output is LO. These output levels bias Q683 on and bias Q682 off. The collector voltage of Q683 reverse biases CR817 to stop Z-Axis drive current from flowing through the diode. With CR683 reverse biased, additional Z-Axis drive current to intensify the A Sweep is supplied whenever CR685 is biased off by the gating action of U665B. Since input pin 5 of U665B is HI, the gate output and therefore the conduction state of CR685 is set by the B GATE signal from U660C. While the B GATE is HI, the output of U665B is LO, and CR685 is biased off to add B INTENS current to the Z-DRIVE line via CR816. During periods that the B GATE is LO (B Sweep not running), the output of U665B is HI, and CR685 is biased on. Diode CR816 becomes reverse biased, and the extra current that was being supplied to the Z-DRIVE line to intensify the A Sweep is removed.

With the Q and $\overline{\text{Q}}$ outputs of U670B switched to display the B Sweep ($\overline{\text{Q}}$ LO and Q HI), Q683 is biased off, and Q682 is biased on. The collector voltage of Q682 reverse biases CR816 to block any Z-Axis drive current from being supplied through that diode. With CR687 off, the B Sweep is displayed if CR680 is reverse biased. During the B Sweep interval, the $\overline{\text{B GATE}}$ output at pin 11 of U665D is LO. Diode CR680 is then reverse biased, and Z-Axis drive current from B INTENS flows through CR817. If the B Sweep is not running, the $\overline{\text{B GATE}}$ output of U665D is HI. That HI forward biases CR680 and reverse biases CR817. No B Z-AXIS drive current flows through CR817.

HORIZONTAL

The Horizontal Amplifier circuit, shown on Diagram 7, provides the signals that drive the horizontal deflection plates of the crt. Signals applied to the Horizontal Preamplifier may come from either the A or the B Miller Sweep Generator (for sweep deflection) or from the XY Amplifier (when Nonstore X-Y display mode is selected). A and B Sweep switching is controlled by signals from the Alternate Display Switching Logic circuit discussed earlier. Either the Nonstore sweeps or the Storage horizontal deflection signals are passed to the Horizontal Output Amplifier via a diode gating circuit. Signal selection by the Horizontal Mux circuit is controlled by the Channel Switch Logic output signals (located on Diagram 2). See Figure 3-6 for the block diagram of the Horizontal Amplifier.

The Horizontal POSITION control, X10 Magnifier circuitry, and the horizontal portion of the Beam Find circuitry are also part of the Horizontal Amplifier circuitry.

Horizontal Preamplifier

The Horizontal Preamplifier switches the Nonstore horizontal drive signals and amplifies input signals for application to the Horizontal Output Amplifier.

The A and B Sweeps are applied to the emitters of Q732 and Q742, through Sweep Gain potentiometers R730 and R740. Switching of the A and B Sweeps is controlled with these transistors. Using the A DISP and B DISP signals obtained from the Alternate Display Switching Logic circuitry (Diagram 6), Q732 and Q742 are either biased into the active or cutoff regions via CR732 and CR742. The POSITION control (R726) horizontally adjusts the crt trace position by supplying a variable dc offset voltage, through pin 14, to the output of the preamplifier. The position offset voltage from the wiper of R726 also goes to the Vector Generator circuitry (Diagram 20) to horizontally position the STORE mode waveform displays. Readout displays are not affected by the Horizontal POSITION control. Preamplifier output bias current levels are set by R751 at pin 5, and frequency compensation for X-axis signals is provided by C751, connectd to pin 13.

Nonstore horizontal X10 Gain is set by the resistor network between pins 3 and 6 of U760. When the X10 Magnifier is on, S721 is closed, and the amplifier gain increases by ten times. Magnified timing accuracy is adjusted using X10 Gain potentiometer R754. MAG REGIS potentiometer R749 is adjusted for no horizontal shift at the center of the graticule as X10 Magnifier is switched on and off. A second set of contacts on S721 informs the Microprocessor whether X10 Magnification is off or on. The SEC/DIV readout is automatically set to the correct scale factor, and STORE mode waveforms are digitally modified to reflect X10 magnification.

X-Y Amplifier

The X-Y Amplifier amplifies the Nonstore Channel 1 signal (X-AXIS) from the Internal Trigger circuitry (Diagram 4) and passes it to the Horizontal Preamplifier.

When the Nonstore X-Y mode is selected, Q737 is biased on to place a HI on U760 pin 12 to internally disconnect the A and B Sweep and the HORIZ POS input pins. The $\overline{XY}$ signal line is LO, biasing Q756 off to let the X-AXIS signal drive the noninverting input of U758. The output of U758 is a combination of the X-AXIS signal on pin 3 and the Horizontal POSITION voltage applied to pin 2 via R758. The X-Axis deflection accuracy is adjusted by X-GAIN potentiometer R760. The single-ended X-AXIS signal at pin 11 of U760 is changed to a differential signal at the preamplifier output pins. The differential signal is passed through the Horizontal Mux circuit to the Horizontal Output Amplifier for final amplification. When the X-Y mode is not selected, Q756 is biased on, and the X-AXIS signal is shunted to ground through the transistor.

Horizontal Output Amplifier

The Horizontal Output Amplifier provides final amplification of the horizontal Nonstore sweep signals or the Store mode deflection signals to drive the horizontal crt deflection plates.

In NONSTORE mode, signals from the (+) and (−) SWP outputs of U760 drive the Horizontal Output Amplifier. In STORE mode, horizontal LH OUT or RH OUT deflection signals are passed through the diode gate to drive the amplifier. Drive signals for STORE mode and readout character displays are selected by the Display Controller. Either Nonstore sweeps or Store deflection signals are selected by the diode gating using signals from the Store/Nonstore Multiplexer (U7201 on Diagram 2) through inverters U7202A and U7202B.

The selected signals drive a differential shunt-feedback amplifier. Due to the feedback, the input impedance of the amplifier is low. The base voltages of Q770 and Q780 are biased at nearly the same dc level by forward-biased diodes CR765 and CR768 located between the two emitters.

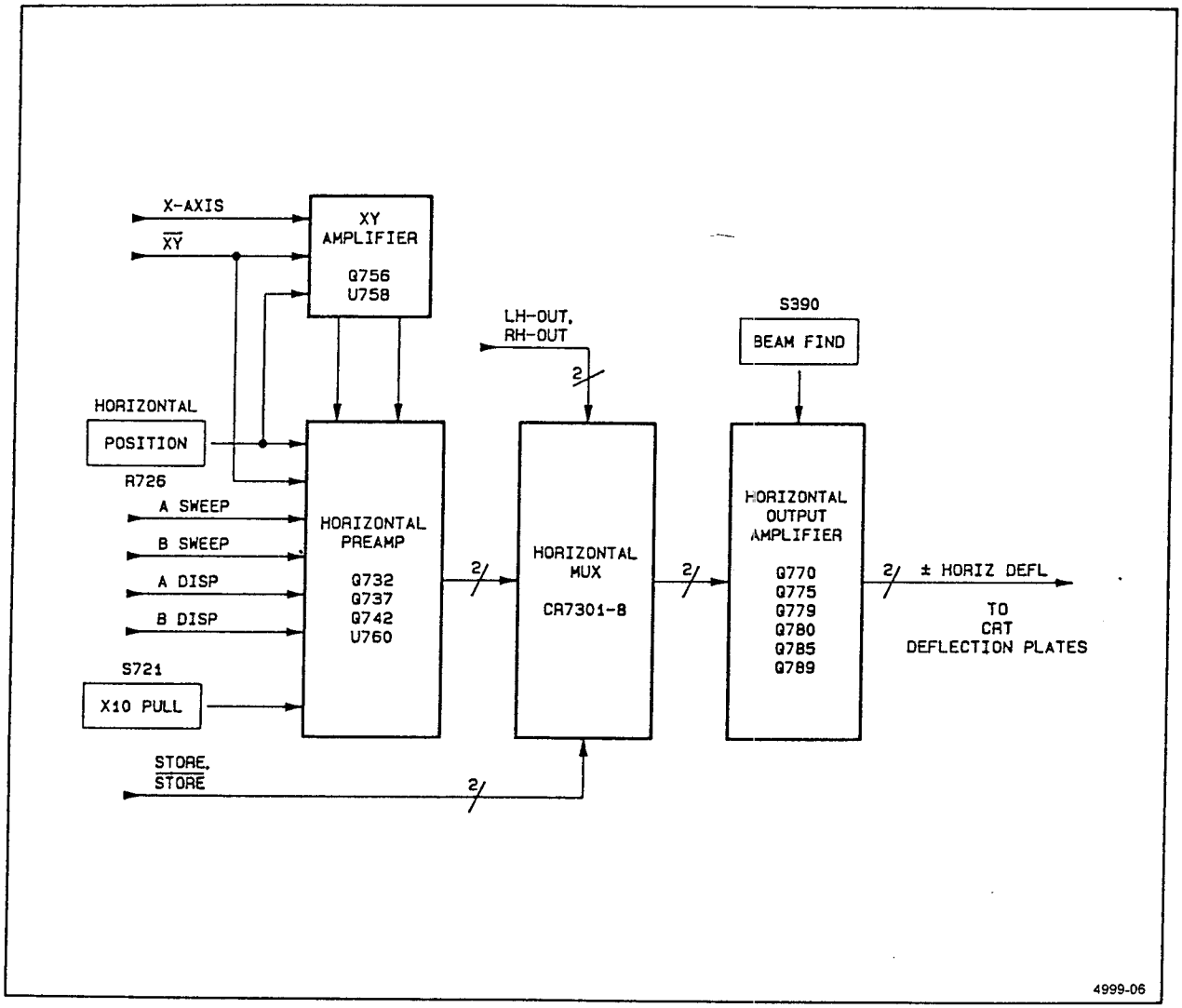


Figure 3-6. Horizontal Amplifier block diagram.

Transistors Q770, Q775, and Q779, as one-half of the complementary differential circuit, form a cascode-feedback amplifier for driving the right crt horizontal deflection plate. Amplifier gain is set by R775, with C775 providing high-frequency compensation. For low-speed signals, Q779 serves as a current source for Q775. At high sweep rates, the deflection signal is coupled through C779 to the emitter of Q779 to provide added pull-up output current to drive the crt. The amplifier formed by Q780, Q785, and Q789 drives the left crt horizontal deflection plate in the same manner as described above, with zener diode VR782 shifting the collector signal level of Q780 to the correct level to drive the emitter Q785.

The BEAM FIND function is active when S390 is pushed in to disconnect the cathode of CR764 from the −8.6 V supply. The voltage on the cathode of VR764 goes positive, causing CR780 and CR770 to be forward biased. Current from R764 causes the output common-mode voltage of the two shunt-feedback amplifiers to be shifted negative to reduce the available voltage swing at the crt plates. This stops the trace from being deflected off-screen horizontally. The BEAM FIND voltage also goes to the Vertical Output Amplifier, and the vertical deflection is limited in that circuit when the voltage is removed.

A circuit formed by Q7501 and Q7502 supplies reference voltages for the 1 K and 4 K storage acquisitions and for the variable SEC/DIV control, R721. Transistor Q7502 provides a 0.6 V drop from the −8.6 V supply to generate a −8 V reference for the 1K REF and one end of potentiometer R721. The 4K REF is produced by Q7501 and is adjusted by using the RATIO ADJ potentiometer to set the correct ratio for the two reference voltages. This reference level also goes to the other end of R721. The wiper voltage of R721 is the HOR REF voltage for the A and B Sweep timing resistors in NONSTORE mode. In STORE mode, either the 1K REF or the 4K REF voltage level is applied to the A and B Sweep timing resistors. Switching between reference levels for the different modes is done by the Storage Panel ACQUISITION switches (located on Diagram 14).

Probe Adjust

The Probe Adjust circuitry, shown on Diagram 7, is a square-wave generator and diode switching network that produces a negative-going square-wave signal at PROBE ADJUST connector J9900. Amplifier U985 forms a multivibrator that has an oscillation period set by the time constant of R987 and C987. When the output of the multivibrator is at the positive supply voltage, CR988 is forward biased. This reverse biases CR989, and the PROBE ADJUST connector signal is held at ground potential by R990. When the multivibrator output switches states, and is at the negative supply voltage level, CR988 is reverse biased. Diode CR989 becomes forward biased, and the circuit output level drops to approximately −0.5 V.

MICROPROCESSOR AND STORE-PANEL CONTROLS

The Microprocessor, shown on Diagram 14, directs the operation of the Storage and digital circuitry in the oscilloscope by following firmware control instructions stored in the Microprocessor memory. The Store-Panel Controls are monitored by the Microprocessor to detect when a Storage operation is selected. The rest of the significant front-panel controls are monitored through the Front-Panel A-to-D converter and I/O interface circuitry. Circuit operation is then directed by the Microprocessor to perform the selected operation.

Microprocessor, Clock, and Timer

Microprocessor U9111 is the center of control activities. It has an eight-bit combination bidirectional data bus for information transfer and addressing (AD0 through AD7) and a 12-bit address bus for selecting the source or destination of the data transfers (A8 through A19). Precise timing of instruction execution, addressing, and data transfer is provided by an external, crystal-controlled oscillator, shown on Diagram 18 and Clock Generator U9104.

A divide-by-three circuit in Clock Generator U9104 reduces the 20 MHz external input from the crystal oscillator circuit to 6.7 MHz for clocking the Microprocessor. An output from the 6.7 MHz clocking signal also drives the Display Controller (U9208 on Diagram 15) to time those devices. Another clock signal (PCLK) output, at one-half the Microprocessor clock frequency (3.3 MHz), is supplied to the input to U9108, a binary ripple counter that produces a lower frequency timing signal. The 6.7 MHz signal is also included in the Control Bus to provide a clocking signal for future options.

The RESET output of U9104 provides a power-on reset signal under normal operation or a manual reset using jumper connector P9104. The $\overline{\text{RES}}$ voltage level at pin 11 is held below the switching threshold of an internal Schmitt Trigger circuit after the power is applied for a time period set by the RC time constant of R9107 and C9107. This holds the Microprocessor in the reset state until the power supply voltages are high enough to permit normal operation of the digital circuitry. The Microprocessor is held reset during the delay period. Manually moving jumper P9104 to the RESET position forces a reset of the Microprocessor and the Display Controller.

The only RAM available for general use is the Display RAM. It's access is mediated by the Display Controller and associated circuitry. To allow the Display Controller to have first priority access to the RAM, the RDY1 input to the clock generator is used to tell the Microprocessor to wait for access to the RAM.

In addition, when one of the Communication Options is installed, the RDY1 input (U9104 pin 4) is used to synchronize the operation of the Microprocessor with the asynchronous activity of the GPIB (General Purpose Interface Bus) or RS-232-C Options for parallel or serial data transfer via the external communications port.

Resistor pack R9113 is a data bus pull-up. During normal operation, the resistor pack generates the interrupt vector pointer. During the hardware kernel test, the resistor pack generates the NOP instruction.

Latch and Buffer

Addressing is done using dedicated address bus lines. Address latch U9112 demultiplexes the address bus (separates the address and data bytes). When an address is valid, the Microprocessor sets the address-latch enable (ALE) HI (U9111 pin 25). Both U9112 and U9114 are clocked to latch the address bits. The latched bits are held until the Microprocessor places a new address on the busses and again sets the ALE signal HI. Some bits passing through U9114 have status information multiplexed with the address, so U9114 also functions as a demultiplexer.

Decoder

In addition to providing specific addresses to internal locations within memory devices, the addresses are decoded to provide enabling signals for blocks of addresses and to control the selection of I/O (Input/Output) devices. Table 3-1 shows the instrument's memory map.

In normal operation, address block decoder U9106 is always enabled. One-half of the dual 1-of-4 decoder looks at address bits A14 and A15. Latched address bits A18 and A19 from U9114 are looked at by the second half of the device.

I/O address decoding is performed by U9105. To perform its decoding, it must be enabled by the decoded output of U9106. The lower half of U9105 is controlled by a logic gating circuit formed by U9101D, U9102A, and U9102D. The lower half becomes enabled when either $\overline{RD}$ or $\overline{WR}$ is Low and BLOCK-0 and IO SEG are both LO. The upper half of U9105 is enabled only when address bits A12 and A13 are both HI, setting pin 9 of U9105 LO.

ROM

The operating system firmware is contained in two 64K by 8-bit read-only memories (U9110 and U9109). Immediately after the power-up reset ends, the Microprocessor automatically fetches the first command from the reset vector (address 0FFFF0), and begins program execution. Other interrupts to the Microprocessor cause vectoring to addresses that start the interrupt handling routines. The NMI (non-maskable interrupt) vector is at 00008, and the Maskable Interrupt (INTR) is vectored to 03FC (both interrupt vectors are in RAM).

Store Panel Controls and Buffer

The open or closed position of the Storage Panel Controls is passed to the Microprocessor via two octal bus drivers, U9301 and U9302. Each bus driver transfers eight individual data bits to the data bus when enabled. Enabling of the bus drivers is done by address line A2, which goes to both drivers, and decoded input/output enabling lines, going separately to each driver. Both enabling inputs must be LO on each IC to pass the input data bit to the data bus.

The Microprocessor communicates with the other devices on the data bus via Octal Bus Transceiver U9113. Two signals from the Microprocessor control enabling of the Transceiver and direction of the data flow. When the $\overline{DEN}$ signal is LO U9113 is enabled for transfers, and the $DT/\overline{R}$ signal sets the direction of the transfer. $IO/\overline{M}$ qualifies the transfer to allow pull-ups to assert an interrupt number on the bus during interrupt cycles. While the address and data are available on the bus side of this transceiver, only the data time slot is used.

Non-Storage Front-Panel Controls

There are many front-panel controls that do two things at the same time; control the real-time scope mode, and tell the Microprocessor what is being selected or modified. These controls include the vertical position controls, the vertical gain controls, the A and B time per division controls, the three major trigger mode controls, the vertical coupling controls, the sweep mode control, and the delay-time control. In addition, the probe-coding ring is read to determine true Volts per Division. In addition to acting as the user interface to the Microprocessor, the 1K/4K and STORE/NON STORE switches select the reference voltage applied the A and B timing resistors in the Sweep Generator circuitry.

STATUS ADC AND BUS INTERFACE

Front-panel control settings and the operating status are passed to the Microprocessor via the Bus Interface. Digital signals that can be read directly as data bits are buffered onto the Data bus either via octal bus driver U6102 or U6103. Analog voltages are converted to digital data bytes by analog-to-digital converter U6105. The analog signals are multiplexed to a buffer amplifier either by

Table 3-1

Memory Space Allocation

Block Designation	Block Address (Hex)	Space Allocation Purpose
RAM SEG	00000-3FFFF	**Four images of Memory Segment 0**
RAM Primary	00000-07FFF 08000-0FFFF	8-bit display RAM—waveforms, interrupt vectors, miscellaneous. 4 bits of display RAM for waveform attributes (LSB).
	10000-3FFFF	RAM Images.
IO SEG	**40000-7FFFF**	**Four images of Memory Segment 1**
IO Main Image	4067C (IO-2 A7,8) 406BC (IO-2 A6,8) 406F0 (IO-2 A3,8) 406F1 (IO-2 A3,8) 406F2 (IO-2 A3,8) 406F3 (IO-2 A3,8) 406F4 (IO-2 A3,8) 406F5 (IO-2 A3,8) 406F6 (IO-2 A3,8) 406F7 (IO-2 A3,8) 406F8 (IO-2 A2,8) 407DE (IO-2 A5) 407EE (IO-2 A4)	Option Status Latch (in). Option Parameters Latch (in). Option UART/GPIB chips (I/O). Option UART/GPIB chips (I/O). Option UART/GPIB chips (I/O). Option UART/GPIB chips (I/O). Option UART/GPIB chips (I/O). Option UART/GPIB chips (I/O). Option UART/GPIB chips (I/O). Option UART/GPIB chips (I/O). Option Interrupt Mask Latch (out). Time Base Mode Register U4119. Time Base Divider Register U4113.
	41XXX ($\overline{\text{INT-RST}}$) 42XXX ($\overline{\text{FRAME}}$)	Display chip interrupt reset. Display chip next frame.
	4377E (IO-0 A7) 437BE (IO-0 A6) 437DE (IO-0 A5) 437EE (IO-0 A4) 437F6 (IO-0 A3) 437FA (IO-0 A2)	Acquisition Memory Address Buffer Low bits U3427. Acquisition Mode Register U3310. B Delay Timer U4123. Record Counter U4115 and U4116. Front Panel A/D control U6104. Front Panel A/D data U6102.
	4377F (IO-1 A7) 437DF (IO-1 A5) 437EF (IO-1 A4) 437F7 (IO-1 A3) 437FB (IO-1 A2)	Acquisition Memory Address Buffer high bits U3428. B Delay Timer U4124. Record Counter U4117. Clock Delay Timer U4231. Main Front Panel Input U6103.
	43FFA (IO-0L A2)	Front Panel Buffer U9301.
	43FFB (IO-1L A2)	Front Panel Buffer U9302.
	48000-4BFFF	Acquisition Memory—Four images of Acquisition RAM U3418 and U3419.
IO Duplicate Images	50000-7FFFF	
COMM SEGMENT	**80000-BFFFF**	**Two images of Memory Segment 2**
Option Main Image	80000-87FFF 88000-8F7FF 8F800-8FFFF 90000-97FFF	Half of Communication Options ROMs U1243 or U1343. Option nonvolatile RAM. Nonvolatile RAM. Half of Communication Options ROMs U1243 or U1343.

Table 3-1 (cont)

Block Designation	Block Address (Hex)	Space Allocation Purpose
Option Duplicate Image	98000-BFFFF	
ROM SEGMENT	**C0000-FFFFF**	**Two images of Memory Segment 3**
ROM Duplicate Image	C0000-DFFFF	
ROM Main Image	E0000-E7FFF	System ROM 0—Low half of U9109.
	E8000-EFFFF	System ROM 1—Low half of U9110.
	F0000-F7FFF	System ROM 0—High half of U9109.
	F8000-FFFFF	System ROM 1—High half of U9110.

U6106 for the Vertical status signals or by U6101 for the Horizontal Status signals. The multiplexers are controlled by the Microprocessor via the control bits latched into U6104. The buffer amplifier output drives the input to the ADC. The converted data from the ADC is buffered onto the data bus by U6102.

STORAGE ACQUISITION

The Storage Signal Acquisition system, shown on Diagram 16, selects the channel or channels for digitizing, samples the signals at clock controlled intervals, and digitizes the samples. The circuitry consists of an analog Channel Switch, a Sample-and-Hold circuit, and the Analog-to-Digital Converter. A Strobe Generator drives the sampling circuitry diode bridge at the $\overline{\text{ADCLK}}$ rate (20 MHz) for all acquisition modes.

Channel Switch

With STORE mode selected, both channel signals are applied to analog Channel Switch U2101 where they may be selected for digitizing. Signals are selected by the $\overline{\text{CHAN1}}$ or the ADD signals from the Acquisition Memory, shown on Diagram 11. The $\overline{\text{CHAN1}}$ signal is derived from the delayed SAVECLK so channel switching takes place at the proper times for the A/D conversion. Both sides of the Channel Switch conduct in ADD Mode, summing the two input signals at the output. See "Channel Select" in the Acquisition Memory discussion for details on channel selection signals.

Differential channel signals are applied to the bases of a pair of transistors within the Channel Switch, at pins 2 and 15 for Channel 1 and pins 7 and 10 for Channel 2. Gain setting and compensation networks are connected between the emitters of both differential pairs in the emitter current source path. A gain setting potentiometer (R2118 for Channel 1 and R2108 for Channel 2) sets the acquisition gain for each channel. Thermistors RT2101 and RT2111 temperature compensate the gain of the circuit. Diodes CR2111 and CR2112 temperature compensate the gain of the circuit at high frequencies. Capacitors C2103 and C2113 set the high-frequency peaking.

The Channel 1 amplifier base biasing voltage is supplied via R2122 and the input termination resistors, R2121 and R2120. The termination resistors provide the proper impedance match between the signal lines from the Vertical Preamplifiers (Diagram 2) and the high impedance inputs of the Channel Switch. Corresponding resistors in the Channel 2 amplifier perform the same job for Channel 2. Selection of the channels is controlled by the inputs at pin 4 and pin 14. The $\overline{\text{CHAN1}}$ signal biases on the Channel 1 differential amplifier pair when LO and the Channel 2 differential amplifier pair when HI. The logic level of $\overline{\text{CHAN1}}$ is toggled at the proper rate to provide dual-channel operation. Diodes CR2103 and CR2104, and resistors R2128 and R2129 level shift $\overline{\text{CHAN1}}$ to the level required by U2101.

For ADD Mode, the $\overline{\text{CHAN1}}$ signal is held LO and the ADD signal applied to pin 14 is switched HI by the Microprocessor via Acquisition Mode Register U3310, shown on Diagram 17, biasing on both the Channel 1 and the Channel 2 amplifiers. The resulting output current is the sum of the input signals applied to Channel 1 and Channel 2. Diodes CR2101 and CR2102, and resistors R2126 and R2127 level shift ADD to the level required by U2101.

The differential output current from the Channel Switch (pins 12 and 13) is converted to a single-ended voltage for application to the sampling circuitry. An amplifier stage composed of Q2101, Q2102, Q2103, Q2104, Q2105, Q2106, and associated circuitry performs the conversion.

Common-base transistors, Q2101 and Q2102 form a differential amplifier that presents a low-impedance load for the Channel Switch. Offset is adjusted (using potentiometer R2138) to match the store display with the non-store display. Thermistor RT2131 temperature compensates the offset. Output current from the collector of Q2102 is applied to the base of Q2103, a shunt-feedback inverting amplifier. The inverted output signal voltage is developed across R2146 in the collector circuit. The output signal of Q2101 is developed across R2147 in series with the signal at the collector of Q2103 to produce a single-ended replica of the differential input signal at the base of Q2105. Transistor Q2104 and its associated biasing resistors provide a constant-current bias source for Q2101, Q2102, and Q2103.

Emitter-followers Q2105 and Q2106 provide the necessary signal drive and impedance matching to the Sample-and-Hold diode bridge. Transistors Q2150 and Q2107 and associated circuitry clamp the signal level to −2.5 V and +1 V respectively at the sample and hold input.

Sample-and-Hold

A sampling diode bridge formed by CR2203 is biased on by a strobe from the Strobe Generator. The bridge is biased off during the hold period while the Analog-to-Digital Converter (ADC) is converting the last sample. When the bridge is strobed on, Hold capacitor C2235 is charged to the new analog level present at the input to the bridge. The bridge becomes biased off when the strobe passes, and the voltage on the hold capacitor is held until the next sample is taken. Signal samples are buffered by a high-impedance input FET amplifier and coupled to the ADC via an emitter-follower amplifier that provides the input of the ADC with a low-impedance source. FET Q2209B, with its source and gate connected together, supplies source current to Q2209A. A constant-current load for the emitter-follower is provided by Q2211 and its associated biasing resistors.

Strobe Generator

The ECL (Emitter-Coupled Logic) circuit formed by U2203A, B, and C produces two pairs of complementary control signals. One pair drives the sample strobe circuit to bias the sampling diode bridge on, and the other clocks the ADC. The 20 MHz $\overline{\text{ADCLK}}$ clock from the Clock Generator circuit (Diagram 18, Digital Timebase) is shifted to ECL levels by the voltage divider formed by R2265, R2266, and R2267. Capacitor C2224 improves the high-frequency characteristics of the divider string, and R2268 limits the input current to U2203C. OR/NOR-gate U2203C produces the complementary ECL clocks to the ADC.

The sample-bridge strobe pulse is developed from the ADC clock signals by U2203B, U2203A, and the RC circuit composed of R2270 and C2225. The uninverted output of U2203C ($\overline{\text{CLK A/D}}$) is applied to pin 4 of OR/NOR-gate U2203A where its signal transitions are seen immediately. The inverted output of U2203C (CLK A/D) must charge C2225 (through R2270) to the switching threshold of U2203B before U2203B can switch state and change the state of input pin 5 of U2203A. When a HI-to-LO transition occurs on pin 4 of U2203A, the output at pin 3 goes HI and pin 2 goes LO to follow the input signal. A short time later, the charge on C2225 reaches the switching threshold of OR-gate U2203B, and the output of that gate goes HI. That HI switches the output at pin 3 of U2203A back LO and pin 2 back HI. The total duration of the pulse is approximately 10 ns. Pin 4 of U2203A switches from LO to HI on the next transition of $\overline{\text{ADCLK}}$, and after a short delay the output of U2203B goes LO again, readying the circuit for the next pulse.

The complementary sample strobes are applied to opposite bases of a current-mode switch formed by Q2208 and Q2207. The amplified output is coupled to the sampling diode bridge biasing circuit by T2201 and T2202, a common mode transformer. Transformer coupling prevents any dc offsets from entering the bridge via the biasing circuit by completely isolating the bias voltage from the signal voltage. The ECL output lines are terminated by R2278 and R2277 at the differential switch. The resistors match the characteristic impedance of the transmission path to prevent reflections that occur when the signals are not properly terminated. Common mode transformers T2202 and T2203 improve the symmetry of the strobe pulses so that, when the pulses are combined at CR2203, the pulses will cancel each other out and not show up as noise in the signal.

When the sample strobe is being amplified, the polarity of the pulse on pin 6 of T2201 is positive. The sampling strobe path is through C2229, C2230, and T2203 to forward bias CR2203. Signal current then flows through the forward biased diodes to charge Hold capacitor C2235. At the end of the strobe the polarity changes across pins 6 and 1 of T2201. The voltage on C2229 and C2230 increase the reverse bias on the bridge during the off time. R2281 and the duty cycle of the strobe determine the charge on C2229 and C2230.

Analog-to-Digital Converter

Analog-to-Digital Converter U2204, converts analog input voltages in the range of 0 V to −2 V into 8-bit digital representations. The digital output code for 0 V is 11111111 and 00000000 for −2 V. Conversions are continually taking place at 20 Megasamples per second (the $\overline{\text{ADCLK}}$ rate) regardless of the SAVECLK rate. The ADC is

a high-speed ECL device having ECL compatible open-emitter outputs. Pull-down resistors to the −5 V supply are in resistor pack R2295. The ECL output levels are converted to TTL levels by U2205 and U2206 and placed on the C-DATA BUS.

An external voltage reference for the ADC is generated by a circuit composed of operational amplifier U2202B and Q2213. The +5 V reference voltage is converted to a current by R2259 and applied to the inverting input of U2202B. An extra current source is provided from the +8.6 V supply via R2260 to reduce loading on the +5 VREF. The closed-loop gain of the stage is −0.4 for an output voltage of −2 V at the emitter of Q2213.

ACQUISITION MEMORY

The Acquisition Memory system, shown on Diagram 17, controls the movement of the digitized data from the A/D Converter to the Acquisition Memory. The acquisition mode controls the way the transfer occurs. Data may be transferred directly to memory through the MIN/MAX registers as either Odd and Even data for a single channel acquisition or Channel 1 and Channel 2 data for dual-channel acquisitions. In the Min-Max Mode, a certain number of data samples are compared for the highest and lowest amplitude during the comparison period. The maximum and minimum data values are transferred to the Acquisition Memory.

Data is transferred through the A/D Buffer, the MIN/MAX Registers, the Swap Registers, and finally into Acquisition Memory in a pipeline fashion. Waveforms are constantly sampled and digitized at the ADCLK rate, then the resulting data byte representing the value of each sample is latched into the A/D Buffer if the CONV clock is 20 MHz. Each succeeding sample clocked into the A/D Buffer follows the previous data sample through the digital devices of the acquisition system. Acquisition control clocks that are copies of the SAVECLK with various delays handle the data transfer timing.

A/D Buffer

A data byte from the A/D Converter is latched into A/D Buffer U3229 on the rising edge of the convert (CONV) clock. The data is immediately available on the G data bus during normal operation because the buffer is enabled by a HI from NAND-gate U3426D.

For testing and diagnostics purposes, the $\overline{\text{TEST}}$ signal on pin 12 of NAND-gate U3426D is made LO by the Microprocessor via the Acquisition Mode Register. That isolates the A/D Buffer from the bus and enables the Diagnostic Code Generator to place data on the G data bus to the MIN/MAX Registers.

MIN/MAX Registers

Data is latched into the MIN/MAX Registers in four different ways depending on the acquisition mode. The MINCLK and MAXCLK clocking signals are selected by MIN/MAX Clock Selector multiplexer U3309. The mode selected determines the actual clock signals that latch data into the MIN/MAX Registers.

For Sampling mode, the data is latched by ODDCLK and $\overline{\text{ODDCLK}}$ to place either odd and even data from a single channel or Channel 1 and Channel 2 data from both channels into the registers. The timing of the data bytes is evenly spaced in sampling mode (see Figure 3-7).

In X-Y mode for 20 μs per division and slower, both channels are chopped to obtain the horizontal and vertical deflection signals. The $\overline{\text{EVENCLK}}$ signal clocks the MIN Register and $\overline{\text{ODDCLK}}$ signal clocks the MAX Register. Selecting these clocks makes the time difference between the two samples 100 ns. The last possible sample in a Channel 1 SAVECLK period and the first possible Channel 2 sample are saved as a pair. X and Y data are then separated by one CONV clock period rather than the longer (possibly much longer) SAVECLK clock period.

Min-Max mode generates the last two clocking modes. The first is the Min-Max Initialization mode. For initialization, the first data sample in a SAVECLK period is latched into both the MIN and the MAX Registers at the same time. This is the sample with which the remaining samples taken during the SAVECLK period are compared. After storing the initial data sample, the MIN/MAX Clock Selector multiplexer (U3309) is switched. It then passes the NEWMIN and NEWMAX signals from the data Comparators, U3233 and U3235, to clock the MIN/MAX Registers.

COMPARATORS. Data bytes latched into the MIN/MAX Registers are compared with each new data byte latched in the A/D Buffer. If the data value is either lower than the present data in the MIN Register or higher than present data in the MAX Register, the appropriate Comparator output pin goes HI. The comparison takes some time after the clocking signals, so the MIN/MAX Clock Selector Multiplexer is disabled from passing the NEWMAX or NEWMIN until the CONV clock goes LO. By that time, the comparator outputs have stabilized. If a NEWMAX or NEWMIN has occurred, the new data byte is latched into the appropriate register one-half a CONV clock cycle after the data was latched into the A/D Buffer.

The Min-Max data comparisons for each saved data byte continue for the duration of the SAVECLK period. The minimum number of samples compared is 4 at 20 μs per division. This corresponds to the number of CONV clock periods possible at the fastest SAVECLK rate (a

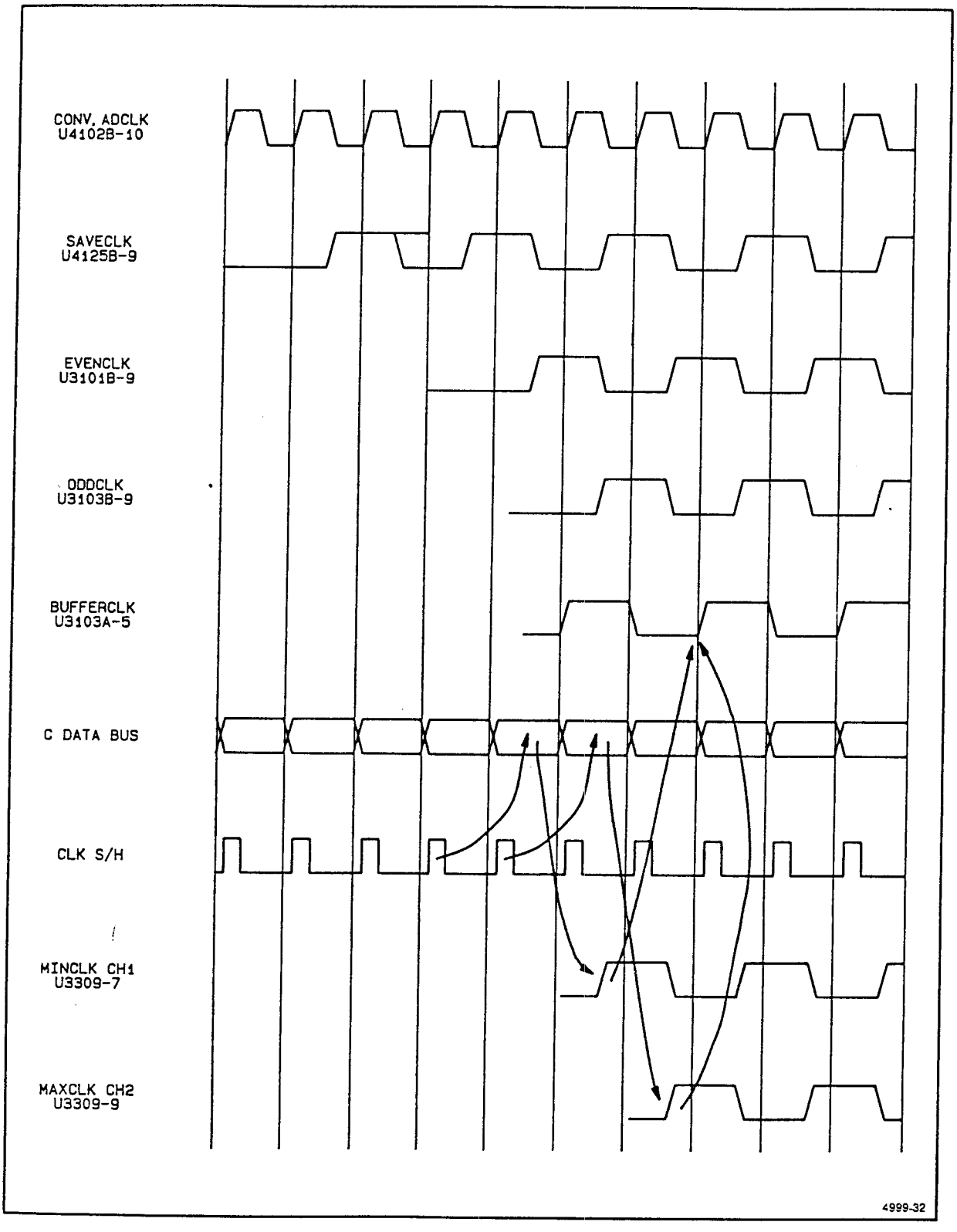


Figure 3-7. Sampling mode acquisition timing at 0.05 μs per division (ADCLK=CONV=20 MHz).

function of the SEC/DIV switch setting). As the SAVECLK period increases with slower SEC/DIV switch settings, the number of samples compared to find a min and a max per SAVECLK period also increases.

MIN-MAX OUTPUT. One CONV clock period before the end of the SAVECLK period, the ACQWRITE signal gives write control of the Acquisition Memory to the acquisition system (see Figure 3-8). If SWAPEN (U3320 pin 13) is HI, either SWAP (U3313A pin 3) or $\overline{\text{SWAP}}$ (U3313B pin 6) becomes TRUE (depending on whether the last sample was a NEWMAX or a NEWMIN) at one-half a CONV clock period before the end of the SAVECLK to enable the output of one set of the Swap Registers onto the memory data buses. At the same time, BUFFERCLK (U3103A pin 5) goes HI to clock the last Min and Max data from the MIN/MAX Registers into and through the Swap Registers onto the memory data buses where the data is written into the Acquisition Memory. All 16 bits of the Min and Max data are transferred into memory in parallel. This 16-bit transfer also holds true for Odd and Even or Channel 1 and Channel 2 data bytes when those signals are being sampled.

Acquisition Mode Register

The Acquisition Mode Register controls the manner in which data is transferred through the acquisition system from the A/D Buffer to the Acquisition Memory. Outputs of the MIN/MAX Clock Selector multiplexer, U3309, were discussed in the description of the MIN/MAX Registers. The control signals for switching the multiplexer and selecting which set of Swap Registers are enabled when transferring data to the Acquisition Memory are described in this part. The mode selection control of the MIN/MAX Clock Selector multiplexer is shown in Table 3-2.

Table 3-2

MIN/MAX Clock Selector Multiplexer Switching

MODE	Control Input 0	Control Input 1	Input Selected
MIN/MAX INIT	1	1	3
MIN/MAX	0	1	2
SAMPLING	1	0	1
SAMPLING XY	0	0	0

Multiplexer switching is controlled by the MIN/MAX and $\overline{\text{XY}}$ signals from the Acquisition Mode Register U3310 (sent by the Microprocessor) and the state of the CONV clock. In MIN/MAX, the circuitry composed of U3306A and U3306B produces a 100 ns HI pulse at the beginning of each SAVECLK cycle to initialize the MIN/MAX Registers for making comparisons. Prior to entering the Min/Max mode, flip-flop U3306A is held in the Set state (reset is also LO, so both outputs of the flip flop are HI). Each rising CONV clock edge clocks the HI through flip-flop U3306B and pin 9 remains HI. With a LO MIN/MAX signal on control input 1 and a HI from flip-flop U3306B on control input 0, the multiplexer selects the sampling mode clocks (ODDCLK and $\overline{\text{ODDCLK}}$) to clock data into the MIN/MAX Registers.

When MIN/MAX (U3310 pin 14) goes HI, the set is removed from U3306A and the flip-flop becomes reset by the LO on pin 1. On the next rising edge of CONV, the LO is clocked through flip-flop U3306B, and the reset is removed from U3306A. On the next rising edge of EVENCLK, the fixed HI on the D input of U3306A is clocked through that flip-flop to the D input of U3306B. Then on the next rising edge of CONV, it is clocked to the Q output to make control input 0 of the multiplexer HI along with the MIN/MAX input on control input 1. The multiplexer will not yet pass the fixed HI inputs selected, because the outputs are not enabled. When CONV goes LO, AND-gate U4101C passes that LO to the enabling inputs of the multiplexer. The two input HI levels are then passed through the multiplexer to clock the same data byte into both MIN/MAX Registers. When CONV again goes HI, the multiplexer outputs become disabled, so the INIT clock to the MIN/MAX Registers last for only one-half of a CONV clock period.

When the HI was clocked to pin 9 of U3306B, pin 8 went LO, and U3306A became reset, placing a LO on its Q output. The next rising edge of the CONV clock clocks the LO through flip-flop U3306B, changing control input 0 of the multiplexer and removing the reset from flip-flop U3306A. The initialization pulse to control input 0 lasts for a period of one CONV clock; 100 ns in Min/Max mode. After initialization, the multiplexer switches to select the NEWMIN and NEWMAX outputs from the data comparators (U3233 and U3235) to clock the MIN/MAX Registers. The one-half CONV clock delay in enabling the multiplexer allows the outputs of the Comparators to settle when, on the next samples, the outputs of the comparators are used to clock the MIN/MAX Registers. A new initialization is started again on the next rising edge of EVENCLK (once for each SAVECLK).

The last Acquisition Mode is XY Sampling. The Microprocessor sets the MIN/MAX and $\overline{\text{XY}}$ signals LO at the Acquisition Mode Register (U3310). That places a LO on control input 1 of the multiplexer and enables the outputs through AND-gate U4101C. With $\overline{\text{XY}}$ LO, flip-flop U3306B is held reset, placing a LO on control input 0 of the Multiplexer. The MINCLK and MAXCLK are then the $\overline{\text{EVENCLK}}$ and $\overline{\text{ODDCLK}}$ signals respectively. These clocks produce the minimum possible time difference (100 ns) between the Channel 1 and Channel 2 data samples that are stored as a pair.

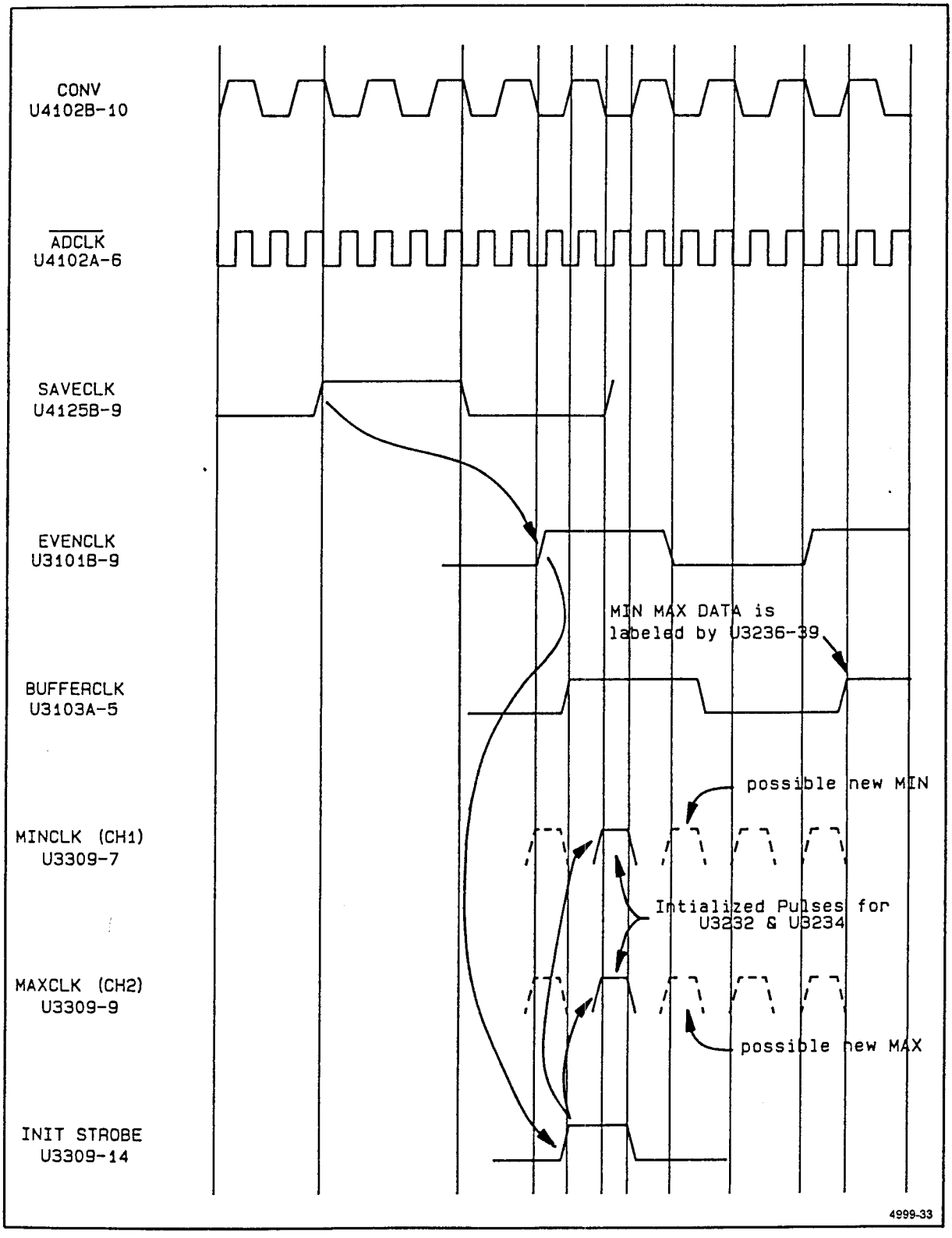


Figure 3-8. MIN/MAX Acquisition timing at 20 μs per division.

Another section of the circuitry is used in conjunction with the Min-Max Sampling mode to determine whether the last sample clocked into the MIN/MAX Registers was a NEWMIN or a NEWMAX. This knowledge is necessary in chopped Min/Max mode to place the Min and Max data samples into the Acquisition Memory in the correct order. Each Swap Register consists of two sets of two. The Min data is placed in both buffers of one set and the Max data in both buffers of the other set at the same time by the rising edge of BUFFERCLK. The outputs of one of the buffers in each set are connected to one of the memory data buses and the other half of the buffers are connected to the opposite memory data bus. Depending on which buffer in each set is enabled, the data is placed on the memory data buses by either the nonswapping buffers or the swapping buffers (controlled by enable signals SWAP and $\overline{\text{SWAP}}$).

When swapping is not enabled, as in sampling and X-Y modes, the SWAPEN signal from the Acquisition Mode Register (U3310) is LO, and flip-flop U3307B is held set. NAND-gates U3313B and U3313A have as one of their inputs the Q and $\overline{\text{Q}}$ outputs of the flip-flop respectively. With the flip-flop held set, NAND-gate U3313B is enabled to pass the DATAEN enabling signal to the nonswapping buffers only. In chopped Min/Max mode, swapping is enabled to place the Min and Max data in memory in the correct order. The SWAPEN signal is set HI and the reset is removed from flip-flop U3307B so that the latch circuit on the D input controls the SWAP/$\overline{\text{SWAP}}$ states.

At initialization in Min/Max mode, both MINCLK and MAXCLK (U3309) go HI for the first data byte. At the end of the initialization pulse, both inputs to the latch are removed by disabling the multiplexer outputs, and the output states of both NOR-gates (U3308C and U3308D) remain LO.

A MAXCLK or MINCLK signal going HI is accompanied by a LO on the opposite signal line. If the MINCLK signal goes HI, the accompanying LO on the MAXCLK line causes U3308C to change output state from LO to HI. That HI goes to pin 12 of U3308D, holding its output LO. No further switching of the latch occurs unless the MAXCLK signal goes HI. MINCLK going HI again will not cause any state changes in the latch. If MAXCLK goes HI, U3308D will change to a LO output state, and U3308D pin 13 will be latched HI. The state of pin 13 when the rising edge of BUFFERCLK occurs is clocked through flip-flop U3307B, enabling one of the NAND-gates that must pass the DATAEN enabling signal to the Swap Registers. If a NEWMAX (MAXCLK) occurred last, the Q output of U3307B will be HI and SWAP will be LO, enabling the nonswapping buffers, U3236 and U3239. If a NEWMIN (MINCLK) occurred last, pin 13 of U3308D will be LO. When that LO is clocked through U3307B, NAND-gate U3313B goes LO, passing and inverting the DATAEN enabling signal. That makes SWAP LO, and the swapping buffers (U3237 and U3238) are enabled, placing the Max data into the Acquisition Memory that the processor looks at to find the data that occurred last.

Acquisition Clock Decoder

The Acquisition Clock Decoder circuitry is composed of three parts. One part is a flip-flop delay chain that produces the transfer clocks. The output clocks from the chain are essentially copies of the SAVECLK delayed by successive CONV or $\overline{\text{CONV}}$ clock periods. The second part controls acquisition writes by producing the ACQWRITE and DATAEN clocks. The outputs of this portion switch control of the Acquisition Memory to the acquisition memory system. This enables the data from the Swap Registers onto the memory data buses so it can be written into memory. The final section of the clock decoder circuitry drives the analog Channel Switch to select the vertical channel signal to be digitized.

DELAY CHAIN. The first four of five flip-flops in the delay chain (U4104B, U3101A, U3101B, and U3103B) are clocked by $\overline{\text{CONV}}$ for delays through each of either 100 ns or 50 ns (10 MHz and 20 MHz CONV clock rates respectively). The various delays represented by the output clock lets data being transferred through each device in the acquisition pipeline settle at the outputs; and, in the case of Min-Max mode, be processed through the comparators before the next data byte is clocked in. The last flip-flop in the delay chain (U3103A) is clocked by CONV and produces a delay of one-half of a CONV-clock period between EVENCLK (U3101B) and BUFFERCLK (U3103A). Every rising edge of BUFFERCLK transfers both 8-bit data bytes from the MIN/MAX Registers into the Swap Registers and, in chopped Min-Max mode, clocks flip-flop U3307B in the Swap-Control circuitry. Flip-flop U3307B latches the last state of MINCLK and MAXCLK to determine which set of Swap Registers are enabled to pass data to the Acquisition Memory buses. See the "Acquisition Mode Control" description for additional information on Swap Register enabling.

ACQUISITION WRITE. Flip-flops U3105A and U3105B form a self-resetting circuit that produces the ACQWRITE signal once each SAVECLK period. The time duration of ACQWRITE is one $\overline{\text{WRITECLK}}$ period, either 100 ns or 200 ns (twice the CONV clock period) except at the fastest sampling rates when the SAVECLK is running at 10 MHz. In that case, once switched HI to write the first data into memory, ACQWRITE remains HI until $\overline{\text{ENDREC}}$ goes LO (a full record). The logic gating of U3104A, B, C, and D controls the reset line to U3105B.

Before the start of an acquisition, U3105A pin 1 is held LO by ACQENA. The LO keeps U3105A reset, putting a LO on U3105A pin 5 and U3104C pin 9. The LO on the input of NAND-gate U3104C causes the reset input of U3105B (pin 13) to be HI. This allows the next delayed SAVECLK to set U3105B. However before the start of an acquisition, SAVECLK is held LO, U3105B remains reset, the D input (pin 12) of U3105A is LO, and the $\overline{\text{WRITECLK}}$ signal continues clocking a LO to an already LO output of U3105A.

At the start of an acquisition, ACQENA goes HI on the reset input of U3105A. On the first rising edge of the delayed SAVECLK from U3101A pin 5, the fixed HI on the D input of U3105B is clocked through to place a HI on the D input of U3105A. On the next rising edge of $\overline{\text{WRITECLK}}$, that HI is passed to the Q output of U3105A and pin 9 of NAND-gate U3104C. Assuming a HI is present on pin 10 of the NAND-gate, the output at pin 8 goes LO, resetting U3105B, and on the next rising edge of $\overline{\text{WRITECLK}}$ the LO from the Q output of U3105B is clocked through U3105A to end the ACQWRITE pulse. The ACQWRITE pulse also removes the reset from U3105B so that the next time it is clocked (by the next delayed SAVECLK), a new ACQWRITE pulse is produced for the next Acquisition Memory write.

The ACQWRITE signal goes to the Memory Control multiplexer (U3417) to switch Acquisition Memory write control to the acquisition system and is also applied to the D input of flip-flop U3307A. One-half of a CONV clock period later, the rising edge of CONV transfers the HI to the DATAEN clock line at the Q output of the flip-flop. DATAEN going HI enables NAND-gates U3313A and U3313B in the Swap-Control circuitry to pass the SWAP and $\overline{\text{SWAP}}$ register enabling signals. That and BUFFERCLK going HI transfers the data from the MIN/MAX Registers onto the Acquisition Memory busses where it can be written into memory.

If the SEC/DIV setting is such that SAVECLK is running at 10 MHz, RNGA and RNGB will both be HI at the inputs to NAND-gate U3104D. That makes the output of U3104A also a HI. $\overline{\text{ENDREC}}$ goes LO only when an acquisition is completed with a full record. The output of U3104B is therefore LO, and U3104C is disabled, preventing a reset from being passed to flip-flop U3105B. When $\overline{\text{ENDREC}}$ does go LO, NAND-gate U3104C is enabled, and the reset is passed to U3105B. On the next rising edge of $\overline{\text{WRITECLK}}$, ACQWRITE is clocked LO, switching memory write control away from the acquisition system. When operating at the fastest SAVECLK rates, a pair of Swap Registers are enabled for the entire acquisition period to immediately transfer data clocked in by BUFFERCLK to the memory data buses.

CHANNEL SELECT. When only Channel 1 or Channel 2 is selected, the Microprocessor controls the choice via the Acquisition Mode Register. For Channel 1 only, the Microprocessor sets the $\overline{\text{CH1}}$ line LO, which sets U3102A and holds the $\overline{\text{CHAN1}}$ line LO. $\overline{\text{CHAN1}}$ switches the analog Channel Switch (U2101 on Diagram 16) to select and apply the Channel 1 signal to the Sample-and-Hold circuitry. Conversely, Channel 2 is selected when the Microprocessor sets the $\overline{\text{CH2}}$ line LO, which resets U3102A and holds the $\overline{\text{CHAN1}}$ line HI. When the signals from both channels are to be added for ADD Mode, the $\overline{\text{CHAN1}}$ signal line is held LO, and the ADD signal is held HI. This turns on both sides of the analog Channel Switch to sum the input signals.

For dual-channel acquisitions, both the set and reset input to flip-flop U3102A are HI, and channel switching is controlled by $\overline{\text{ADCLK}}$ and the logic circuitry driving the D input of the flip-flop. Channel switching is then determined by the acquisition mode and the range setting of the SEC/DIV switch. The channel switching is timed to place the switching point between ADCLK positive transitions (between sampling points) at the correct time for starting waveform data into the acquisition system pipeline.

Multiplexer U4103 (Diagram 18) is switched by the RNGA and RNGB signals from the Timebase Mode Register. For SEC/DIV settings of 0.05 μs to 10μs, CONV clock and ADCLK run at 20 MHz and are in phase. In that case, the SAVECLK signal phase is also correct for driving the analog Channel Switch. For the remaining SEC/DIV switch settings, the CONV clock runs at one-half the ADCLK clock rate, and the control clocks developed by the delay chain are delayed by 100 ns through each flip-flop rather than by 50 ns as at the faster SEC/DIV settings. Since this changes the delays of data going through the pipeline, a delayed SAVECLK is required to switch channels at the proper time. The 100 ns delayed SAVECLK from the Q output of U4104B is delayed another 25 ns, by the rising edge of $\overline{\text{ADCLK}}$, before reaching the output of flip-flop U3106A (Diagram 17).

Either the delayed SAVECLK from U3106A or SAVECLK is selected by the multiplexer and applied to the clock input of U3102B and to one input of NAND-gate U3112 (pin 2). When Min-Max mode is selected, flip-flop U3102B divides the selected clock by two. The channel is switched only once for each SAVECLK so that the samples compared for min and max during a SAVECLK cycle are all from the same channel.

When ACQENA on the reset input of U3102 is HI, the flip-flop is enabled to toggle on each rising clock edge. If Min-Max mode is also HI, NAND-gate U3313 is enabled to pass the signal from the Q output of the flip-flop. NOR-gate U3308, connected as an inverter, places a LO on

pin 1 of U3112A, and NAND-gate U3112 is disabled from passing the selected clock signal. U3112A puts a HI on pin 13 of U3112D, enabling U3112D to pass the divided clock signal to the D input of flip-flop U3102A. Rising edges of $\overline{\text{ADCLK}}$ transfer the inverted state of the signal at the D input of U3102A to the $\overline{\text{CHAN1}}$ signal line, switching the Analog-Channel Switch at one-half the SAVECLK frequency. In Sampling and XY Sampling Modes, MIN/MAX is LO. This disables U3313D, stopping the divided clock, and enables U3112 to pass the selected clock to the D input of U3102A. Then, the selected clock and $\overline{\text{CHAN1}}$ are the same frequency. Another 50 ns of delay is added when clocking through U3102A. The delay is present for either selected clock.

MEMORY CONTROL. Memory Control multiplexer U3417 selects the enabling and read-write signals that control the Acquisition Memory. When the ACQWRITE clock goes HI (see Figure 3-9), the multiplexer turns the memory over to the Acquisition System (1 inputs) to perform a write to memory. From the inverting multiplexer, the $\overline{\text{E}}$ enabling signal (pin 7) is a fixed LO that selects the Acquisition Memory devices for access. The $\overline{\text{G}}$ enabling signal (pin 4) is a fixed HI that disables the memory devices for outputting data. Writing to memory is controlled by the WRITECLK signal from the Clock Generator (Diagram 18). It becomes the $\overline{\text{W}}$ (write enable) on pin 9 and the ADDRCLK (memory address clock) on pin 12 of multiplexer (U3417). When the ACQWRITE signal switches the multiplexer, one-half a CONV clock period later, the Swap Registers are enabled onto the memory buses, transferring from the MIN/MAX Registers the samples that are to be stored. In another one-half CONV clock period, the data bytes have settled, and the memories are enabled for an acquisition write by the LO state of the second half period of WRITECLK. The WRITECLK falling transition increments the Address Counters to the address of the next location to be written to in memory.

For a memory read or memory write by the Microprocessor, the Memory Control multiplexer is switched to the $\overline{\text{1}}$ input signals. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (read and write control signals) from the Microprocessor control bus, determine if a read or write is to be done. Loading the Address Counter (U3423, U3424, and U3425), enabling the Microprocessor Data Transceivers (U3421 and U3422), and gating the control logic is done by the $\overline{\text{ACQSEL}}$ signal. The signal is the OR of the $\overline{\text{IO-SEG}}$ and $\overline{\text{BLCK2}}$ signals in the processor section. Both address selection signals must be LO to access the Acquisition Memory from the Microprocessor. The ADDRCLK signal from pin 12 of the multiplexer is a fixed HI that disables the Address Counters from counting while the Microprocessor is either reading from or writing to memory. The $\overline{\text{RD}}$ signal is inverted to pin 2 of the multiplexer by U3416A, and is again inverted to pin 4 by the multiplexer. When the memory is enabled for reading stored data, pin 4 is LO ($\overline{\text{RD}}$). The $\overline{\text{ACQSEL}}$ signal is inverted by U3416B and applied to pin 5 of the multiplexer. It is again inverted through the multiplexer to a LO, enabling the memory outputs onto the memory data buses. The $\overline{\text{WR}}$ signal is also HI to enable the memory for a read.

The Microprocessor writes to the memory only for diagnostics. $\overline{\text{WR}}$ and $\overline{\text{ACQSEL}}$ must both be LO at the inputs of U3420C to cause pin 9 of the multiplexer to be LO, enabling a memory write. The Address Counters are enabled for a parallel load of the selected memory address. Only one memory device at a time is read from or written to by the Microprocessor, because the microprocessor data transceivers that buffer data to and from the memory devices are never both enabled at the same time. The enabling signals are gated by U3420A ($\overline{\text{ODDEN}}$) and U3420D and U3426A ($\overline{\text{EVENEN}}$). Address bit A0 selects the data transceiver. When A0 is HI, transceiver (U3422) is enabled; when LO, transceiver (U3421) is enabled. The $\overline{\text{RD}}$ signal from the microprocessor control bus selects the direction of transfer through the transceivers. When it is LO, the transfer is from the memory bus to the microprocessor data bus (read); when HI, the transfer is from the microprocessor data bus to the memory bus (write).

Acquisition Memory and Microprocessor Access

The Acquisition Memory stores the acquired waveform data that will be read out for the stored waveform display. In the normal operation, the Acquisition System controls writing the acquired data bytes, and the Microprocessor controls reading the data out for display. For diagnostic purposes, the Microprocessor also has a limited ability to write to the memory.

The Acquisition Memory is composed of two, 2K by 8-bit static random-access memories (U3418 and U3419) for a total of 4K bytes of memory. The memory space is divided into Odd and Even halves. Single channel data is stored as odd and even data byte pairs. Dual-channel operation requires that the Channel 1 data and Channel 2 data be stored in the opposite memory halves for a record length of 2k bytes each channel. In Min-Max mode, the minimum and maximum data points of each data pair are stored in opposite halves of the memory. When both channels are being acquired (CHOP) in Min-Max mode, min data points and max data points for each channel are alternately stored in opposite halves of the memory.

Both memories are enabled at the same time for either reading or writing in parallel. When reading from or writing to the memories from the Microprocessor, the microprocessor data transceivers (U3421 and U3422) are enabled on opposite states of A0, the least-significant address bit, to select the half of memory placed on the data bus for

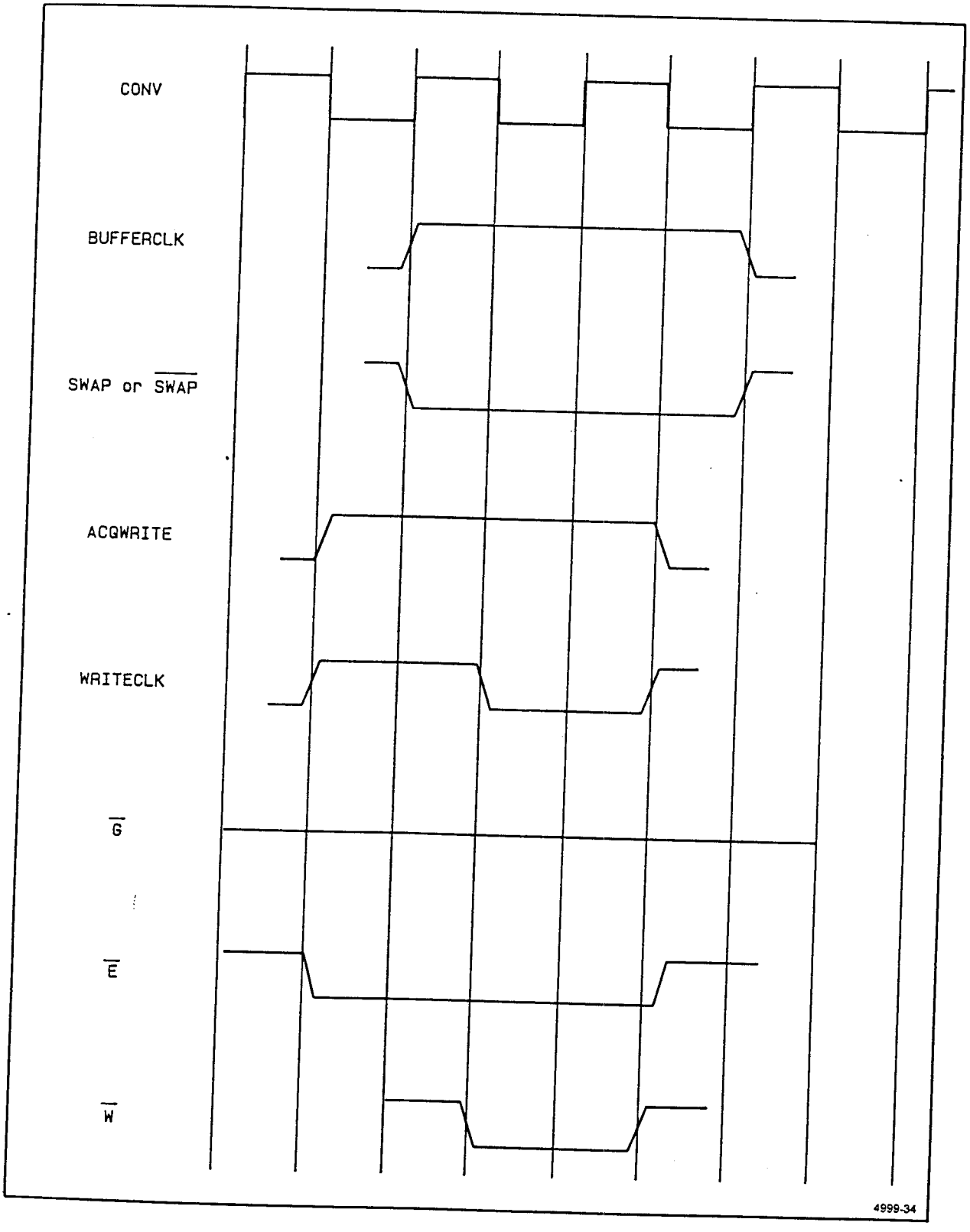


Figure 3-9. Acquisition Memory timing.

access by the Microprocessor. The memory address to be written to or read from is controlled by the Address Counter.

Acquisition Memory Address Counter

The Address Counter contains three, 4-bit binary counters (U3423, U3424, and U3425). They are presettable and cascaded to obtain a maximum count of 2048. The last bit count from the last counter (U3425) is the PREFULL signal, and when it goes HI the pretrigger portion of the record has been completed. When a triggered acquisition mode is in effect, PREFULL qualifies the next trigger received as a valid trigger point. For triggered operation of the acquisition system, the counters are preloaded with a count that causes the last bit to become a 1 when the pretrigger portion of the memory is full. The following data point pairs of a record are then stored starting at location 0 and continue up to the end of the record. The end (ENDREC) is determined by the Record Counter in the Digital Time Base circuitry (shown on Diagram 18).

While waiting for a trigger after the pretrigger part of the record is filled, data pairs are continually written into the essentially circular memory space to keep the stored waveform data (pretrigger data) current. When the acquisition becomes triggered, the Record Counter (Diagram 18) starts counting the post trigger data pairs. At the end-of-record count, $\overline{\text{ENDREC}}$ goes HI and the acquisition is stopped. The Microprocessor then reads the address of the last data byte pair that was stored. Using that address and the known length of record for the type of acquisition being done, the Microprocessor calculates the beginning address for the record.

When a read of the memory is done, the Address Counter is enabled for a parallel load of the location to be read by the $\overline{\text{ACQSEL}}$ signal from the processor. The beginning address of the record is the first address loaded from the Microprocessor Address Bus, bits A1 through A12. The least significant address bit (A0) is reserved for selecting which of the memories is to be read. The Microprocessor sequences through the addresses reading out the data bytes. In ROLL and SCAN even though there is a continual updating of the waveform seen on the crt, the Microprocessor and Acquisition System are not required to run in step at all times. Instead, the Microprocessor is allowed to carry out other processes as the data pairs are being stored in memory. When a read is started, the current address count is read and stored away. The Microprocessor then loads the address of the next unread data pair to begin reading data. Memory locations are then read and transferred to the display RAM (Diagram 15). At the end of the read, the address count is reset to the previously stored address to resume storing more data pairs into the Acquisition Memory.

Acquisition Memory Address Registers

These registers pass the address count onto the Microprocessor data bus when enabled. Registers U3427 and U3428 are enabled during different I/O periods. The lower seven bits of the address count and the SAVECLK are buffered by U3427; the upper four bits of the address count and four status bits (BTRIGD, TRIGD, BYTEINT, and $\overline{\text{ENDREC}}$) are buffered by U3428. SAVECLK is checked because both sample data pairs are transferred in parallel from the MIN/MAX Registers into the Acquisition Memory, losing the trigger-point reference. However, the samples stored in one half period of SAVECLK are stored in the opposite memory half from the samples stored in the other half period. The memory half that the trigger must be associated with is determined by the state of SAVECLK at the end of the acquisition.

The two address registers are read by the Microprocessor, as the result of an interrupt, to determine the cause of an interrupt. If the $\overline{\text{ENDREC}}$ bit is LO, the address of the end of the waveform record is stable because the acquisition stopped. In that case, the Microprocessor must read the address and store it. To do a memory read, the Microprocessor must change the count of the Address Counters. After a BYTEINT read has been done to transfer more waveform data to the display RAM to update the display, the stored address count is restored to the Address Counter to allow the acquisition to continue.

DIGITAL TIME BASE

Clock Generator

Accurate clock signals are needed to transfer the data and to control the timing of each operation. The main clocking signals are produced by an oscillator and clock generator circuit. A 40 MHz signal is produced by crystal oscillator Y4100. The 40 MHz signal clocks all the flip-flops in the Clock Generator, setting the clock edge timing of all the other clocks. In the following description, refer to the clock timing diagram, Figure 3-10.

Flip-flop U4102A divides the 40 MHz input clock by two. The 20 MHz Q output goes to the Microprocessor clock divider for timing the processor operations. The 20 MHz $\overline{\text{Q}}$ Converter) and is one input to the Clock state machine (formed by the logic gates of U3112B, C, U3113C, U4101B, and flip-flops U4118A, U4102B and U4104A). Use of the state machine allows the choice of a CONV clock rate of either 20 MHz (the same as the ADCLK rate) or 10 MHz (one-half the ADCLK rate).

The final flip-flop circuit (U4104A) in the Clock Generator produces the WRITECLK and $\overline{\text{WRITECLK}}$ signals at one-half the selected CONV clock rate. The flip-flop is held

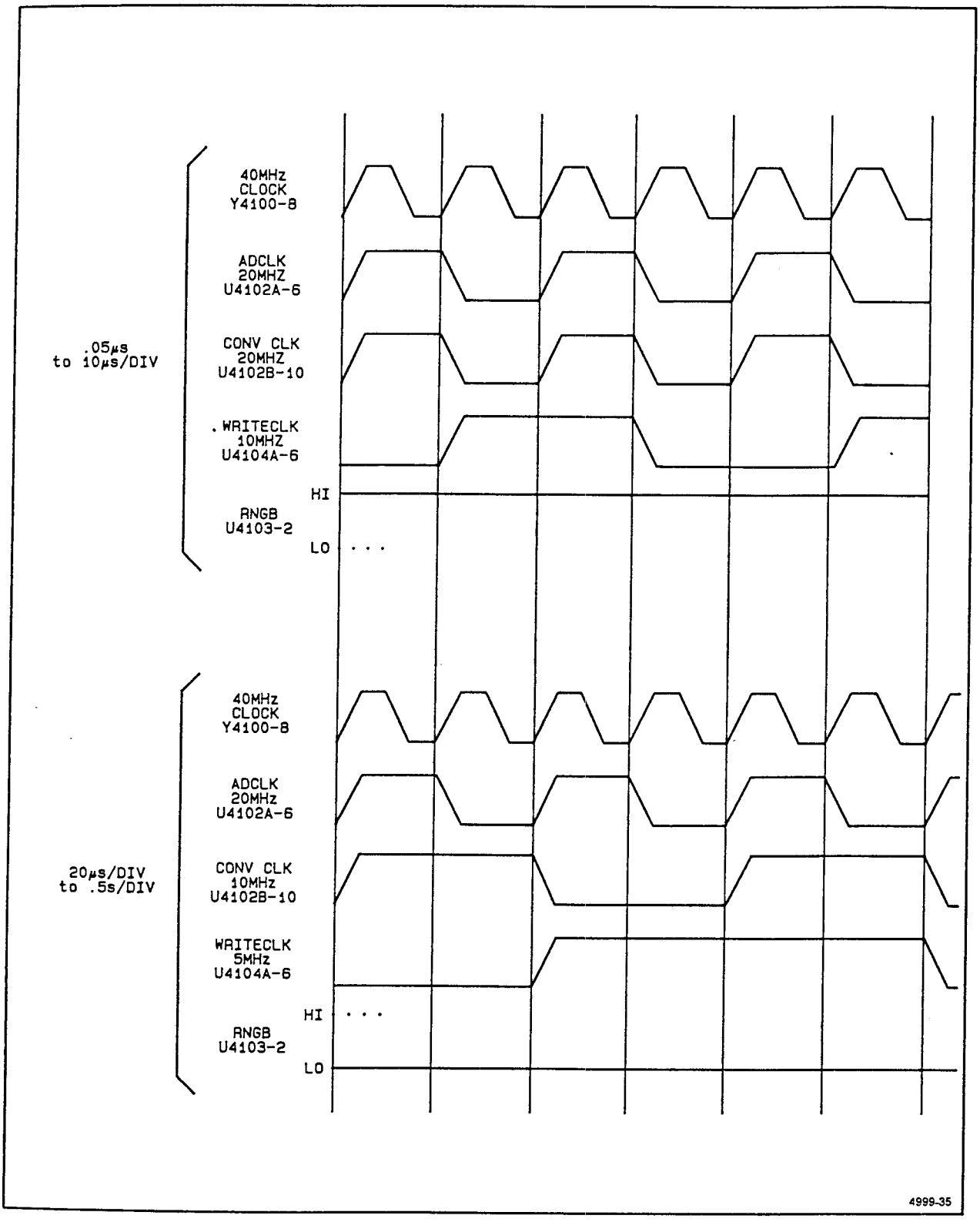


Figure 3-10. Clock timing.

reset when the ACQENA signal is LO. ACQENA is clocked HI by the $\overline{\text{CONV}}$ clock going HI (one-half CONV clock cycle after CONV goes HI). Therefore WRITECLK, at the Q output of U4104A, starts off LO at the beginning of an acquisition period.

The gating circuit of the Clock Generator looks at the states of ADCLK, CONV, and RNGB to set the active LO K input of U4102B and U4104A. The J and K inputs of U4104A have complemented signals applied from the logic gating (J from NAND-gate U3112C and K from AND-gate U4101B). When clocked, the flip-flop toggles for one state of the applied J and K signals (J HI and K LO) and has no change for the other (J LO and K HI). The WRITECLK and $\overline{\text{WRITECLK}}$ outputs of the flip-flop are therefore at one-half the CONV clock rate. The K signal from AND-gate U4101B also goes to the K input of U4102B to set up U4104A to either divide the ADCLK by two or just clock ADCLK through. The CONV clock switches from 20 MHz to 10 MHz when the SEC/DIV switch is switched from 10 μs to 20 μs while the ADCLK remains at 20 MHz for all SEC/DIV switch settings.

Time Base Mode Register

The Microprocessor controls the Digital Time Base via the Time Base Mode Register, U4119. Control bits are latched into the register from the Data bus by the rising edge of the signal on pin 11 of OR-gate U4114D. The output of U4114D pin 11 is normally HI, but when $\overline{\text{IO 2}}$ and address bit A5 are both made LO by the Microprocessor, U4114D pin 11 goes LO. The data on the AD0 through AD7 bus lines then becomes valid. Either $\overline{\text{IO 2}}$ or A5 going HI then causes the signal on pin 11 to also go HI, latching the data that is on the bus into the register. The outputs are permanently enabled by the fixed LO on pin 1 of the register.

Time Base Divider and Divider Register

The Time Base Divider is formed by a chain of six programmable counters (U4107-U4112). The Microprocessor loads the counters to produce an output from the divider that is a function of the SEC/DIV switch setting from 20 μs to 5 s per division. Alternate sources of the SAVECLK are selected at the fast sampling rates used for SEC/DIV switch settings of 10 μs to 0.05 μs (see Table 3-3).

The Microprocessor writes the preloaded counts to the Time Base Divider via time base Divider Register U4113 (see Table 3-4). A data byte is loaded into the counters of the Time Base Divider chain by placing the data on the Microprocessor Data Bus during I/O time segment $\overline{\text{IO 2}}$. After the data settles, the $\overline{\text{IO 2}}$ signal goes HI. The rising transition is gated through OR-gate U4114C to clock the data into the register. The data bits loaded determine the number of times the $\overline{\text{CONV}}$ 10 MHz clock is divided to produce the SAVECLK frequency. Flip-flop U4125A divides the output of the divider chain by two.

An external signal may be used to clock the digital acquisition system. TTL level signals up to 1 kHz may be applied to the EXT CLK INPUT connector on the instrument side panel. The external signal is applied to the D input of flip-flop U4126A where it is clocked through to the Q output on the rising edge of the $\overline{\text{WRITE}}$ clock. That Q output is applied to the D input of flip-flop U4126B and also clocked through by the rising edge of the $\overline{\text{WRITE}}$ clock. The external clock is therefore delayed by two $\overline{\text{WRITE}}$ clock periods and synchronized with the rising edge of $\overline{\text{WRITE}}$. The Q output of U4126B is applied to the SAVECLK multiplexer where it is selected when the A SEC/DIV switch is set to EXT CLK. External clock symmetry is not critical, but each amplitude must remain stable for at least 100 μs to acquire the waveform sample. One sample of a sample pair is acquired on each half cycle of the SAVECLK. As with the other clocking frequencies, flip-flop U4125A divides the signal by two to produce the SAVECLK frequency.

Record Counter

The Record Counter (U4115-U4117) determines when the total number of data samples have been acquired to fill the acquisition memory for triggered acquisitions. Depending on the record length for the acquisition and the amount of pretrigger, the Record Counters are preloaded with a count that will cause full count (ENDREC) to be generated when the record is full. When the acquisition starts, the Acquisition Memory Address Counters count up to PRE-FULL. At that point, the Trigger Mux is enabled. After a trigger arrives, the Clock Delay Timer generates TRIGD at the next $\overline{\text{CONV}}$ clock, enabling the Record Counter. The Record Counter counts RECCLK clocks until ENDREC goes HI, stopping the acquisition (because the entire record has been acquired).

Interrupt Logic

When selectively enabled by the Microprocessor, interrupts ($\overline{\text{INTR}}$) are generated after a full record is acquired, after a byte pair is acquired, or when a trigger occurs. After the interrupt is generated, the Microprocessor polls U3428 to find out what caused the interrupt.

RECORD INTERRUPT. Record interrupts are generated each time a full record has been acquired in a triggered acquisition mode. When Record Counter U4115-U4117 overflows and stops, the end of record signal ENDREC is generated HI at U4105B pin 9. If the Microprocessor has

Table 3-3

Time Base Clock Frequencies

SEC/DIV	CONV	SAVECLK	RECCLK	SAVECLK SOURCE	RANGE	
					A	B
0.05 μs	20 MHz	10 MHz	20 MHz	$\overline{\text{CONV}}$/2	1	1
0.1 μs	20 MHz	10 MHz	20 MHz	$\overline{\text{CONV}}$/2	1	1
0.2 μs	20 MHz	10 MHz	20 MHz	$\overline{\text{CONV}}$/2	1	1
0.5 μs	20 MHz	10 MHz	20 MHz	$\overline{\text{CONV}}$/2	1	1
1 μs	20 MHz	10 MHz	20 MHz	$\overline{\text{CONV}}$/2	1	1
2 μs	20 MHz	10 MHz	20 MHz	$\overline{\text{CONV}}$/2	1	1
5 μs	20 MHz	10 MHz	20 MHz	$\overline{\text{CONV}}$/2	1	1
10 μs	20 MHz	5 MHz	10 MHz	$\overline{\text{WRITECLK}}$/2	0	1
20 μs	10 MHz	2.5 MHz	5 MHz	DIVIDER/2	1	0
50 μs	10 MHz	1 MHz	2 MHz	DIVIDER/2	1	0
0.1 ms	10 MHz	0.5 MHz	1 MHz	DIVIDER/2	1	0
0.2 ms	10 MHz	0.25 MHz	0.5 MHz	DIVIDER/2	1	0
0.5 ms	10 MHz	0.1 MHz	0.2 MHz	DIVIDER/2	1	0
1 ms	10 MHz	50 kHz	100 kHz	DIVIDER/2	1	0
2 ms	10 MHz	25 kHz	50 kHz	DIVIDER/2	1	0
5 ms	10 MHz	10 kHz	20 kHz	DIVIDER/2	1	0
10 ms	10 MHz	5 kHz	10 kHz	DIVIDER/2	1	0
20 ms	10 MHz	2.5 kHz	5 kHz	DIVIDER/2	1	0
50 ms	10 MHz	1 kHz	2 kHz	DIVIDER/2	1	0
0.1 s	10 MHz	0.5 kHz	1 kHz	DIVIDER/2	1	0
0.2 s	10 MHz	0.25 kHz	0.5 kHz	DIVIDER/2	1	0
0.5 s	10 MHz	0.1 kHz	0.2 kHz	DIVIDER/2	1	0
1 s	10 MHz	50 Hz	100 Hz	DIVIDER/2	1	0
2 s	10 MHz	25 Hz	50 Hz	DIVIDER/2	1	0
5 s	10 MHz	10 Hz	20 Hz	DIVIDER/2	1	0
EXT	10 MHz	EXT/2	EXT	EXTCLK/2	0	0

Table 3-4

Time Base Divider Preload Bits

SEC/DIV Setting	SAVE CLOCK Frequency	DIVIDER Output	Divider DD Bits 7 6 5 4 3 2 1 0	Divide Ratio
20 μs	2.5 MHz	5 MHz	1 1 1 1 1 1 0 0	2
50 μs	1 MHz	2 MHz	1 1 1 1 1 0 1 1	5
0.1 ms	0.5 MHz	1 MHz	1 1 1 1 1 0 0 0	10
0.2 ms	0.25 MHz	0.5 MHz	1 1 1 1 0 1 0 0	20
0.5 ms	0.1 MHz	0.2 MHz	1 1 1 1 0 0 1 1	50
1 ms	50 kHz	100 kHz	1 1 1 1 0 0 0 0	100
2 ms	25 kHz	50 kHz	1 1 1 0 0 1 0 0	200
5 ms	10 kHz	20 kHz	1 1 1 0 0 0 1 1	500
10 ms	5 kHz	10 kHz	1 1 1 0 0 0 0 0	1,000
20 ms	2.5 kHz	5 kHz	1 1 0 0 0 1 0 0	2,000
50 ms	1 kHz	2 kHz	1 1 0 0 0 0 1 1	5,000
0.1 s	0.5 kHz	1 kHz	1 1 0 0 0 0 0 0	10,000
0.2 s	0.25 kHz	0.5 kHz	1 0 0 0 0 1 0 0	20,000
0.5 s	0.1 kHz	0.2 kHz	1 0 0 0 0 0 1 1	50,000
1 s	50 Hz	100 Hz	1 0 0 0 0 0 0 0	100,000
2 s	25 Hz	50 Hz	0 0 0 0 0 1 0 0	200,000
5 s	10 Hz	20 Hz	0 0 0 0 0 0 1 1	500,000

set RECINTEN (U4119 pin 12) HI, ENDREC and the enable are combined at U4120D, making $\overline{\text{INTR}}$ LO generating a maskable interrupt. To clear the interrupt, the Microprocessor makes ACQENA (U4118A pin 5) LO via U4119. This makes ENDREC (U4105B) LO and $\overline{\text{INTR}}$ (U4120D) HI, removing the interrupt.

BYTE INTERRUPT. Byte interrupts are generated each time a byte pair is acquired in the byte modes of ROLL and SCAN. To start the acquisition of a byte pair, the Microprocessor sets BYTEINTEN (U4119 pin 13) HI. After the acquisition of two bytes, SAVECLK (U4125B pin 9) goes HI setting U4118B. A HI at pin 9 of U4118B is inverted by U4120B, generating a LO $\overline{\text{INTR}}$, the maskable interrupt, at U4120B pin 4. To clear the interrupt, the Microprocessor makes TBMODE (U4114D pin 11) LO. This resets U4118B, removing the interrupt.

TRIGGERED INTERRUPT. Triggered interrupts are generated when triggers occur after first being enabled by the Microprocessor in a triggered mode with triggers allowed. The Microprocessor enables the interrupt by setting TRIGINTEN (U4119 pin 14) HI. When a trigger occurs, TRIGD (U4226B pin 9) goes HI. The HI TRIGD and TRIGINTEN are combined at U4120C, making $\overline{\text{INTR}}$ LO. To clear the interrupt, the Microprocessor makes TRIGINTEN (U4119 pin 14) LO, removing the interrupt.

Trigger Mux

Multiplexer U4227 is driven by the B/A TRIG and CALTIMER signals. The multiplexer selects either the A GATE, B GATE, or $\overline{\text{CONV}}$ signal to drive the Clock Delay Timer circuit. The $\overline{\text{CONV}}$ clock is used by the CALTIMER to determine the maximum and minimum counts from the Clock Delay Timer circuit. See Table 3-5 for the switching logic of the multiplexer. The additional state of the $\overline{\text{TEST}}$ signal is necessary to determine if a maximum or a minimum count is to be measured by the Clock Delay Timer for calibration.

Clock Delay Timer

The circuitry forming the Clock Delay Timer is used only during equivalent-time sampling (20 μs per division to 0.05 μs per division). The purpose of the timer is to determine the time interval between the trigger event and the next rising edge of the $\overline{\text{CONV}}$ clock. The Microprocessor

Table 3-5

Trigger Logic Multiplexer Switching

CALTIMER	$\overline{A}$/BTRIG	$\overline{TEST}$	TRIGGER MODE	SELECTED SIGNAL
0	0	1	A TRIG	A GATE
0	1	1	B TRIG	B GATE
1	0	0	MIN COUNT	$\overline{CONV}$
1	1	1	MAX COUNT	$\overline{CONV}$

must know the information to place the data samples into the correct locations in Display Memory. Since the trigger is asynchronous to the $\overline{CONV}$ clock (and therefore to the SAVECLK that stores data byte pairs into the Acquisition Memory), no fixed timing relationship exist between the trigger and the data samples taken as a result of the trigger. Therefore the relationship must be determined for each trigger in equivalent-time sampling.

The timer is formed by a dual-slope capacitor charging circuit. A fast-charging current source composed of Q4203 and Q4204 charges capacitor C4201 when FET Q4207 is turned off, removing its shunting effect (short) from the capacitor. This happens for every A GATE or B GATE (depending on which trigger it is looking for) regardless of whether a STORE mode trigger is enabled or not. If a STORE mode trigger was not enabled, the capacitor is immediately discharged when the gate signal passes. If a STORE mode trigger is enabled (PREFULL generated from the acquisition memory Address Counter), Q4207 is held off to allow C4201 to continue to charge. The fast-charging current source through Q4204 is then shut off by the second rising edge of the $\overline{CONV}$ signal clocking a LO onto the $\overline{Q}$ output of flip-flop U4226B. The LO turns Q4203 on and shuts off the fast-charging current source, Q4204. The complementary HI on the Q output of U4226B also removes the reset from the Clock-Delay-Timer counter, U4230, enabling the counter to count.

A slow-charging current source (Q4205 and associated resistors) then begins discharging C4201 towards the −8.6 V supply through Q4205 and R4212. This discharge path has a long time constant so that the discharge time is much longer than the capacitor's charge time. The voltage on C4201 is applied to the inverting input of comparator U4229. A comparison voltage with a threshold of about 0.6 V is on the noninverting input of the comparator.

When the capacitor's voltage drops to the comparison voltage, the output of the comparator goes HI. That HI is applied to NAND-gate U4106, the Set input of flip-flop U4232A. The flip-flop has been toggling on the CONV clock, so depending on the state of the Q output when the comparator changes state, the flip-flop will either be set immediately (if the Q state is HI) or as soon as the logic state of the Q output of U4232A goes HI. The action of the NAND-gate ensures that the flip-flop becomes set within ±1 CONV clock period of the actual comparator output level change. As soon as U4232A becomes set, a LO is placed on the D input of flip-flop U4232B. On the next rising edge of the $\overline{CONV}$ clock, the LO is clocked to a HI on the $\overline{Q}$ output of U4232B, stopping the Clock-Delay-Timer counter. The count now held in the counter is a measure of the time between the trigger point and the next rising edge of the $\overline{CONV}$ clock. In I/O period $\overline{IO\text{-}1}$, address line A3 is made LO by the Microprocessor, enabling the count onto the data bus so the count can be read. The count is used by the Microprocessor to place the equivalent-time data samples into the correct (in relation to the trigger) display memory locations.

In order for the Microprocessor to place the data samples into the correct display locations, the Microprocessor needs to know the maximum and minimum counts produced by the Clock Delay Timer. A calibration routine in the Diagnostics determines the maximum and minimum counts and calculates the calibration constant used by the equivalent-time sampling firmware.

To determine the maximum count, $\overline{CONV}$ is selected as the trigger source (U4227 pins 12 and 13). The trigger source, through U4228A, U4127, and Q4207 starts the ramp on C4201. The $\overline{CONV}$ trigger also propagates through U4228A, U4228B, U4127C, and U4226B to Q4203, stopping the current source for the ramp and removing the clear on counter U4230 pin 10. Counter U4230 starts counting and contains the maximum count when stopped by $\overline{CONV}$ through U4232.

To determine the minimum count, $\overline{CONV}$ is also selected as the trigger source. The trigger, through U4228A, starts the ramp on C4201. The calibration routine sets $\overline{TEST}$ LO. With $\overline{TEST}$ LO (on U4228B pin 10), $\overline{CONV}$ bypasses U4228B, stopping the current source for the ramp, starting counter U4230 50 ns sooner.

Resistor R4213 and C4202 adjust the counter's gain and offset. Nominal counts are 300 for maximum and 100 for minimum. The difference of the two counts represents the 50 ns $\overline{CONV}$ clock period.

B-Delay Timer

The B-Delay Timer determines the starting address of the B Display in memory. The length of the record is determined by the setting of the SEC/DIV switch and the acquisition-mode information (i.e. is it CHOP, single trace, or a 1K or a 4K acquisition). The BTRIGD signal (U4121A pin 5) goes HI on the first falling edge of RECCLK after the B-GATE signal goes HI. BTRIGD going HI causes U4123 and U4124 to latch the value of the Record Counter. The microprocessor then reads the starting address from U4123 and U4124, which are enabled by $\overline{IO\ 2}$, $\overline{IO\ 1}$, and A5 (Address Decode).

DIGITAL DISPLAY

A custom LSI integrated circuit controls the stored waveform and readout displays. Six 16K x 4-bit random-access memories (RAM) make up the Display Memory. Four of the RAM chips provide 32K x 8-bit waveform data, and two RAMs hold the 32K x 4-bit waveform-attribute data. Waveform data may be stored in the RAM from data on the Microprocessor bus or data may be read from the RAM and transferred to a Communication Option. For waveform displays, data is read from the RAM (display memory) by the display controller. The display controller then processes the data, and then drives the Vertical (Y) and Horizontal (X) digital-to-analog converters (DAC) where the data is converted to analog voltages used to drive the X- and Y-Axis vector generators.

Data Transceivers

Communication between the Microprocessor and the display memory is via two bus transceivers, U9206 and U9207. Waveform data from the Acquisition Memory is transferred to the display memory where the data is always available to the Display Controller for refreshing the display. The data transceivers are enabled by logic gating in U9211 that decodes the PA15 and PA14 signals from the Microprocessor and the $\overline{PROCEN}$ signal from the Display Controller to determine when a transfer is possible. The direction of transfer is controlled by the $\overline{WR}$ (write) signal from the Microprocessor. The $\overline{WR}$ signal also enables U9211 to allow either a read from memory (for outputting data) or a write to memory (for transferring in the data from the Acquisition Memory). Bus transceiver U9206 is enabled for 8-bit data transfers and transceiver U9207 is enabled for 4-bit transfers.

Address Decoder

To access a byte in RAM, a row address followed by a column address is required. Row and column memory addresses are written together as one address word from the Microprocessor. Address Decoders U9204 and U9205 are switched by the ROW/$\overline{COL}$ signal from the Display Controller to select either the row address or the column address from the Microprocessor address bus. The $\overline{RAS}$ and $\overline{CAS}$ signals enable the address latches, internal to each display RAM, to latch the selected row and column addresses. Column addresses are decoded from the middle six bits of the 8-bit address by address decoders in each RAM. Row addresses require all eight bits. The Display Controller has direct access to addresses in the RAM using the RA bus.

RAM

Six 16K by 4-bit memories make up the display RAM. The 8-bit waveform bytes are stored with the lower four bits in U9203 and U9233 and the higher four bits in U9202 and U9232. The remaining RAMs (U9201 and U9231) store attribute bits that are used to define the waveform print intensity and mark the end of the record. The memories are arranged in a 256 X 64 row and column format to allow eight addressing lines to access the 16K of 4-bit memory addresses (64K-bits of memory).

Memory refreshing is satisfied whenever the 256 Row addresses are accessed. Refreshing occurs when the Display Controller does a memory read for display purposes. While the Microprocessor is controlling the Display Memory, it must also perform memory refreshing by activating all the memory Row addresses. To maintain the dynamic memory, a refresh must be done at least every eight milliseconds.

DATA TYPES. The data stored in the Display Memory is either readout characters or waveforms. The microprocessor also uses the display memory for operational data storage. In either case a 9-byte field-attribute preamble is read first. The preamble defines the data type and sets up the display attributes. Readout information is displayed using short vector X-Y displays positioned to specified fields on the crt.

Display Controller

The Display Controller runs the display system for the STORE waveform and STORE and NON STORE readout displays. It takes control of the RAM to read the waveform or readout data. Besides the waveform data, the Display Controller runs the Store Z-Axis, selects the type of display (vector, dots, or X-Y plotter output), and drives the horizontal and vertical channel switches.

When reading data out of the RAM, the Display Controller has direct access to the memory address bus (RA). RAM row and column addresses to be read from are sequenced through in order. When a display data read is taking place, the dynamic memory is refreshed by the Display Controller.

When the Display Controller has completed a display frame, it signals the Microprocessor (using the $\overline{\text{INTR}}$ signal) that the last field is finished and awaiting the next frame request. After the interrupt is received, the Microprocessor can request the next frame ($\overline{\text{FRAME}}$), then the Display Controller resumes control of the RAM for the next frame of data. When $\overline{\text{PROC RQ}}$ (U9208 pin 3) is HI, the Display Controller is in the middle of a display cycle and the Microprocessor is denied access to the display RAM. The Microprocessor can request access to the Display RAM using the $\overline{\text{PROC RQ}}$ ($\overline{\text{RAM SEG}}$) signal line to either write in new waveform data or read out data for the Communication Option. The Display Controller allows the Microprocessor to access the display RAM by setting the $\overline{\text{PROC EN}}$ (U9208 pin 5) signal line LO. A LO $\overline{\text{PROC EN}}$ signal enables the circuitry that allows the $\overline{\text{WR}}$, PA14, and PA15 signals, from the Microprocessor, to control the display RAM. Even though the memory addresses are under control of the Microprocessor, the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals are generated by the Display Controller.

YDAC and XDAC

Data from display controller U9208 is applied to X- and Y-axis DACs U9210 and U9220. These DACs are biased to provide output currents (approximately 0 to 2 mA) proportional to the digital data. R9214 and R9224 are adjustments to align the storage signals on the crt. The DAC currents are applied to the Vector Generator along with various control signals from U9208 via W6100.

VECTOR GENERATOR

Vector Generators

Vector Generator circuitry is shown on Diagram 20. U6303 and U6304 convert the DAC currents into bipolar voltages (approximately −2.5 V to +2.5 V) which are applied to sample and hold circuits U6305 and U6306. Outputs of the sample and hold circuits are applied to integrator stages U6307 and U6308 through electronic switches in U6301A and C. The integrator output signals are continuously fed back to the sample and hold inputs, causing these input voltages to be equal to the difference between the drive inputs and the integrator outputs. When the vector sample ($\overline{\text{VECT-SMPL}}$) control line (via U6301B) is actuated, the outputs of the sample and hold circuits store these difference signals. Since the integrator output slopes are proportional to these signals, the net result is to effectively "connect the dots" which are equivalent to the digital data values.

These circuits also have a "dot" mode available so that the integrator outputs are stepped (dots) rather than continuous (vectors). When the VECT/$\overline{\text{DOT}}$ signal is LO, U6301A and C switch the integrator inputs directly to the difference signals while also disconnecting the integration capacitors C6315 and C6314. The feedback loops are thus closed continuously, resulting in normal amplifier action.

Although the Vertical and Horizontal vector generators operate the same, there are some differences between the circuits and between their signal characteristics. To end up with the proper signal polarities at the crt, X DAC U9210 (Horizontal) current is from 2 mA to 0 mA, while Y DAC U9220 (Vertical) current is from 0 mA to 2 mA. Also, the vertical integrator output is −2 V to +2 V while the horizontal integrator output is −2.5 V to +2.5 V. The reduced vertical dynamic range allows proper interface to the main deflection system. Since the vertical signal eventually passes through the vertical delay line before reaching the crt, it is necessary to delay the horizontal signal as well. This is done in the vector mode by delaying slightly the vector sample signal applied to U6306 via R6320 and C6312. In the dot mode the crt beam is blanked during the transitions so the dots are only displayed after the signals have arrived and settled.

VECTOR INTEGRATOR. The Y-axis (vertical) current from the D/A Converter goes to the inverting input of operational amplifier U6303. The amplifier is biased to produce a bipolar output voltage, from −2.5 V to +2.5 V, that is proportional to the input current. Negative feedback from the parallel combination of R6303 and C6311 stabilizes the amplifier.

Biasing of the non-inverting input of both the X-axis and the Y-axis amplifiers is identical and supplied by a resistive divider formed by R6304 and R6305 between ground and the +5 V reference. Both resistors are equal valued to produce a bias voltage of +2.5 V. Resistor R6308 provides a summing node for the input vector current and the feedback current and develops the voltage on the inverting input of U6303. Full current range of the vector signal is from 0 to 2 mA. With no vector current in, the feedback current supplies the full current through R6308, and the output voltage of U6303 goes to −2.5 V. At maximum vector current input, the sum of the current through R3608 must remain the same as with no vector current; therefore the feedback current is reduced by the amount of the vector current, and the output voltage goes to +2.5 V.

SAMPLE-AND-HOLD. The voltage output of U6303 is applied via R6309 to sample-and-hold circuit U6305. Sample-and-Hold (S/H) switching is controlled by the $\overline{\text{VECT SMPL}}$ signal from the Display Controller applied to

U6305 pin 14. That signal in turn is controlled by the PLT-EN signal (U6301B pin 9) that switches section B of multiplexer U6301. When displaying storage waveforms and readout characters, the PLT-EN signal is not active, and the VECT SMPL signal is switched to control the S/H circuit. For producing X-Y Plots, U6301C is activated, and the VECT SMPL signal drives the X-Y Plotter Pen-Down circuit (shown on Diagram 22).

SAMPLE INTEGRATOR. During digital storage waveform displays, the S/H circuit and the Y-Integrating circuit formed by U6307 and associated components produce either vectors or dots. When U6301C connects pin 13 to pin 14, U6307 integrates each step output of the S/H circuit into a smooth ramp signal. This integrated signal is the vertical deflection signal (still single-ended) that connects the data points of the stored waveform display. When the user selects either dot displays or X-Y Mode, multiplexer U6301C connects pin 12 to pin 14. The long time constant integrating function of U6308 is switched out, and U6307 acts as an amplifier only for the voltage being held by the S/H circuit, causing the crt display to be dots. For readout character displays both during STORE and NONSTORE modes, the S/H and integrator work only in the vector mode because readout characters are vector displays.

The integrator output is subtracted from the input voltage at all times. When VECT SMPL goes LO, the difference value is sampled and held by S/H U6305. The held voltage value sets the slope of the integrator and effectively "connects the dots" since the slope of the output vector is proportional to the difference between the input voltage and the output voltage of the integrator.

Diode clamps CR6301, CR6303, CR6305, and CR6307 prevent voltage transients that could cause U6301C latch up.

Vector Amplifiers

The integrator outputs are applied to vector amplifiers U6401 and U6402, which are differential voltage-to-current converters. Their outputs are differential currents which are sent to the main deflection multiplex circuitry via J6410 and the I/O wiring harness. Vertical positioning information is processed by display controller U9208, but horizontal position information is not. Therefore the horizontal position voltage is applied to U6402D to affect horizontal position control of stored waveforms. At times when readout characters are being drawn, this position signal is shunted by transistor U6403A to reduce the positioning effect on the characters. This action is controlled by the HPOS-DIS signal from the display controller.

Plot Drive

When plot mode is on, the display controller activates the PLT-EN signal, causing U6301B to apply the VECT-SMPL signal to the PEN-DN line via U6404A and U6402E, and the display controller internal modes change so that VECT-SMPL provides the pen down control function. The PEN-DN signal is sent via J6420 to the Z-axis section and to the X-Y board or communication option board (if installed). When U6301B activates plot mode, Q6301 pulls the sample control lines of U6305 and U6306 LO putting them in tracking mode. This closes the vector generator feedback loops regardless of vector/dot mode selection. The PLT-EN signal also turns on operational transconductance amplifiers U6404A, B, and C via transistor U6403E. Normally, their outputs are off, the plotter signals are zero (held at ground by R6433, R6434). In plot mode they turn on and act as voltage followers for the vector signals (Y POINT, X POINT, and PEN). The "Y" amplifier input is connected ahead of the Y vector generator to preserve the ±2.5 V range and correct polarity. The X-PLOT and Y-PLOT signals are sent via J6420 to the X-Y board or communication option board (if installed).

Readout Off Detector

To detect when the Storage/Readout Intensity knob is at its counterclockwise end, U6405A (Diagram 20) monitors the readout (RO) voltage from J6410. Since RO voltage is normally negative, but goes slightly positive at the end of its rotation, U6405A output will go positive, turning on transistor U6403B, causing the NO-RO line to be LO. This signal is sent to the I/O board as status information.

Signal Conditioning

The signals ARES1, A-RES2, B-RES, and B-CAPS on J6420 come from the Sweep Interface board. They are encoded analog currents which contain most of the information about the positions of the A and B Timing switches. Since the sum of the possible changes in these currents is larger than U6302 (5V REF) can accommodate, U6405B (Diagram 21) is used to buffer the 5V reference to supply the termination resistors (Diagram 20). As these currents change, the resulting voltages are measured by the Status A/D (Diagram 19) so that the Microprocessor can determine the state of the timing switch.

I/O and Vector Generator Board Power Distribution

±15 VOLT POWER SUPPLYS. U6305 and U6306 operate from ±15 Volt supplies. These are generated by flyback converters (see Diagram 21) consisting of U6202A, U6202B, Q6202, Q6203, and associated circuitry. The comparators in U6202 form oscillators which drive the switch transistors to alternately store and unload energy in

their respective chokes. Feedback is applied to the comparators causing duty cycle and frequency modulation, which adjusts output power accordingly.

+5 VOLT POWER SUPPLY. Logic power (+5 V) for all I/O board and Vector Generator board circuitry is generated from the +8.6 V supply by U6201.

+5 VOLT REFERENCE. The 5 Volt Reference is generated by U6302. It is used by the vector generator circuits, status A/D circuit, display DAC circuit, and acquisition system. Associated with each of these circuits is a local pull-up resistor from the +8.6 V supply to the 5V reference line to supply nominal load current so that U6302 does not have to supply the total load current. This also greatly reduces the reference line current which could cause excessive voltage drops at the far ends of its travel.

Status ADC and Bus Interface

I/O PORTS. The system data bus and associated control signals are sent to the I/O board via J6100 (see Diagram 19). Input ports U6102 and U6103 transfer logic signals representing instrument status. U6103 operates as a simple port for eight of the status lines. U6102 has 15 input signals. It serves as a data buffer for the Status A/D converter U6105, when required. During part of the status scanning cycle, U6105 data outputs are tri-stated, and seven additional status signals are applied via 22 kΩ resistors (R6121 through R6126). The Microprocessor then reads these status lines through U6102. When U6105 is active, its outputs dominate the data lines and the 22 kΩ resistors act as high impedance loads. The Microprocessor can then read the data from U6105 via U6102. Output port U6104 is used to control the operation of U6105 to perform the A/D conversion function. U6104 is also the multiplexer selection register, driving U6106 and U6108, which select the analog status signals to be measured. The port address selection is made by combinations of control lines $\overline{IO\text{-}0}$, and $\overline{IO\text{-}1}$, and address lines A2 and A3. U6101A and B provide the selection logic for U6104.

STATUS A/D. U6105 is a 10-bit A/D converter which allows measurement of analog status signals. After each conversion it produces an interrupt which is gated by U6101D and applied to Q6201 via R6218. This produces a processor interrupt to indicate completion of its task. This interrupt is maskable by U6104. U6107A serves as a buffer amplifier to drive the input resistance of U6105 while maintaining fairly high load impedance for U6106 and U6108. U6107B and U6107C are differential amplifiers which convert the differential vertical position signals to single voltage levels within the range of the measuring system.

POWER INPUT, PREREGULATOR AND INVERTER

The Power Supply (see Diagram 8 and Diagram 9) changes the ac power-line voltage into the voltages needed for instrument operation. It consists of the Power Input, Preregulator, and Inverter circuits (which drive the primary of the power transformer) and secondary circuits (which produce the necessary supply voltages for the instrument).

Power Input

The Power Input circuit changes the ac power-line voltage to filtered dc for use by the Preregulator.

POWER switch S901 connects the ac power line through fuse F9001 to the bridge rectifier formed by CR901, CR902, CR903, and CR904. The full-wave bridge rectifies the source voltage, and the output is filtered by C906. Input surge current at instrument power-on is limited by thermistor RT901. The thermistor resistance is moderately high when the power is first turned on, but decreases as the input current warms the device. The instrument is protected from large voltage transients by suppressor VR901. Conducted interference originating within the power supply is attenuated by common-mode transformer T901, differential-mode transformer T903, line filter FL9001, and capacitors C900, C902, and C903.

Preregulator

The Preregulator provides a regulated dc output voltage for use by the Inverter circuitry.

When the instrument is turned on, the voltage developed across C906 charges C925 through R926. When the voltage across C925 has risen to a level high enough that Pulse-Width Modulator U930 can reliably drive Q9070, U930 receives operating supply voltage through Q930. This voltage level is set by zener diode VR925 in the emitter of Q928 and by the voltage divider formed by R925 and R927. The zener diode keeps Q928 biased off until the base voltage reaches approximately 6.9 V. At that point, Q928 is biased into conduction, and the resulting collector current causes a voltage drop across R929 that biases on Q930. The positive feedback through R930 reinforces the turn-on of Q928, which quickly drives both Q928 and Q930 into saturation. Once Q930 is on, the Pulse-Width Modulator begins to function.

Pulse-Width Modulator U930 controls the output voltage of the Preregulator by regulating the duty cycle of the pulse going to the gate of Q9070. The modulator has an

oscillator that operates at a frequency set by R919 and C919 (approximately 60 kHz). A sawtooth voltage produced at pin 5 of U930 is compared internally with the output voltage produced by the two internal error amplifiers. Whenever the sawtooth voltage is greater than the error amplifier output voltage, Q9070 is biased on to supply current to the remaining portions of the switching circuitry and charge C940. The two error amplifiers maintain a constant output voltage and monitor the output current of the Preregulator. One input of each amplifier is connected through a divider network to the IC internal +5 V reference. The output voltage of the Preregulator is monitored by the voltage divider at pin 2. The voltage drop across R907, produced by the Preregulator output current, is applied to the internal current-limit amplifier at pin 16.

When the instrument is first turned on, the current-limit amplifier controls the conduction time of Q9070. While Q9070 is conducting, the output current increases until a voltage large enough to permit the current-limit circuitry to function is developed across R907. The current-limit amplifier then holds the output current below the limiting threshold of approximately 1 A. When the voltage across C940 reaches approximately 43 V, the internal voltage amplifier starts controlling the duty cycle of Q9070, and the Preregulator will not limit current unless there is excessive current demand.

With Q9070 off, C907 charges to the output voltage of the Power Input circuit. When Q9070 turns on, current through the FET comes from the winding connected to pins 1 and 2 of T906 and from C907. Current to C907 is supplied by the winding connected to pins 4 and 5 of T906. When U930 shuts off Q9070, the collapsing magnetic field raises the voltage at the anode of CR907. This diode then becomes forward biased and passes the currents supplied by C907 and the winding connected to pins 4 and 5 of T906. For this part of the cycle, current to C907 is supplied by the winding connected to pins 1 and 2 of T906. This process continues for each period of the oscillator, and the duty cycle controlling the conduction period of Q9070 is altered as necessary to maintain 43 V across C940. During each oscillator period, Q908 is used to discharge the gate-drain capacitance of Q9070. At the shutoff point, Pin 10 of U930 goes LO to reverse bias CR908 and turn on Q908 to switch off the FET.

Once the supply is running, power to U930 is supplied from the winding connected to pins 6 and 7 of T906. Diode CR920 half-wave rectifies the voltage across pins 6 and 7 to keep filter capacitor C925 charged and to maintain supply voltage to U930 through Q930.

Instrument protection from excessive output voltage is supplied by silicon-controlled rectifier Q935. Should the Preregulator output voltage exceed 51 V, zener diode VR935 conducts, causing Q935 to also conduct. The Preregulator output current is then shunted through Q935, and the output voltage quickly drops to zero. With the supply voltage of U930 no longer being provided by the winding connected to pins 6 and 7 of T906, the Preregulator shuts down, and Q935 becomes reset. The supply then attempts to power up, but it will shut down again if the overvoltage condition reoccurs. This sequence continues until the overvoltage condition is corrected. A thermal shutdown circuit is included to protect the instrument from damage in case of fan failure or air flow restriction at high ambient temperatures. Overheating causes the resistance of RT950 to increase, eventually firing SCR Q950, which reduces voltage on VR943. This causes all outputs to drop to very low values, thus reducing total power dissipation. To reset the circuit, the power must be shut off momentarily.

Inverter

The Inverter circuit changes the dc voltage from the Preregulator to ac for use by the supplies that are connected to the secondaries of T948.

The output of the Preregulator circuit is applied to the center tap of T948. Power-switching transistors Q946 and Q947 alternate conducting current from the Preregulator output through the primary windings of T948. The transistor switching action is controlled by T944, a saturating base-drive transformer.

When the instrument is first turned on, one or the other of the switching transistors starts to conduct. As the collector voltage of the conducting transistor drops toward the common voltage level, a positive voltage is induced from T944 to the base of the conducting transistor that reinforces conduction. Eventually T944 saturates; and, as the voltage across T944 (and T948) begins to reverse, the conducting transistor is cut off by the drop in base drive. The other transistor does not start conduction until the voltage on the leads of T944 reverse enough to bias it on. The saturation time of T944 plus the transistor-switching time determine the frequency of Inverter operation (typically about 20 kHz). After the initial Inverter start up, the switching transistors do not saturate; they remain in the active region during switching.

Diodes CR946 and CR947 serve as a negative-peak detector to generate a voltage for controlling the output of the error amplifier. Capacitor C943 charges to a voltage equal to the negative peak voltage at the collectors of Q946 and Q947, referenced to the Preregulator input voltage. This voltage level is applied to the divider formed by R937, R938, and R939. The error amplifier, formed by Q938 and Q939, is a differential amplifier that compares the reference voltage of VR943 with the wiper voltage of potentiometer R938. The current through Q939 sets the

base drive of Q944 and, thereby, controls the voltage on C944. This voltage biases Q946 and Q947 to a level that maintains the peak-to-peak input voltage of T948. The amplitude of the voltage across the transformer primary winding, and thus that of the secondary voltages of T948, is set by adjusting −8.6-V-ADJ potentiometer R938.

At turn-on, Q938 is biased off, and Q939 is biased on. All the current of the error amplifier then goes through Q939 to bias on Q944. The current through Q944 controls the base drive for Q946 and Q947. Base current provided by base-drive transformer T944 charges C944 negative with respect to the Inverter circuit floating ground (common) level.

POWER SUPPLY SECONDARIES, Z-AXIS AND CRT

XFMER and LV Power Supplies

The Low-Voltage supplies use center-tapped secondary windings of T948 (XFMER). The +100 V supply is rectified by CR954 and CR955 and filtered by C954. Diodes CR956 and CR957 rectify ac from taps on the 100 V winding, and C956 filters the output to produce +30 V dc. The full-wave diode bridge formed by CR960, CR961, CR962, and CR963 produces the +8.6 V and −8.6 V supplies. Filtering of the +8.6 V is done by C960, L960, and C962. Filtering of the −8.6 V is done by C961, L961, and C963. Ac voltage from the ±8.6 V primary is rectified by CR965 and CR967, and then filtered by C965 and R965 to provide the fan power source. The +5 V supply is produced by CR970, C968, L968, C958 and C970. The −5 V supply is produced by CR980, CR981, C964, L962, and C959.

Unblanking Logic, Intensity, and Z-Axis Ampl

The Z-Axis Amplifier, shown on Diagram 9, controls the crt intensity level via several input-signal sources. The effect of these input signals is either to increase or decrease trace intensity or to completely blank portions of the display. The Nonstore Z-Axis drive signal currents, as set by the A and B Z-Axis switching logic and the input current from the EXT Z AXIS INPUT connector (if in use), are summed at the emitter of common-base amplifier Q825. The total sets the collector current of the stage. The common-base amplifier provides a low-impedance termination for the input signals and isolates the signal sources from the rest of the Z-Axis Amplifier.

For the Nonstore Z-Axis signals, common-base transistor Q829 passes a constant current through R832. This current is divided between Q825 and Q829, with the portion through Q829 driving the shunt-feedback output amplifier formed by Q835, Q840, and Q845. The bias level of Q825 therefore controls the emitter current available to Q829. Feedback-resistor R841 sets the transresistance gain for changing the input current to a proportional output voltage. Emitter-follower Q835 is dc coupled to Q840, and for low-speed signals, Q845 acts as a current source. Fast transitions couple through C845, providing added current gain through Q845 for fast voltage swings at the output of the Amplifier.

Store Z-Axis signals, controlled by the Display Controller, are applied to the Z-Axis amplifier at the emitter of Q829. The Nonstore Z-Axis signals are shunted away from Q829 by CR824, which is forward biased from the CHOP Blanking circuit (Diagram 2) during STORE mode displays. The overall store waveform and readout character intensity level is set by the STORAGE/READOUT INTENSITY control (see Diagram 13). The level setting of that control sets the Z-Axis drive current supplied to the Z-Axis Amplifier by Q829 during digitally controlled displays. When the Display Controller turns off Q7203, Q7202, or Q7201, the current normally shunted away from the emitter of Q829 is added via the forward biased diode connected to the emitter of the cutoff transistor. With more current available from Q7204, more current flows in Q829 to intensify the crt display.

The intensity of the Nonstore crt display in the A, B, and Alt Horizontal modes is set by the INTENSITY controls and associated circuitry. The A INTENSITY potentiometer controls the base voltage of Q804 to set the amount of emitter current that flows through that transistor and, therefore, the level of the Z-Axis signal. Likewise the B INTENSITY potentiometer controls the base voltage of Q814 and the intensity of the B and Alt Sweep displays.

When only the Nonstore A Sweep is displayed, Q586 and Q583 are biased off. The current through R818, as set by the A INTENSITY potentiometer, flows through CR818 and Q825 to fix the voltage level at the Z-Axis Amplifier output. For a B-Only display, Q586 is biased on to reverse bias CR818 and prevent A-Intensity current from reaching Q825. Current set by the base voltage of Q814 flows through CR817 to Q825 and sets the B Sweep intensity. For an alternating A and B display, Q586 is biased off when the A Sweep is displayed. During the portion of the A Sweep in which the B Sweep runs, current from R816 is passed through CR816 by the Alternate Display Switching and the Unblanking Logic circuitry to produce an intensified zone on the A Sweep trace.

When CHOP VERTICAL MODE is selected, the Chop Blanking signal is sent to the collector of Q825 through U537B and CR824 during the Nonstore display-switching time. Signal current is shunted away from CR825, and the forward bias of Q829 rises to the blanking level. When blanked, the output of the Z-Axis Amplifier drops to reduce the crt beam current below viewing intensity.

For a Nonstore X-Y display, CR818, CR817, and CR816 are reverse biased. The $\overline{XY}$ signal is LO to reverse bias CR551 and allow current in R820 to flow through CR820. The crt intensity is then controlled by the A INTENSITY potentiometer which sets the current in R820 through Q804.

During Nonstore operation, any applied External Z-Axis input voltages drive proportional input currents through R822 and R823 to the Z-Axis Amplifier. Sensitivity to external signals is determined by the transresistance gain of the shunt-feedback amplifier. Diode CR823 protects the Z-Axis Amplifier if excessive voltage levels are applied to the EXT Z AXIS INPUT connector. External Z-Axis modulation does not function for STORE MODE displays.

BEAM FIND switch S390 controls the base bias voltages of Q825 and Q829. When the BEAM FIND button is out, −8.6 V is supplied to the normal base-biasing network. When the button is held in, the −8.6 V supply is removed, and the voltage at the anode of VR828 rises to about −5.6 V. This voltage level turns off the current supply from Q829. The Z-Axis amplifier output voltage is then fixed by R835 and the voltage at the BEAM FIND switch, as set by other parts of the Beam Find circuitry. The output voltage of Q835 is set to a level that displays either a bright trace or dot (depending on whether the sweep is triggered or not), and the INTENSITY controls and the Z-Axis drive signals have no control over the crt intensity.

Hv Multiplier, Dc Restorer, and Crt

The Dc Restorer circuit sets the crt control-grid bias and couples the ac and dc components of the Z-Axis Amplifier output to the crt control grid. Direct coupling of the Z-Axis Amplifier output to the crt control grid is not employed due to the high potential differences involved. Refer to Figure 3-11 during the following discussion.

Ac drive to the Dc Restorer circuit is obtained from pin 16 of T948. The drive voltage has a peak amplitude of about ±100 V at a frequency of about 20 kHz and is coupled into the Dc Restorer circuit through C853 and R853. The cathode of CR851 is biased by the wiper voltage of Grid Bias potentiometer R851, and the ac-drive voltage is clamped whenever the positive peaks reach a level that forward biases CR851.

The Z-Axis Amplifier output voltage, which varies between +10 V and +75 V, is applied to the Dc Restorer at the anode of CR853. The ac-drive voltage holds CR853 reverse biased until the voltage falls below the Z-Axis Amplifier output voltage level. At that point, CR853 becomes forward biased and clamps the junction of

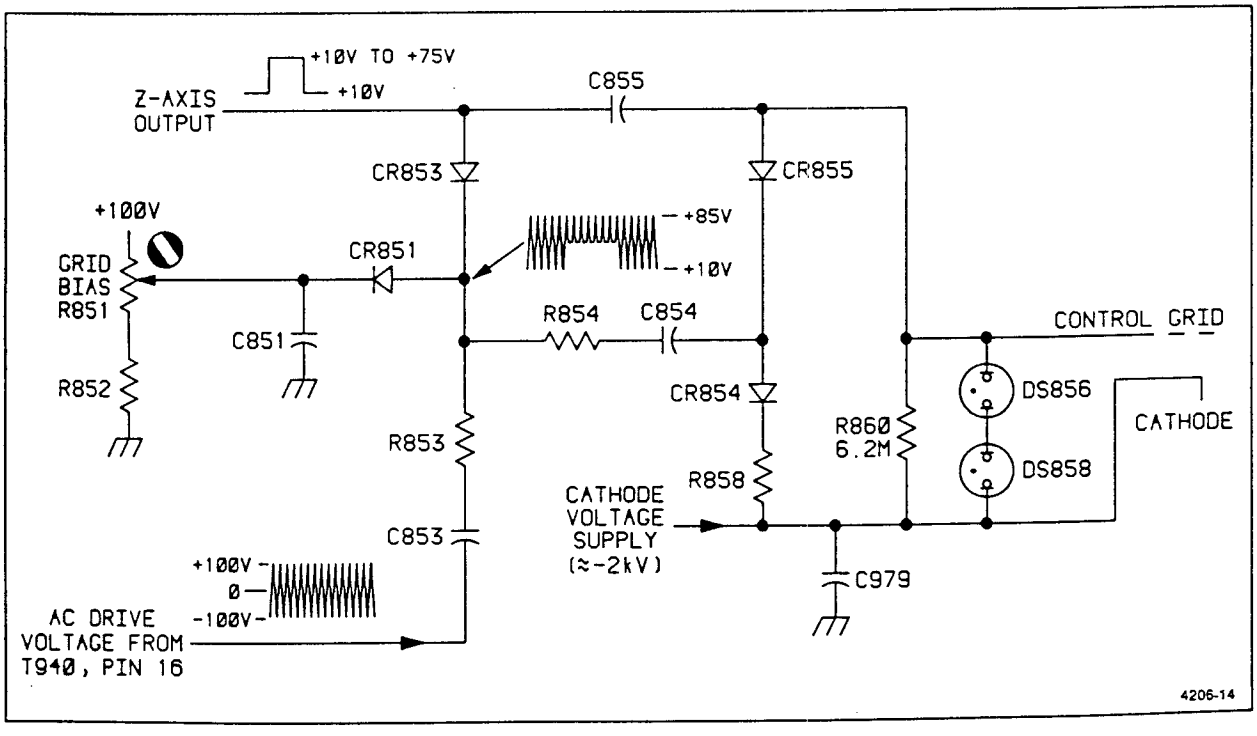


Figure 3-11. Simplified diagram of the Dc Restorer circuitry.

CR851, CR853, and R854 to the Z-Axis output level. Thus, the ac-drive voltage is clamped at two levels to produce a square-wave signal with a positive dc-offset level.

The Dc Restorer is referenced to the −2 kV crt cathode voltage through R858 and CR854. Initially, both C855 and C854 charge up to a level determined by the difference between the Z-Axis output voltage and the crt cathode voltage. Capacitor C855 charges from the Z-Axis output through R858, CR854, and CR855, to the crt cathode. Capacitor C854 charges through R858, CR854, R854, and CR853 to the crt cathode.

During the positive transitions of the ac drive, from the lower clamped level toward the higher clamped level, the charge on C854 increases due to the rising voltage. The voltage increase across C854 is equal to the amplitude of the positive transition. The negative transition is coupled through C854 to reverse bias CR854 and to forward bias CR855. The increased charge of C854 is then transferred to C855 as C854 discharges toward the Z-Axis output level. Successive cycles of the ac input to the Dc Restorer charge C855 to a voltage equal to the initial level plus the amplitude of the clamped square-wave input.

The charge held by C855 sets the control-grid bias voltage. If more charge is added to that already present on C855, the control grid becomes more negative, and less crt writing-beam current flows. Conversely, if less charge is added, the control-grid voltage level becomes closer to the cathode-voltage level, and more crt writing-beam current flows.

During periods that C854 is charging, the crt control-grid voltage is held constant by the long time-constant discharge path of C855 through R860.

Fast-rise and fast-fall transitions of the Z-Axis output signal are coupled to the crt control grid through C855 to start the crt writing-beam current toward the new intensity level. The Dc Restorer output level then follows the Z-Axis output-voltage level to set the new bias voltage for the crt control grid.

Neon lamps DS858 and DS856 protect the crt from excessive grid-to-cathode voltage if the potential on either the control grid or the cathode is lost for any reason.

High-voltage multiplier U975 uses the 2-kV winding of T948 to generate 12 kV to drive the crt anode. An internal half-wave rectifier diode in the multiplier produces −2 kV for the crt cathode. The −2 kV supply is filtered by a low-pass filter formed by C975, C976, R976, R978, and C979.

Neon lamp DS870 protects against excessive voltage between the crt heater and crt cathode by conducting if the voltage exceeds approximately 75 V.

Focus voltage is also developed from the −2 kV supply by a voltage divider formed by R894, R892, FOCUS potentiometer R893, R891, R890, R889, R888, and R886.

X-Y PLOTTER

The X-Y plotter circuitry (see Diagram 22) drives the internal circuitry for the external clock, and an external XY Plotter, if connected.

External Clock

The TTL compatible (active LO) $\overline{\text{EXT CLK}}$ signal, accessed through the AUXILIARY CONNECTOR (J1011 pin 1), drives the external clock circuitry (active HI) of the oscilloscope through internal connector J4110 pin 1.

Operational amplifier U1001A, PNP transistor Q1011, and associated components buffer and invert the external clock signal $\overline{\text{EXT CLK}}$. Input bias resistors R1011, R1014, and R1015 condition the $\overline{\text{EXT CLK}}$ input signal. The same three resistors protect the external clock circuitry from over-voltage and reverse-voltage inputs. Resistor R1016 provides hysteresis.

Operational amplifier U1001A serves as a buffer and amplifier. Even though $\overline{\text{EXT CLK}}$ only swings from 0 V to +5 V maximum, the input bias resistors produce plus and minus voltage swings of ≤2 V at non-inverting input U1001A pin 3. The amplifier output U1001A pin 1 has a plus and minus 7 V range which, through current limit resistor R1017, overdrives the base of Q1011. This base current overdrive assures a fast clean rise and fall time of the EXT CLK output signal (J4110 pin 1) required by the oscilloscopes external clock circuit input.

The emitter of Q1011 goes to +5 V_k and the collector goes to both the EXT CLK output and to level-shift resistor R1012. Level-shift resistor R1012 makes the EXT CLK output a valid TTL LO when Q1011 is shut off. The EXT CLK output is an active HI TTL drive.

Shield Ground

The SHIELD GND connection (J1011 pin 4) is the chassis ground connection for cable shield connections.

Signal Ground

The AUXILIARY CONNECTOR SIG GND connection (J1011 pin 9) is the ground point for all signal path ground returns.

Pen-Down Circuit

The Pen-Down circuitry controls the pen mechanism of an external X-Y plotter or the motor drive of a Y-T strip chart recorder.

The Pen-Down circuit is comprised of operational amplifier U1001B, transistor Q1012, relay K1001, and related components. The $\overline{\text{PEN DWN}}$ signal (J6423 pin 1) drives the non-inverting input of the operational amplifier (U1001B pin 5). The inverting input of the operational amplifier (U1001B pin 6) is tied to ground. The operational amplifier output, U1001B pin 7, goes to the base of PNP relay-drive transistor Q1012, through current limiting resistor R1005. This amplifier has no negative feedback resistor and operates in an open-loop gain configuration. Small input signals therefore drive the output near one rail or the other. The output signal resembles a square wave, regardless of the input waveform.

Transistor Q1012 inverts the signal and drives relay K1001. Diode CR1016 protects the transistor from inductive kick-back voltages generated by the relay's collapsing magnetic field as the transistor turns off. Fuse F1001, in the RELAY COMM signal path, provides over-current protection for all relay contact configurations.

When the $\overline{\text{PEN DWN}}$ signal on U1001B pin 5 goes negative, the output on pin 7 of the operational amplifier also goes negative, turning on transistor Q1012 and energizing the relay coil. When the relay is energized, the relay common to normally closed connection opens and the relay common to normally open connection closes. When $\overline{\text{PEN DWN}}$ returns to a positive level, the transistor shuts off. The relay's coil discharges its kick-back current through diode CR1016, and the relay common returns to its normally closed position.

In order to drive both an X-Y plotter and a Y-T strip chart recorder, the Pen-Down circuitry does double duty. With an X-Y plotter, the circuitry simply lowers the plotter pen. with a Y-T strip chart recorder, the pen-down circuitry is actually a motor drive control circuit. This double duty is accomplished by providing the Pen-Down signal to the operational amplifier about 1 s prior to the signals being provided to X & Y plot output circuitry. This allows the motor to have time to start up before signals are applied to the Y plot output circuit. The circuit can not differentiate between X-Y plotters and Y-T strip chart recorders, therefore the time delay from $\overline{\text{PEN DWN}}$ to X and Y channel information output is the same in each case.

X and Y Amplifiers

The X and Y amplifiers drive the X and Y outputs. Because both amplifiers operate the same, only the X-PLOT amplifier is discussed in detail.

Input signal X PLOT goes to the non-inverting input of unity gain amplifier U1001C pin 10. The output of the operational amplifier is fed to auxiliary connector J1011 pin 3 through resistor R1002. The resistor limits the output current and is part of the amplifier's protection network. The X-PLOT protection network consists of diodes CR1003, CR1011, R1002, VR1012, and VR1011. If the X output goes above 5.8 V peak, VR1011 and CR1011 turn on, clipping U1001C pin 8 to about +6 V. If output goes below −5.8 V peak, VR1012 and CR1003 turn on, clipping U1001C pin 8 to about −6 V. The Y-PLOT protection components are CR1001, CR1002, R1001, VR1012, and VR1011.

Power Supplies

The filters for all supplies are pi filters, consisting of two filter caps to ground, one on each side of a series choke.

Each filter circuit for the three supplies filter in both directions. The filters reduce noise on the power supply lines generated elsewhere in the instrument, and they also reduce noise generated by the X-Y plotter board as the noise goes back out to the supplies in the rest of the instrument. Capacitors C1003, C1004, and C1005 decouple and by-pass the supplies.

The +4.2 V output makes interfacing to various X-Y and Y-T devices easier. The +5 V_g goes to the anode of reverse voltage protection diode CR1014. The diode drops the voltage to +4.2 V. The +4.2 V goes through current limit resistor R1013 to the auxiliary connector output (J1011 pin 6).

PERFORMANCE CHECK PROCEDURE

INTRODUCTION

PURPOSE

The "Performance Check Procedure" is used to verify the instrument's Performance Requirements statements listed in Table 1-1 and to determine the need for calibration. The performance checks may also be used as an acceptance test or as a preliminary troubleshooting aid.

PERFORMANCE CHECK INTERVAL

To ensure instrument accuracy, check its performance after every 2000 hours of operation or once each year, if used infrequently. A more frequent interval may be necessary if the instrument is subjected to harsh environments or severe usage.

STRUCTURE

The "Performance Check Procedure" is structured in subsections to permit checking individual sections of the instrument whenever a complete Performance Check is not required. At the beginning of each subsection there is an equipment-required list showing only the test equipment necessary for performing the steps in that subsection. In this list, the Item number that follows each piece of equipment corresponds to the Item number listed in Table 4-1.

Also at the beginning of each subsection is a list of all the front-panel control settings required to prepare the instrument for performing Step 1 in that subsection. Each succeeding step within a particular subsection should then be performed, both in the sequence presented and in its entirety, to ensure that control-setting changes will be correct for ensuing steps.

TEST EQUIPMENT REQUIRED

The test equipment listed in Table 4-1 is a complete list of the equipment required to accomplish both the "Performance Check Procedure" in this section and the "Adjustment Procedure" in Section 5. Test equipment specifications described in Table 4-1 are the minimum necessary to provide accurate results. Therefore, equipment used must meet or exceed the listed specifications. Detailed operating instructions for test equipment are not given in this procedure. If more operating information is required, refer to the appropriate test equipment instruction manual.

When equipment other than that recommended is used, control settings of the test setup may need to be altered. If the exact item of equipment given as an example in Table 4-1 is not available, check the "Minimum Specification" column to determine if any other available test equipment might suffice to perform the check or adjustment.

LIMITS AND TOLERANCES

The tolerances given in this procedure are valid for an instrument that is operating in and has been previously calibrated in an ambient temperature between +20°C and +30°C. The instrument also must have had at least a 20-minute warm-up period. Refer to Table 1-1 for tolerances applicable to an instrument that is operating outside this temperature range. All tolerances specified are for the instrument only and do not include test-equipment error.

PREPARATION FOR CHECKS

It is not necessary to remove the instrument cover to accomplish any subsection in the "Performance Check Procedure," since all checks are made using operator-accessible front- and rear-panel controls and connectors.

The most accurate display adjustments are made with a stable, well-focused, low-intensity display. Unless otherwise noted, adjust the A and B INTENSITY, STORAGE/READOUT INTENSITY, FOCUS, and TRIGGER LEVEL controls as needed to view the display.

Table 4-1

Test Equipment Required

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
1. Calibration Generator	Standard-amplitude signal levels: 5 mV to 50 V. Accuracy: ±0.3%. High-amplitude signal levels: 1 V to 60 V. Repetition rate: 1 kHz. Fast-rise signal level: 1 V. Repetition rate: 1 MHz. Rise time: 1 ns or less. Flatness: ±2%.	Signal source for gain and transient response.	TEKTRONIX PG 506 Calibration Generator.[a]
2. Leveled Sine-Wave Generator	Frequency: 250 kHz to above 100 MHz. Output amplitude: variable from 10 mV to 5 V p-p. Output impedance: 50 Ω. Reference frequency: 50 kHz. Amplitude accuracy: constant within 3% of reference frequency as output frequency changes.	Vertical, horizontal, and triggering checks and adjustments. Display adjustments and Z-Axis check.	TEKTRONIX SG 503 Leveled Sine-Wave Generator.[a]
3. Time-Mark Generator	Marker outputs: 10 ns to 0.5 s. Marker accuracy: ±0.1%. Trigger output: 1 ms to 0.1 μs, time-coincident with markers.	Horizontal checks and adjustments. Display adjustment.	TEKTRONIX TG 501 Time-Mark Generator.[a]
4. Low-Frequency Generator	Range: 1 kHz to 500 kHz. Output amplitude: 300 mV. Output impedance: 600 Ω. Reference frequency: constant within 0.3 dB of reference frequency as output frequency changes.	Low-frequency trigger checks.	TEKTRONIX SG 502 Oscillator.[a]
5. Pulse Generator	Repetition rate: 1 kHz. Output amplitude: 5 V.	External clock and storage checks.	TEKTRONIX PG 501 Pulse Generator.[a]
6. Test Oscilloscope with 10X Probes	Bandwidth: dc to 100 MHz. Minimum deflection factor: 5 mV/div. Accuracy: ±3%.	General troubleshooting, holdoff check.	TEKTRONIX 2235 Oscilloscope.
7. Digital Voltmeter (DMM)	Range: 0 to 140 V. Dc voltage accuracy: ±0.15%. 4 1/2 digit display.	Power supply checks and adjustments. Vertical adjustment.	TEKTRONIX DM 501A Digital Multimeter.[a]
8. Coaxial Cable (2 required)	Impedance: 50 Ω. Length: 42 in. Connectors: BNC.	Signal interconnection.	Tektronix Part Number 012-0057-01.
9. Dual-Input Coupler	Connectors: BNC female-to-dual-BNC male.	Signal interconnection.	Tektronix Part Number 067-0525-01.
10. Coupler	Connectors: BNC female-to-BNC female.	Signal interconnection.	Tektronix Part Number 103-0028-00.
11. T-Connector	Connectors: BNC.	Signal interconnection.	Tektronix Part Number 103-0030-00.
12. Termination	Impedance: 50 Ω. Connectors: BNC.	Signal termination.	Tektronix Part Number 011-0049-01.

[a]Requires a TM 500-Series Power Module.

Table 4-1 (cont)

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
13. Termination	Impedance: 600 Ω. Connectors: BNC.	Signal termination.	Tektronix Part Number 011-0092-00.
14. 10X Attenuator	Ratio: 10X. Impedance: 50 Ω. Connectors: BNC.	Vertical compensation and triggering checks.	Tektronix Part Number 011-0059-02.
15. 2X Attenuator	Ratio: 2X. Impedance: 50 Ω. Connectors: BNC.	External triggering checks.	Tektronix Part Number 011-0069-02.
16. Adapter	Connectors: BNC male-to-miniature-probe tip.	Signal interconnection.	Tektronix Part Number 013-0084-02.
17. Adapter	Connectors: BNC male-to-tip plug.	Signal interconnection.	Tektronix Part Number 175-1178-00.
18. Low-Capacitance Alignment Tool	Length: 1-in. shaft. Bit size: 3/32 in.	Adjust variable capacitors.	J.F.D. Electronics Corp. Adjustment Tool Number 5284.
19. Screwdriver	Length: 3-in. shaft. Bit size: 3/32 in.	Adjust variable resistors.	Xcelite R-3323.

INDEX TO PERFORMANCE CHECK STEPS

Vertical

	Page
1. Check Deflection Accuracy and Variable Range	4-4
2. Check Store Deflection Accuracy	4-5
3. Check Save Expansion and Compression	4-5
4. Check Position Range	4-6
5. Check Acquisition Position Registration	4-6
6. Check Non Store Aberrations	4-6
7. Check Store Aberrations	4-7
8. Check Bandwidth	4-7
9. Check Repetitive Store Mode and Bandwidth	4-8
10. Check Single Sweep Sample Acquisition	4-8
11. Check Bandwidth Limit Operation	4-8
12. Check Common-Mode Rejection Ratio	4-8
13. Check Non Store and Store Channel Isolation	4-9
14. Check Store Mode Cross Talk	4-10
15. Check Store Pulse Width Amplitude	4-10
16. Check Average Mode	4-11

Horizontal

	Page
1. Check Timing Accuracy and Linearity	4-12
2. Check Store Differential and Cursor Time Difference Accuracy	4-13
3. Check Variable Range and Sweep Separation	4-14
4. Check Delay Time Differential Accuracy	4-14
5. Check Delay Jitter	4-15
6. Check Position Range	4-15
7. Check Store Expansion Range	4-15
8. Check 4K to 1K Display Compress	4-16
9. Check Non Store Sweep Length	4-16
10. Check X Gain	4-16
11. Check X Bandwidth	4-16

Trigger

	Page
1. Check Internal A and B Triggering	4-17
2. Check HF Reject A Triggering	4-18
3. Check External Triggering	4-19
4. Check External Trigger Ranges	4-19
5. Check Single Sweep Operation	4-19
6. Check Acquisition Window Trigger Point	4-20

External Z-Axis, Probe Adjust, External Clock and X-Y Plotter

	Page
1. Check External Z-Axis Operation	4-21
2. Check Probe Adjust Operation	4-21
3. Check External Clock	4-22
4. Check X-Y Plotter	4-22

VERTICAL

Equipment Required (see Table 4-1):

- Calibration Generator (Item 1)
- Leveled Sine-Wave Generator (Item 2)
- 50 Ω BNC Cable (Item 8)
- Dual-Input Coupler (Item 9)
- 50 Ω BNC Termination (Item 12)
- 10X Attenuator (Item 14)

INITIAL CONTROL SETTINGS

Vertical (Both Channels)

POSITION	Midrange
VERTICAL MODE	CH 1
X-Y	Off (button out)
BW LIMIT	On (button in)
VOLTS/DIV	2 mV
VOLTS/DIV Variable	CAL detent
INVERT	Off (button out)
AC-GND-DC	DC

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
A SEC/DIV	20 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A Trigger

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT
A EXT COUPLING	AC

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Check Deflection Accuracy and Variable Range

a. Connect the standard-amplitude signal from the Calibration Generator via a 50 Ω cable to the CH 1 OR X input connector.

b. CHECK—Deflection accuracy is within the limits given in Table 4-2 for each CH 1 VOLTS/DIV switch setting and corresponding standard-amplitude signal. When at the 20 mV VOLTS/DIV switch setting, rotate the CH 1 VOLTS/DIV Variable control fully counterclockwise and CHECK that the display decreases to 2 divisions or less. Then return the CH 1 VOLTS/DIV Variable control to the CAL detent and continue with the 50 mV check.

Table 4-2

Deflection Accuracy Limits

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Accuracy Limits (Divisions)
2 mV	10 mV	4.90 to 5.10
5 mV	20 mV	3.92 to 4.08
10 mV	50 mV	4.90 to 5.10
20 mV	0.1 V	4.90 to 5.10
50 mV	0.2 V	3.92 to 4.08
0.1 V	0.5 V	4.90 to 5.10
0.2 V	1 V	4.90 to 5.10
0.5 V	2 V	3.92 to 4.08
1 V	5 V	4.90 to 5.10
2 V	10 V	4.90 to 5.10
5 V	20 V	3.92 to 4.08

c. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the VERTICAL MODE switch to CH 2.

d. Repeat part b using the Channel 2 controls.

2. Check Store Deflection Accuracy

a. Set:

CH 2 VOLTS/DIV	2 mV
STORE/NON STORE	STORE (button in)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)

b. Use the CURSORS control and SELECT C1/C2 switch to set one cursor at the bottom and the other cursor at the top of the square wave.

c. CHECK—Deflection accuracy is within the limits given in Table 4-3 for each CH 2 VOLTS/DIV switch setting and corresponding standard-amplitude signal.

Table 4-3

Storage Deflection Accuracy

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Divisions of Deflection	Voltage Readout Limits
2 mV	10 mV	4.90 to 5.10	9.80 to 10.20 mV
5 mV	20 mV	3.92 to 4.08	19.6 to 20.4 mV
10 mV	50 mV	4.90 to 5.10	49.0 to 51.0 mV
20 mV	0.1 V	4.90 to 5.10	98.0 to 102.0 mV
50 mV	0.2 V	3.92 to 4.08	198.0 to 204.0 mV
0.1 V	0.5 V	4.90 to 5.10	0.490 to 0.510 V
0.2 V	1 V	4.90 to 5.10	0.980 to 1.020 V
0.5 V	2 V	3.92 to 4.08	1.960 to 2.040 V
1 V	5 V	4.90 to 5.10	4.90 to 5.10 V
2 V	10 V	4.90 to 5.10	9.80 to 10.20 V
5 V	20 V	3.92 to 4.08	19.60 to 20.40 V

d. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. set the VERTICAL MODE switch to CH 1.

e. Repeat parts b and c using the Channel 1 controls.

3. Check Save Expansion and Compression

a. Set the CH 1 VOLTS/DIV switch to 0.1 V.

b. Set the generator to produce a 0.5 div standard-amplitude signal.

c. Set the SAVE/CONTINUE switch to SAVE (button in).

d. Set the CH 1 VOLTS/DIV switch to 10 mV and reposition the display.

e. CHECK—The display is expanded to 5 divisions in amplitude.

f. Set:

CH 1 VOLTS/DIV	0.1 V
SAVE/CONTINUE	CONTINUE (button out)

g. Set the generator to produce a 5 division standard-amplitude signal.

h. Set the SAVE/CONTINUE switch to SAVE (button in).

i. Set the CH 1 VOLTS/DIV switch to 1 V.

j. CHECK—The display is compressed to 0.5 division in amplitude.

k. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

l. Set:

VERTICAL MODE	CH 2
SAVE/CONTINUE	CONTINUE (button out)

m. Repeat parts a through j.

4. Check Position Range

a. Set:

VOLTS/DIV (both)	50 mV
AC-GND-DC (both)	AC
STORE/NON STORE	NON STORE (button out)

b. Set the generator to produce a 0.5 V standard-amplitude signal.

c. Adjust the CH 2 VOLTS/DIV Variable control to produce a 4.4 division display. Set the CH 2 VOLTS/DIV switch to 10 mV.

d. CHECK—The bottom and top of the trace may be positioned above and below the center horizontal graticule line by rotating the Channel 2 POSITION control fully clockwise and counterclockwise respectively.

e. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the VERTICAL MODE switch to CH 1.

f. Repeat parts c and d using the Channel 1 controls.

g. Disconnect the test equipment from the instrument.

5. Check Acquisition Position Registration

a. Set:

VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	GND
A SEC/DIV	10 μs
SAVE/CONTINUE	CONTINUE (button out)

b. Position the trace exactly on the center horizontal graticule line using the Channel 1 POSITION control and position the trace start to the left most vertical graticule line.

c. Set STORE/NON STORE switch to STORE (button in).

d. CHECK— Trace remains within 0.5 division of the center horizontal graticule line and the trace start is within 0.5 division of the left vertical graticule line.

e. Set:

VERTICAL MODE	CH 2
STORE/NON STORE	NON STORE

f. Repeat parts b through d for Channel 2 trace.

g. Position the trace 0.5 division below the top horizontal graticule line using the Channel 2 POSITION control.

h. Set SAVE/CONTINUE switch to SAVE (button in).

i. CHECK—Trace shift of 0.5 division or less.

j. Set SAVE/CONTINUE switch to CONTINUE (button out).

k. Position the trace 0.5 division above the bottom horizontal graticule line using the Channel 2 POSITION control.

l. Set SAVE/CONTINUE switch to SAVE (button in).

m. CHECK—Trace shift of 0.5 division or less.

n. Set SAVE/CONTINUE switch to CONTINUE (button out).

o. Set the VERTICAL MODE switch to CH 1.

p. Repeat steps g through l for Channel 1 trace.

6. Check Non Store Aberrations

a. Set:

BW LIMIT	Off (button out)
VOLTS/DIV (both)	2 mV
AC-GND-DC (both)	DC
A SEC/DIV	0.05 μs
STORE/NON STORE	NON STORE (button out)

b. Connect the fast-rise, positive-going square-wave output via a 50 Ω cable, a 10X attenuator, and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 1 MHz, 5-division display.

d. CHECK—Display aberrations are within 4% (0.2 division or less) for the following VOLTS/DIV switch settings: 5 mV through 50 mV. Adjust the generator output and attach or remove the 10X attenuator as necessary to maintain a 5-division display at each VOLTS/DIV switch setting.

e. CHECK—Display aberrations are within 6% (0.25 division or less) for the following VOLTS/DIV switch settings: 0.1 V through 0.5 V. Adjust the generator output and attach or remove the 10X attenuator as necessary to maintain a 5-division display at each VOLTS/DIV switch setting.

f. Disconnect the cable from the CH 1 OR X input connector. Reconnect the 10X attenuator (if previously removed) and reduce the generator amplitude to minimum.

g. Connect the cable to the CH 2 OR Y input connector and set the VERTICAL MODE switch to CH 2.

h. Set the generator to produce a 5-division display.

i. Repeat parts d and e using the Channel 2 controls.

7. Check Store Aberrations

a. Reconnect the 10X attenuator and 50 Ω termination (if previously removed) and reduce the generator amplitude to minimum.

b. Set the CH 2 VOLTS/DIV switch to 2 mV.

c. Set the generator to produce a 5-division display.

d. Set:

STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)

e. Allow acquisition cycle to complete and press in the SAVE/CONTINUE button to SAVE (button in).

f. CHECK—Display aberrations are within 4% (0.2 division or less).

g. Repeat part f for each of the following VOLTS/DIV switch settings: 5 mV through 0.5 V. Adjust the generator output and attach or remove the 10X attenuator as necessary to maintain a 5-division display at each VOLTS/DIV switch setting.

h. Disconnect the cable from the CH 2 OR Y input connector. Reconnect the 10X attenuator (if previously removed) and reduce the generator amplitude to minimum.

i. Connect the cable to the CH 1 OR X input connector and set the VERTICAL MODE switch to CH 1.

j. Set the generator to produce a 5-division display.

k. Repeat parts e and f using the Channel 1 controls.

l. Disconnect the test equipment from the instrument.

8. Check Bandwidth

a. Set:

VOLTS/DIV (both)	2 mV
A SEC/DIV	0.2 ms
STORE/NON STORE	NON STORE (button out)

b. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 2 OR Y input connector.

c. Set the generator to produce a 50 kHz, 6-division display.

d. CHECK—Display amplitude is 4.2 divisions or greater as the generator output frequency is increased up to the value shown in Table 4-4 for the corresponding VOLTS/DIV switch setting.

Table 4-4

Settings for Bandwidth Checks

VOLTS/DIV Switch Setting	Generator Output Frequency
2 mV	80 MHz
5 mV to 5 V	100 MHz

e. Repeat parts c and d for all indicated CH 2 VOLTS/DIV switch settings, up to the output-voltage upper limit of the sine-wave generator being used.

f. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

g. Set the VERTICAL MODE switch to CH 1.

h. Repeat parts c and d for all indicated CH 1 VOLTS/DIV switch settings, up to the output-voltage upper limit of the sine-wave generator being used.

9. Check Repetitive Store Mode and Bandwidth

a. Set:

CH 1 VOLTS/DIV	10 mV
A SEC/DIV	0.2 ms

b. Set the generator to produce a 50 kHz, 6-division display.

c. Set:

A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

d. Set the generator to produce a 100 MHz display.

e. Set:

STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)

NOTE

Allow the points to accumulate for a few seconds before saving the display.

f. CHECK—The 100 MHz display will accumulate and store.

g. CHECK—Display amplitude is 4.2 divisions or greater.

h. Set the VERTICAL MODE switch to BOTH and ALT.

i. Repeat parts f and g.

10. Check Single Sweep Sample Acquisition

a. Set:

VERTICAL MODE	CH 1
A SEC/DIV	5 μs
X10 Magnifier	Off (knob in)
A TRIGGER Mode	NORM
A&B INT	CH 1
SAVE/CONTINUE	CONTINUE (button out)
1K/4K	1K (button in)

b. Set the generator to produce a 50 kHz, 6-division display.

c. Set:

Channel 1 AC-GND-DC	GND
A TRIGGER	SGL SWP

d. Set the generator output to 2 MHz.

e. Set the AC-GND-DC switch to DC.

f. CHECK—The minimum peak-to-peak envelope amplitude is greater than 5.6 divisions.

11. Check Bandwidth Limit Operation

a. Set:

BW LIMIT	On (button in)
CH 1 VOLTS/DIV	10 mV
AC-GND-DC	DC
A SEC/DIV	20 μs
A TRIGGER	P-P AUTO
A&B INT	VERT MODE
STORE/NON STORE	NON STORE (button out)

b. Set the generator to produce a 50 kHz, 6-division display.

c. Increase the generator output frequency until the display amplitude decreases to 4.2 divisions.

d. CHECK—Generator output frequency is between 18 and 22 MHz.

e. Disconnect the test equipment from the instrument.

12. Check Common-Mode Rejection Ratio

a. Set:

BW LIMIT	Off (button out)
CH 2 VOLTS/DIV	10 mV
INVERT	On (button in)

b. Connect the leveled sine-wave generator output via a 50 Ω cable, a 50 Ω termination, and a dual-input coupler to the CH 1 OR X and the CH 2 OR Y input connectors.

c. Set the generator to produce a 50 MHz, 6-division display.

d. Vertically center the display using the Channel 1 POSITION control. Then set the VERTICAL MODE switch to CH 2 and vertically center the display using the Channel 2 POSITION control.

e. Set the VERTICAL MODE switches to BOTH and ADD.

f. CHECK—Display amplitude is 0.6 division or less.

g. If the check in part f meets the requirement, skip to part p. If it does not, continue with part h.

h. Set the VERTICAL MODE switch to CH 1.

i. Set the generator to produce a 50 kHz, 6-division display.

j. Set the VERTICAL MODE switch to BOTH.

k. Adjust the CH 1 or CH 2 VOLTS/DIV Variable control for minimum display amplitude.

l. Set the VERTICAL MODE switch to CH 1.

m. Set the generator to produce a 50 MHz, 6-division display.

n. Set the VERTICAL MODE switch to BOTH.

o. CHECK—Display amplitude is 0.6 division or less.

p. Disconnect the test equipment from the instrument.

13. Check Non Store and Store Channel Isolation

a. Set:

VERTICAL MODE	CH 1
VOLTS/DIV (both)	0.1 V
VOLTS/DIV Variable (both)	CAL detent
INVERT	Off (button out)
Channel 1 AC-GND-DC	AC
Channel 2 AC-GND-DC	GND
A SEC/DIV	0.1 μs

b. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50 MHz, 5-division display.

d. Set the VERTICAL MODE switch to CH 2.

e. CHECK—Display amplitude is 0.05 division or less.

f. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

g. Set:

VERTICAL MODE	CH 1
Channel 1 AC-GND-DC	GND
Channel 2 AC-GND-DC	AC

h. CHECK—Display amplitude is 0.05 division or less.

i. Set:

CH 2 VOLTS/DIV	50 mV
STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)

j. CHECK—Display amplitude is 0.1 division or less.

k. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

l. Set:

VERTICAL MODE	CH 1
CH 1 VOLTS/DIV	50 mV
CH 2 VOLTS/DIV	0.1 V
Channel 1 AC-GND-DC	GND
Channel 2 AC-GND-DC	AC

m. CHECK—Display amplitude is 0.1 division or less.

n. Disconnect the test equipment from the instrument.

14. Check Store Mode Cross Talk

a. Set:

VERTICAL MODE	BOTH and CHOP
VOLTS/DIV (both)	0.1 V
A SEC/DIV	10 μs

b. Connect the Pulse Generator pulse-period output via a 50 Ω cable and a 50 Ω termination to CH 1 OR X input connector.

c. Set the generator to produce a 100 kHz, 5-division display.

d. Use the Channel 1 POSITION control to center the display.

e. Set CH 1 VOLTS/DIV switch to 50 mV for a 10-division display.

f. CHECK—Display amplitude on Channel 2 is less than 1% (0.1 division).

g. Set the A SEC/DIV switch to 10 ms.

h. CHECK—Display amplitude on Channel 2 is less than 1% (0.1 division).

i. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

j. Set:

CH 2 VOLTS/DIV	0.1 V
Channel 1 AC-GND-DC	GND
Channel 2 AC-GND-DC	AC

k. Use the Channel 2 POSITION control to center the display.

l. Set CH 2 VOLTS/DIV switch to 50 mV for a 10-division display.

m. Repeat parts f through h for Channel 1.

15. Check Store Pulse Width Amplitude

a. Set:

VERTICAL MODE	CH 2
A SEC/DIV	1 ms
STORE/NON STORE	NON STORE (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	1K (button in)

b. Set the generator to produce a 1 ms period, 100 ns pulse duration, 5-division display.

c. Set the STORE/NON STORE switch to STORE (button in).

d. CHECK—The amplitude of the display is 2.5 divisions or greater.

e. Set the A SEC/DIV switch to 0.1 sec.

f. CHECK—The amplitude of the display is 2.5 divisions or greater.

g. Set ROLL/SCAN switch to ROLL (button in).

h. CHECK—The amplitude of the display is 2.5 divisions or greater.

i. Set:

VERTICAL MODE	BOTH and CHOP
A SEC/DIV	1 ms
STORE/NON STORE	NON STORE (button out)
ROLL/SCAN	SCAN (button out)

j. Set the generator to produce a 0.1 s period, 2 ms pulse duration, 5-division display.

k. Repeat parts c through h.

l. Set:

A SEC/DIV	1 ms
STORE/NON STORE	NON STORE (button out)
ROLL/SCAN	SCAN (button out)

m. Set the generator to produce a 1 ms period, 20 μs pulse duration, 5-division display.

n. Repeat parts c and d.

o. Disconnect the test equipment from the instrument.

16. Check Average Mode

a. Set the WAVEFORM REFERENCE/MENU SELECT switch to MENU SELECT (button out).

b. Use the Menu controls to select SWP LIMIT.

c. CHECK—The SWP LIMIT is adjustable from 1 to 2047 or NO LIMIT by rotating the CURSORS control.

HORIZONTAL

Equipment Required (see Table 4-1):

- Calibration Generator (Item 1)
- Leveled Sine-Wave Generator (Item 2)
- Time-Mark Generator (Item 3)
- 50 Ω BNC Cable (Item 8)
- 50 Ω BNC Termination (Item 12)

INITIAL CONTROL SETTINGS

Vertical

Channel 1 POSITION	Midrange
VERTICAL MODE	CH 1
X-Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	0.5 V
CH 1 VOLTS/DIV Variable	CAL detent
Channel 1 AC-GND-DC	DC

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
A SEC/DIV	0.05 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)
B DELAY TIME POSITION	Fully counterclockwise

B TRIGGER

SLOPE	OUT
LEVEL	Fully clockwise

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT
A EXT COUPLING	DC÷10

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Check Timing Accuracy and Linearity

a. Connect the time-mark generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

b. Select 50 ns time markers from the time-marker generator.

c. Use the Channel 1 POSITION control to center the display vertically. Adjust the A TRIGGER LEVEL control for a stable, triggered display.

d. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

e. CHECK—Timing accuracy is within 2% (0.16 division at the 10th vertical graticule line), and linearity is within 5% (0.1 division over any 2 of the center 8 divisions).

NOTE

For checking the timing accuracy of the A SEC/DIV switch settings from 50 ms to 0.5 s, watch the time marker tips only at the 2nd and 10th vertical graticule lines while adjusting the Horizontal POSITION control.

f. Repeat parts c through e for the remaining A SEC/DIV and time-mark generator setting combinations shown in Table 4-5 under the "Normal (X1)" column.

g. Set:

A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

Table 4-5

Settings for Timing Accuracy Checks

SEC/DIV Switch Setting	Time-Mark Generator Setting	
	Normal (X1)	X10 Magnified
0.05 μs	50 ns	10 ns
0.1 μs	0.1 μs	10 ns
0.2 μs	0.2 μs	20 ns
0.5 μs	0.5 μs	50 ns
1 μs	1 μs	0.1 μs
2 μs	2 μs	0.2 μs
5 μs	5 μs	0.5 μs
10 μs	10 μs	1 μs
20 μs	20 μs	2 μs
50 μs	50 μs	5 μs
0.1 ms	0.1 ms	10 μs
0.2 ms	0.2 ms	20 μs
0.5 ms	0.5 ms	50 μs
1 ms	1 ms	0.1 ms
2 ms	2 ms	0.2 ms
5 ms	5 ms	0.5 ms
10 ms	10 ms	1 ms
20 ms	20 ms	2 ms
50 ms	50 ms	5 ms
A Sweep Only		
0.1 s	0.1 s	10 ms
0.2 s	0.2 s	20 ms
0.5 s	0.5 s	50 ms

h. Select 10 ns time markers from the time-mark generator.

i. Use the Horizontal POSITION control to align the 1st time marker that is 25 ns beyond the start of the sweep with the 2nd vertical graticule line.

j. CHECK—Timing accuracy is within 3% (0.24 division at the 10th vertical graticule line), and linearity is within 5% (0.1 division over any 2 of the center 8 divisions). Exclude any portion of the sweep past the 100th magnified division.

k. Repeat parts i and j for the remaining A SEC/DIV and time-mark generator setting combinations shown in Table 4-5 under the "X10 Magnified" column.

l. Set:

HORIZONTAL MODE	B
A SEC/DIV	0.1 μs
B SEC/DIV	0.05 μs
X10 Magnifier	Off (knob in)

m. Repeat parts b through k for the B Sweep. Keep the A SEC/DIV switch one setting slower than the B SEC/DIV switch.

2. Check Store Differential and Cursor Time Difference Accuracy

a. Set:

Channel 1 AC-GND-DC	GND
HORIZONTAL MODE	A
A SEC/DIV	0.1 ms
X10 Magnifier	Off (knob in)
STORE/NON STORE	STORE (button in)
1K/4K	1K (button in)

b. Use the Channel 1 POSITION control to center the base line vertically and the Horizontal POSITION control to align the start of the trace with the 1st vertical graticule line.

c. Use the CURSORS control and SELECT C1/C2 switch to set one cursor exactly on the 2nd vertical graticule line and position the active cursor to the right using the CURSORS control until ΔT readout displays 0.800 ms.

d. CHECK—Graticule indication of cursor difference at the 10th vertical graticule line is within 0.16 division.

e. Set the Channel 1 AC-GND-DC switch to DC.

f. Select 0.1 ms time markers from the time-mark generator.

g. Align the 2nd time marker with the 2nd vertical graticule line using the Horizontal POSITION control.

h. Set the SAVE/CONTINUE switch to SAVE (button in) for a stable display.

i. Use the CURSORS control and SELECT C1/C2 switch to set the first cursor on the trailing edge of the 2nd time marker.

j. Press in the C1/C2 button to activate the second cursor.

k. Set the second cursor on the trailing edge of the 10th time marker at the same voltage level as on the 2nd time marker.

l. CHECK—The ΔT readout is between 0.798 ms and 0.802 ms.

m. Set the SAVE/CONTINUE switch to CONTINUE (button out).

n. Set the A SEC/DIV switch to 0.5 μs.

o. Select 0.5 μs time markers from the time-mark generator.

p. Align the 2nd time marker with the 2nd vertical graticule line using the Horizontal POSITION control.

NOTE

Allow the points to accumulate for a few seconds before saving the display.

q. Repeat parts h through k.

NOTE

Pulses with fast rise and fall times have only a few sample points and it may not be possible to place the cursors at exactly the same voltage levels.

r. CHECK—The ΔT readout is between 3.948 μs and 4.052 μs.

3. Check Variable Range and Sweep Separation

a. Set:

A and B SEC/DIV	0.2 ms
SEC/DIV Variable	Fully counterclockwise
STORE/NON STORE	NON STORE (button out)

b. Select 0.5 ms time markers from the time-mark generator.

c. CHECK—Time markers are 1 division or less apart.

d. Set:

Channel 1 AC-GND-DC	GND
SEC/DIV Variable	CAL detent
HORIZONTAL MODE	BOTH

e. Use the Channel 1 POSITION control to set the A Sweep at the center horizontal graticule line.

f. CHECK—The B Sweep can be positioned more than 3.5 divisions above and below the A Sweep when the A/B SWP SEP control is rotated fully clockwise and counterclockwise respectively.

4. Check Delay Time Differential Accuracy

a. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

b. Set the B DELAY TIME POSITION control fully counterclockwise.

c. CHECK—Intensified portion of the trace starts within 0.5 division of the start of the sweep.

d. Rotate the B DELAY TIME POSITION control fully clockwise.

e. CHECK—Intensified portion of the trace is past the 11th vertical graticule line.

f. Set the A and B SEC/DIV switch to 0.5 μs.

g. Repeat parts a through e.

h. Set:

Channel 1 AC-GND-DC	DC
B SEC/DIV	0.05 μs
B DELAY TIME POSITION	Fully counterclockwise

i. Select 0.5 μs time markers from the time-mark generator.

j. Rotate the B DELAY TIME POSITION control so that the top of the 2nd time marker on the B Sweep is aligned with a selected reference vertical line. Record the DLY> readout for part i.

k. Rotate the B DELAY TIME POSITION control fully clockwise until the top of the 10th time marker on the B Sweep is aligned with the same selected reference vertical line as in part j. Record the DLY> readout for part l.

l. CHECK—Delay time readout is within the limits given in Table 4-6 (Delay Readout Limits column) by subtracting the delay time reading in part j from part k.

m. Repeat parts k through l for the remaining B SEC/DIV and time-mark generator settings given in Table 4-6, check the 8-division delay time accuracy for each A SEC/DIV switch setting given in column 1 of the table.

Table 4-6

Settings for Delay Time Differential Checks

Time-Mark Generator and A SEC/DIV Settings	B SEC/DIV Setting	Eight Division Delay	Delay Readout Limits
0.5 μs	0.05 μs	4.000 μs	3.948 to 4.052 μs
5 μs	0.5 μs	40.00 μs	39.48 to 40.52 μs
50 μs	5 μs	400.0 μs	394.8 to 405.2 μs
0.5 ms	50 μs	4.000 ms	3.948 to 4.052 ms
5 ms	0.5 ms	40.00 ms	39.48 to 40.52 ms
50 ms	5 ms	400.0 ms	394.8 to 405.2 ms
0.5 s	50 ms	4.000 s	3.948 to 4.052 s

5. Check Delay Jitter

a. Set:

A SEC/DIV	0.5 ms
B SEC/DIV	0.5 μs
HORIZONTAL MODE	B

b. Select 50 μs time markers from the time-mark generator.

c. Rotate the B DELAY TIME POSITION control counterclockwise to position a time marker within the graticule area for each major dial division and CHECK that the jitter on the leading edge of the time marker does not exceed 2 divisions. Disregard slow drift.

6. Check Position Range

a. Set:

HORIZONTAL MODE	A
A SEC/DIV	10 μs

b. Select 10 μs time markers from the time-mark generator.

c. CHECK—Start of the sweep can be positioned to the right of the center vertical graticule line by rotating the Horizontal POSITION control fully clockwise.

d. CHECK—The 11th time marker can be positioned to the left of the center vertical graticule line by rotating the Horizontal POSITION control fully counterclockwise.

e. Select 50 μs time markers from the time-mark generator.

f. Align the 3rd time marker with the center vertical graticule line using the Horizontal POSITION control.

g. Set the X10 Magnifier knob to On (knob out).

h. CHECK—Magnified time marker can be positioned to the left of the center vertical graticule line by rotating the Horizontal POSITION control fully counterclockwise.

i. CHECK—Start of the sweep can be positioned to the right of the center vertical graticule line by rotating the Horizontal POSITION control fully clockwise.

7. Check Store Expansion Range

a. Set:

A SEC/DIV	0.1 μs
X10 Magnifier	Off (knob in)

b. Select 10 ns time markers from the time-mark generator.

c. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

d. Set the STORE/NON STORE switch to STORE (button in).

e. Set the X10 Magnifier knob to On (knob out).

f. CHECK—The time markers are 1 division apart.

8. Check 4K to 1K Display Compress

a. Set:

A SEC/DIV	50 μs
X10 Magnifier	Off (knob in)
1K/4K	4K (button out)

b. Select 0.1 ms time markers from the time-mark generator and check that the time markers are 2 divisions apart.

c. Rotate the SEC/DIV Variable control out of detent.

d. CHECK—For 2 time markers per division over the center 8 divisions.

9. Check Non Store Sweep Length

a. Set:

SEC/DIV Variable	CAL detent
STORE/NON STORE	NON STORE (button out).

b. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

c. CHECK—End of the sweep is to the right of the 11th vertical graticule line.

d. Disconnect the test equipment from the instrument.

10. Check X Gain

a. Set:

X-Y	On (button in)
CH 1 VOLTS/DIV	10 mV
Horizontal POSITION	Midrange

b. Connect the standard-amplitude signal from the Calibration Generator via a 50 Ω cable to the CH 1 OR X input connector.

c. Set the generator to produce a 50 mV signal.

d. Use the Channel 2 POSITION and Horizontal POSITION controls to center the display.

e. CHECK—Display is 4.85 to 5.15 horizontal divisions.

f. Disconnect the test equipment from the instrument.

11. Check X Bandwidth

a. Set the STORE/NON STORE switch to NON STORE (button out).

b. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 5-division horizontal display at an output frequency of 50 kHz.

d. Increase the generator output frequency to 2.5 MHz.

e. CHECK—Display is at least 3.5 horizontal divisions.

f. Disconnect the test equipment from the instrument.

TRIGGER

Equipment Required (see Table 4-1):

- Leveled Sine-Wave Generator (Item 2)
- Low Frequency Generator (Item 4)
- 50 Ω BNC Cable (Item 8)
- Dual-Input Coupler (Item 9)
- 50 Ω BNC Termination (Item 12)
- 600 Ω BNC Termination (Item 13)

INITIAL CONTROL SETTINGS

Vertical

POSITION (both)	Midrange
VERTICAL MODE	CH 1
X-Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	5 mV
CH 2 VOLTS/DIV	50 mV
VOLTS/DIV Variable (both)	CAL detent
INVERT	Off (button out)
AC-GND-DC (both)	DC

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
A and B SEC/DIV	0.2 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)
B DELAY TIME POSITION	Fully counterclockwise

B TRIGGER

SLOPE	OUT
LEVEL	Midrange

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	CH 1
A SOURCE	INT
A EXT COUPLING	DC

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Check Internal A and B Triggering

a. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

b. Set the generator to produce a 10 MHz, 3.5-division display.

c. Set the CH 1 VOLTS/DIV switch to 50 mV.

d. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 4-7.

e. Set the HORIZONTAL MODE switch to B.

f. CHECK—Stable display can be obtained by adjusting the B TRIGGER LEVEL control to a position other than the B RUNS AFTER DLY position for both the OUT and IN positions of the B TRIGGER SLOPE switch.

Table 4-7

Switch Combinations for A Triggering Checks

A TRIGGER Mode	A TRIGGER SLOPE
NORM	OUT
NORM	IN
P-P AUTO	IN
P-P AUTO	OUT

g. Set:

VERTICAL MODE	CH 2
HORIZONTAL MODE	A
A&B INT	CH 2

h. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

i. Repeat parts d through f.

j. Set:

HORIZONTAL MODE	A
A SEC/DIV	0.1 μs
X10 Magnifier	On (knob out)

k. Set the generator to produce a 60 MHz, 1.0-division display.

l. Repeat parts d through f.

m. Set:

VERTICAL MODE	CH 1
HORIZONTAL MODE	A
A&B INT	CH 1

n. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

o. Repeat parts d through f.

p. Set:

HORIZONTAL MODE	A
A SEC/DIV	0.05 μs

q. Set the generator to produce a 100 MHz, 1.5-division display.

r. Repeat parts d through f.

s. Set:

VERTICAL MODE	CH 2
HORIZONTAL MODE	A
A&B INT	CH 2

t. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

u. Repeat parts d through f.

v. Disconnect the test equipment from the instrument.

2. Check HF Reject A Triggering

a. Set:

VERTICAL MODE	CH 1
VOLTS/DIV (both)	50 mV
HORIZONTAL MODE	A
A SEC/DIV	5 μs
X10 Magnifier	Off (knob in)
A TRIGGER Mode	NORM
A TRIGGER LEVEL	Midrange
A&B INT	CH 1

b. Connect the low-frequency generator output via a 50 Ω cable and a 600 Ω termination to the CH 1 OR X input connector.

c. Set the low-frequency generator output to produce a 250 kHz, 1-division display.

d. Adjust the A TRIGGER LEVEL control for a stable display.

e. Set HF REJECT switch to ON.

f. CHECK—Stable display cannot be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 4-7.

g. Set:

VERTICAL MODE	CH 2
A&B INT	CH 2

h. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

i. Repeat part f.

j. Disconnect the test equipment from the instrument.

3. Check External Triggering

a. Set:

VERTICAL MODE	CH 1
CH 1 VOLTS/DIV	5 mV
HORIZONTAL MODE	A
A SEC/DIV	0.1 μs
HF REJECT	OFF
A&B INT	CH 1
A SOURCE	EXT

b. Connect the leveled sine-wave generator output via a 50 Ω cable, a 50 Ω termination, and a dual-input coupler to both the CH 1 OR X and EXT INPUT connectors.

c. Set the leveled sine-wave generator output voltage to 40 mV and the frequency to 10 MHz.

d. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 4-7.

e. Set:

CH 1 VOLTS/DIV	50 mV
X10 Magnifier	On (knob out)

f. Set the generator output voltage to 120 mV and the frequency to 60 MHz.

g. Repeat part d.

h. Set the generator output voltage to 150 mV and the frequency to 100 MHz.

i. Repeat part d.

4. Check External Trigger Ranges

a. Set:

CH 1 VOLTS/DIV	0.5 V
A SEC/DIV	20 μs
X10 Magnifier	Off (knob in)
A TRIGGER SLOPE	OUT
A TRIGGER Mode	NORM

b. Set the generator to produce a 50 kHz, 6.4-division display.

c. CHECK—Display is triggered along the entire positive slope of the waveform as the A TRIGGER LEVEL control is rotated.

d. CHECK—Display is not triggered (no trace) at either extreme of rotation.

e. Set the A TRIGGER SLOPE button to IN.

f. CHECK—Display is triggered along the entire negative slope of the waveform as the A TRIGGER LEVEL control is rotated.

g. CHECK—Display is not triggered (no trace) at either extreme of rotation.

5. Check Single Sweep Operation

a. Adjust the A TRIGGER LEVEL control to obtain a stable display.

b. Set:

Channel 1 AC-GND-DC	GND
A SOURCE	INT

c. Press in the SGL SWP button. The READY LED should illuminate and remain on.

d. Set the Channel 1 AC-GND-DC switch to DC.

NOTE

The A INTENSITY control may require adjustment to observe the single-sweep trace.

e. CHECK—READY LED goes out and a single sweep occurs.

f. Press in the SGL SWP button several times.

g. CHECK—Single-sweep trace occurs, and the READY LED illuminates briefly every time the SGL SWP button is pressed in and released.

h. Disconnect the test equipment from the instrument.

6. Check Acquisition Window Trigger Point

a. Set:

A TRIGGER Mode	P-P AUTO
1K/4K	4K (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
WAVEFORM REFERENCE/ MENU SELECT	MENU SELECT (button out)

b. Use the Menu controls to select A TRIG POS.

c. CHECK—The A TRIG POS default number is 512.

d. Press in momentarily the PRETRIG/POST TRIG switch to activate the trigger point display on the crt. Return the PRETRIG/POST TRIG switch to POST TRIG (button out).

e. CHECK—The trigger point (T) appears near the 2nd vertical graticule line below the Menu.

f. Set the PRETRIG/POST TRIG switch to PRETRIG (button in).

g. CHECK—The A TRIG POS default number is 3584 and the trigger point (T) appears near the 9th vertical graticule line below the Menu.

h. Set the 1K/4K switch to 1K (button in).

i. CHECK—The A TRIG POS default number is 896 and the trigger point (T) appears near the 9th vertical graticule line below the Menu.

j. Set the PRETRIG/POST TRIG switch to POST TRIG (button out).

k. CHECK—The A TRIG POS default number is 128 and the trigger point (T) appears near the 2nd vertical graticule line below the Menu.

l. CHECK—The trigger point (T) can be moved between the 1st and the center vertical graticule line as the CURSORS control is rotated.

m. Set the PRETRIG/POST TRIG switch to PRETRIG (button in).

n. CHECK—The trigger point (T) can be moved between the 10th and the center vertical graticule line as the CURSORS control is rotated.

o. Set the 1K/4K switch to 4K (button out).

p. Repeat part n for PRETRIG mode and part l for POST TRIG mode.

EXTERNAL Z-AXIS, PROBE ADJUST, EXTERNAL CLOCK, AND X-Y PLOTTER

Equipment Required (see Table 4-1):

- Leveled Sine-Wave Generator (Item 2)
- Pulse Generator (Item 5)
- Digital Voltmeter (Item 7)
- Two 50 Ω BNC Cables (Item 8)
- BNC T-Connector (Item 11)
- 50 Ω BNC Termination (Item 12)
- BNC Male-to-Tip Plug (Item 17)
- 10X Probe (provided with instrument)

INITIAL CONTROL SETTINGS

VERTICAL

Channel 1 POSITION	Midrange
VERTICAL MODE	CH 1
X-Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	1 V
CH 1 VOLTS/DIV Variable	CAL detent
Channel 1 AC-GND-DC	DC

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
A SEC/DIV	20 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Check External Z-Axis Operation

a. Connect the leveled sine-wave generator output via a 50 Ω cable and a T-connector to the CH 1 OR X input connector. Then connect a 50 Ω cable and a 50 Ω termination from the T-connector to the EXT Z-AXIS INPUT connector on the rear panel.

b. Set the generator to produce a 5 V, 50 kHz signal.

c. CHECK—For noticeable intensity modulation. The positive part of the sine wave should be of lower intensity than the negative part.

d. Disconnect the test equipment from the instrument.

2. Check Probe Adjust Operation

a. Set:

CH 1 VOLTS/DIV	10 mV
A SEC/DIV	0.5 ms

b. Connect the 10X Probe to the CH 1 OR X input connector and insert the probe tip into the PROBE ADJUST jack on the instrument front panel. If necessary, adjust the probe compensation for a flat-topped square-wave display.

c. CHECK—Display amplitude is 4.75 to 5.25 divisions.

d. Disconnect the probe from the instrument.

3. Check External Clock

a. Set:

CH 1 VOLTS/DIV	1 V
A SEC/DIV	1 ms

b. Connect the Pulse Generator high-amplitude output via a 50 Ω cable and a 50 Ω termination to CH 1 OR X input connector.

c. Set the generator to produce a 1 kHz, 5-division display.

d. Disconnect the cable from the CH 1 OR X input connector and connect it to the BNC male-to-tip plug via BNC female to BNC female connector.

e. Insert the BNC male-to-tip plug signal lead and ground lead into pin 1 and pin 9 respectively of the X-Y Plotter connector.

f. Set the A SEC/DIV switch to 0.1 sec.

g. Connect the Calibration Generator high-amplitude output via a 50 Ω cable and a 50 Ω termination to CH 1 OR X input connector.

h. Set the generator to produce a 100 Hz, 5-division display.

i. Set:

A SEC/DIV	EXT CLK
STORE/NON STORE	STORE (button in)

j. CHECK—The 100 Hz signal is displayed on the screen and updated.

k. Set the SAVE/CONTINUE switch to SAVE (button in).

l. CHECK—The display is saved.

m. Disconnect the test equipment from the instrument.

4. Check X-Y Plotter

a. Connect the digital voltmeter low lead to either chassis ground or pin 9 (signal ground) of the X-Y Plotter connector. Connect the volts lead to pin 3 (X Output) of the X-Y Plotter connector.

b. Set the digital voltmeter to the 20 V scale.

c. Set the WAVEFORM REFERENCE/MENU SELECT switch to MENU SELECT (button out).

d. Use the Menu controls to select PLOT and then ON for GRATICULE.

NOTE

The next menu selection is only valid if the instrument contains one of the communication options.

e. Use the Menu controls to select PLOT and then XY for FORMAT.

f. Use the Menu controls to select PLOT START.

g. Press in momentarily the CURSORS button to activate the X-Y Plotter.

NOTE

Voltage reading of the X Output will be negative left of the center vertical graticule line and positive to the right of the center vertical graticule line. Voltage reading of the Y output will be negative below the center horizontal graticule line and positive above the center horizontal graticule line.

h. Record the voltage reading as the instrument plots the 1st and the 10th graticule line (as the intensity spot moves along the graticule line).

i. CHECK—The voltage difference between the 1st and 10th graticule line is between 4.5 V and 5.5 V.

j. Move the volts lead of the voltmeter from pin 3 (X Output) to pin 5 (Y Output) of the X-Y Plotter connector.

k. Press in momentarily the CURSORS button to activate the X-Y Plotter.

l. Record the voltage reading as the instrument plots the top and the bottom of the graticule lines (as the intensity spot moves along the graticule line).

m. CHECK—The voltage difference between the top and bottom graticule line is between 3.6 V and 4.4 V.

n. Disconnect the test equipment from the instrument.

ADJUSTMENT PROCEDURE

INTRODUCTION

PURPOSE

The "Adjustment Procedure" is a set of logically sequenced instructions intended to return the instrument to conformance with the Performance Requirement statements listed in Table 1-1. Adjustments contained in this procedure should only be performed after checks from the "Performance Check Procedure" (Section 4) have indicated a need for readjustment or after repairs have been made to the instrument.

STRUCTURE

This procedure is structured into subsections, each of which can be performed independently to permit adjustment of individual sections of the instrument. For example, if only the Vertical section fails to meet the Performance Requirements or has been repaired, it can be readjusted with little or no effect on other sections of the instrument.

The Power Supply section, however, affects all other sections of the instrument. Therefore, if repairs or readjustments have been made that change the absolute value of any of the supply voltages, the entire Adjustment Procedure should be performed.

At the beginning of each subsection is a list of all the front-panel control settings required to prepare the instrument for performing Step 1 in that subsection. Each succeeding step within a subsection should be performed in sequence and in its entirety to ensure that control settings will be correct for ensuing steps. All steps within a subsection should be completed.

TEST EQUIPMENT

Table 4-1 is a complete list of the test equipment required to accomplish both the "Performance Check Procedure" in Section 4 and the "Adjustment Procedure" in this section. To assure accurate measurements, it is important that test equipment used for making these checks meet or exceed the specifications described in Table 4-1. When considering use of equipment other than that recommended, utilize the "Minimum Specification" column to determine whether available test equipment will suffice.

Detailed operating instructions for test equipment are not given in this procedure. If more operating information is required, refer to the appropriate test-equipment instruction manual.

LIMITS AND TOLERANCES

The limits and tolerances stated in this procedure are instrument specifications only if they are listed in the "Performance Requirements" column of Table 1-1. Tolerances given are applicable only to the instrument undergoing adjustment and do not include test equipment error. Adjustment of the instrument must be accomplished at an ambient temperature between +20°C and +30°C, and the instrument must have had a warm-up period of at least 20 minutes.

ADJUSTMENTS AFFECTED BY REPAIRS

Repairs to a circuit may affect one or more adjustment settings of the instrument. Table 5-1 identifies the adjustment(s) affected due to repairs or replacement of components on a circuit board. Refer to Table 5-1 if a partial procedure is performed or if a circuit requires readjustment due to repairs to a circuit. To use this table, first find, in the leftmost column, the circuit that was repaired. Then move to the right, across that row, until you come to a darkened square, move up the column and check the accuracy of the adjustment found at the heading of that column. Readjust if necessary.

PREPARATION FOR ADJUSTMENT

The instrument cabinet must be removed to perform the Adjustment Procedure. See the "Cabinet" remove and replace instructions located in the "Maintenance" section of the manual. When making adjustments inside the instrument, the Storage circuit board has to be lifted up and

latched to allow access to the internal adjustments. See the "Storage Circuit Board in Servicing Position" procedure in the "Removal and Replacement Instructions" part of the "Maintenance" section.

All test equipment items listed in Table 4-1 are required to accomplish a complete Adjustment Procedure. At the beginning of each subsection there is an equipment-required list showing only the test equipment necessary for performing the steps in that subsection. In this list, the item number following each piece of equipment corresponds to the item number listed in Table 4-1.

Before performing this procedure, do not preset any internal adjustments and do not change the −8.6 V power-supply adjustment. Altering this adjustment may necessitate a complete readjustment of the instrument, whereas only a partial adjustment might otherwise be required. Only change an internal adjustment setting if a Performance Characteristic cannot be met with the original setting.

Before performing any procedure in this section, set the POWER switch to ON and allow a 20-minute warm-up period.

The most accurate display adjustments are made with a stable, well-focused, low-intensity display. Unless otherwise noted, adjust the INTENSITY, FOCUS, and TRIGGER LEVEL controls as needed to view the display.

Table 5-1

Adjustments Affected by Repairs

REPAIRS MADE	INTERNAL ADJUSTMENTS AFFECTED																												
	-8.6 V ADJ	GRID BIAS, ASTIG, & GEOM	STEP ATTN BAL	2/5 mV DC BAL	VAR BAL & INVERT BAL	MF/LF COMP & MF/LF GAIN BAL	CH 1, CH 2 GAIN, & 2mV GAIN	STORE Y GAIN & Y OFFSET	ACQ OFFSET	CH 1 & CH 2 GAIN	CH 1 & CH 2 ACQ POS OFFSET	10X ATTN & 100X ATTN	HF COMP & CH 2 HF COMP	2mV PEAK	CH 1 & CH 2 ACQ HF PEAK	A & B SWEEP GAIN	X10 GAIN	MAG	DELAY START, D-END, & READOUT	A & B HIGH SPEED TIMING	5 nS TIMING	RATIO ADJ	X & Y VECTOR/DOT ALIGN	STORE X GAIN & X OFFSET	CDT XY & CDT X	X-GAIN	TRIG OFFSET, SENS, & B SENS	P-P AUTO LEVEL
POWER SUPPLIES	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
VERTICAL ATTENUATORS			■	■	■	■	■		■	■	■	■	■	■	■													■	■
PREAMPS & CHANNEL SW				■	■	■	■		■	■	■		■	■	■													■	■
VERTICAL OUTPUT				■	■	■	■	■		■	■	■		■	■	■												■	■
TRIGGER CIRCUITS																										■			
A SWEEP GENERATOR																■	■	■	■	■	■	■			■			■	
B SWEEP GENERATOR																■	■		■	■	■	■						■	
HORIZONTAL AMPLILFIER																■	■	■	■	■	■	■			■				
DIGITAL TO ANALOG								■	■	■	■																		
STORE ACQUISITION								■		■	■				■									■					
VECTOR GENERATOR								■	■	■	■									■				■					
I/O CIRCUIT											■															■			
DIGITAL TIMEBASE																											■		
CRT		■						■	■	■	■					■									■		■		

INDEX TO ADJUSTMENT PROCEDURE STEPS

Power Supply and CRT Display — Page

1. Check/Adjust Power Supply DC Levels 5-4
2. Adjust CRT Grid Bias 5-4
3. Adjust Astigmatism 5-5
4. Adjust Trace Alignment 5-5
5. Adjust Geometry 5-5

Vertical

1. Adjust Step Attenuator Balance 5-6
2. Adjust 2/5 mV DC Balance 5-7
3. Adjust Channel 1 Variable Balance 5-7
4. Adjust Channel 2 Invert Balance 5-7
5. Adjust MF/LF Compensation and Gain Balance 5-7
6. Adjust Vertical Gain 5-8
7. Check Deflection Accuracy and Variable Range 5-8
8. Check Input Coupling 5-9
9. Check Position Range 5-9
10. Adjust/Check Acquisition Position Registration 5-9
11. Adjust Acquisition Gain 5-10
12. Check Store Deflection Accuracy 5-10
13. Adjust Store Y Offset and Gain 5-11
14. Adjust Acquisition Position Offset 5-11
15. Check Save Expansion and Compression 5-11
16. Adjust Attenuator Compensation 5-12
17. Check Alternate Operation 5-13
18. Check Chop Operation 5-13
19. Adjust High-Frequency Compensation and Channel 2 High-Frequency Compensation 5-13
20. Adjust 2 mV Peaking Compensation 5-14
21. Adjust Acquisition High-Frequency Peaking 5-14
22. Check Store Mode Cross Talk 5-15
23. Check Store Pulse Width Amplitude 5-15
24. Check Average Mode 5-16
25. Check Bandwidth Limit Operation 5-16
26. Check Bandwidth 5-16
27. Check Repetitive Store Mode 5-16
28. Check Single Sweep Sample Acquisition 5-17
29. Check Non Store and Store Channel Isolation 5-17
30. Check Common-Mode Rejection Ratio 5-18
31. Check Probe Encoding 5-18

Horizontal — Page

1. Adjust Horizontal Amplifier Gain 5-19
2. Adjust X10 Horizontal Amplifier Gain 5-20
3. Adjust Magnifier Registration 5-20
4. Check Sweep Length 5-20
5. Check Position Range 5-20
6. Check Variable Range 5-20
7. Adjust/Check 4K to 1K Display Compress 5-21
8. Adjust Delay Timing and Readout 5-21
9. Adjust High-Speed Timing 5-21
10. Adjust 5 ns Timing and Linearity 5-22
11. Check Timing Accuracy and Linearity 5-22
12. Check Delay Time Differential Accuracy 5-23
13. Check Delay Jitter 5-24
14. Adjust Vector Generator 5-24
15. Adjust Store X Offset and Gain 5-24
16. Adjust Clock Delay Timer 5-24
17. Check Store Differential and Cursor Time Difference Accuracy 5-24
18. Check Store Expansion Range 5-25
19. Check A/B Sweep Separation 5-25
20. Adjust X Gain 5-25
21. Check X-Y Store 5-26
22. Check X Bandwidth 5-26
23. Check A-Sweep Holdoff 5-26

Trigger

1. Adjust Channel 1 Trigger Offset 5-27
2. Adjust A and B Trigger Sensitivity 5-28
3. Adjust P-P Auto Level 5-28
4. Check Internal A and B Triggering 5-28
5. Check HF Reject A Triggering 5-29
6. Check External Triggering 5-30
7. Check External Trigger Ranges 5-30
8. Check Single Sweep Operation 5-30
9. Check Acquisition Window Trigger Point 5-31

External Z-Axis, Probe Adjust, External Clock, and X-Y Plotter

1. Check External Z-Axis Operation 5-32
2. Check Probe Adjust Operation 5-32
3. Check External Clock 5-33
4. Check X-Y Plotter 5-33

POWER SUPPLY AND CRT DISPLAY

Equipment Required (See Table 4-1):

Leveled Sine-Wave Generator (Item 2)	50 Ω BNC Cable (Item 8)
Time-Mark Generator (Item 3)	50 Ω BNC Termination (Item 12)
Digital Voltmeter (Item 7)	Screwdriver (Item 19)

See ADJUSTMENT LOCATIONS 1 *at the back of this manual for location of test points and adjustments.*

INITIAL CONTROL SETTINGS

Vertical

POSITION (both)	Midrange
VERTICAL MODE	CH 1
X-Y	On (button in)
CH 1 VOLTS/DIV Variable	CAL detent
Channel 1 AC-GND-DC	GND

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT
A EXT COUPLING	AC

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Check/Adjust Power Supply DC Levels (R938)

NOTE

Review the information at the beginning of the Adjustment Procedure before starting this step.

a. Connect the digital voltmeter low lead to chassis ground and connect the volts lead to the −8.6 V supply (W961).

b. CHECK—Voltmeter reading is −8.56 to −8.64 V. If the reading is within these limits, skip to part d.

c. ADJUST—The −8.6 V Adj potentiometer (R938) for a voltmeter reading of −8.6 V.

d. CHECK—Voltage levels of the remaining power supplies listed in Table 5-2 are within the specified limits.

e. Disconnect the test equipment from the instrument.

2. Adjust CRT Grid Bias (R851)

a. Connect a 50 Ω termination to the EXT Z AXIS INPUT connector located on the rear panel.

b. Adjust the front-panel FOCUS control to produce a well-defined dot.

c. Rotate the A INTENSITY control fully counter-clockwise.

Table 5-2

Power Supply Limits

Power Supply	Test Point	Reading (Volts)
−8.6 V	W961	−8.56 to −8.64
−5.0 V	W9020	−4.75 to −5.25
+5.0 V	W9068	+4.75 to +5.25
+8.6 V	W960	+8.43 to +8.77
+30 V	W956	+29.1 to +30.9
+100 V	W954	+97.0 to +103.0

d. ADJUST—Grid Bias (R851) for a visible dot. Then back off the Grid Bias potentiometer until the dot just disappears.

e. Disconnect the 50 Ω termination from the EXT Z AXIS INPUT connector.

3. Adjust Astigmatism (R874)

a. Set:

A INTENSITY	Visible display
X-Y	Off (button out)
Channel 1 AC-GND-DC	DC
A SEC/DIV	5 μs

b. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50 kHz, 4-division display.

d. ADJUST—Astig (R874) and the front-panel FOCUS control for the best defined waveform.

e. Disconnect the test equipment from the instrument.

4. Adjust Trace Alignment

a. Position the trace to the center horizontal graticule line.

b. ADJUST—The front-panel TRACE ROTATION control for optimum alignment of the trace with the center horizontal graticule line.

5. Adjust Geometry (R870)

a. Set:

CH 1 VOLTS/DIV	50 mV
A SEC/DIV	0.1 ms

b. Connect 50 μs time markers from the time-mark generator via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Adjust the Channel 1 POSITION control to position the baseline part of the display below the bottom horizontal graticule line.

d. Adjust the SEC/DIV Variable control for 5 markers per division.

e. ADJUST—Geom (R870) for minimum curvature of the time markers at the left and right edges of the graticule.

f. Set the Channel 1 AC-GND-DC switch to GND.

g. ADJUST—Geom (R870) for minimum curvature of the baseline trace when positioned at the top and bottom horizontal graticule lines using the Channel 1 POSITION control.

h. Set the Channel 1 AC-GND-DC switch to DC.

i. Repeat parts e through h for optimum compromise between the vertical and horizontal displays.

j. Disconnect the test equipment from the instrument.

VERTICAL

Equipment Required (See Table 4-1):

Calibration Generator (Item 1)	10X Attenuator (Item 14)
Leveled Sine-Wave Generator (Item 2)	BNC Male-to-Miniature-Probe Tip (Item 16)
50 Ω BNC Cable (Item 8)	Low-Capacitance Alignment Tool (Item 18)
Dual-Input Coupler (Item 9)	Screwdriver (Item 19)
50 Ω BNC Termination (Item 12)	10X Probe (Included with instrument)

See ADJUSTMENT LOCATIONS 1; ADJUSTMENT LOCATIONS 2; *and* ADJUSTMENT LOCATIONS 4 *at the back of this manual for test point and adjustment locations.*

INITIAL CONTROL SETTINGS

Vertical (Both Channels)

POSITION	Midrange
VERTICAL MODE	CH 1
X-Y	Off (button out)
BW LIMIT	On (button in)
VOLTS/DIV	10 mV
VOLTS/DIV Variable	CAL detent
INVERT	Off (button out)
AC-GND-DC	GND

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
A SEC/DIV	0.5 ms
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT
A EXT COUPLING	AC

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Adjust Step Attenuator Balance (R10 and R60)

a. Position the trace on the center horizontal graticule line using the Channel 1 POSITION control.

b. Set the CH 1 VOLTS/DIV switch to 5 mV.

c. ADJUST—Step Attn Bal (R10) to set the trace on the center horizontal graticule line.

d. Set the CH 1 VOLTS/DIV switch to 10 mV.

e. Repeat parts a through d until there is no trace shift when changing the CH 1 VOLTS/DIV switch from 50 mV to 5 mV.

f. Set the VERTICAL MODE switch to CH 2.

g. Repeats parts a through e for Channel 2, adjusting Step Attn Bal (R60) in part c.

2. Adjust 2/5 mV DC Balance (R83 and R33)

a. Set the CH 2 VOLTS/DIV switch to 5 mV.

b. Position the trace on the center horizontal graticule line using the Channel 2 POSITION control.

c. Set the CH 2 VOLTS/DIV switch to 2 mV.

d. ADJUST—2/5 mV Dc Bal (R83) to set the trace on the center horizontal graticule line.

e. Repeat parts a through d until there is no trace shift when changing the CH 2 VOLTS/DIV switch from 5 mV to 2 mV.

f. Set the VERTICAL MODE switch to CH 1.

g. Repeat parts a through e for Channel 1, adjusting 2/5 mV Dc Bal (R33) in part d.

3. Adjust Channel 1 Variable Balance (R25)

a. Set both VOLTS/DIV switches to 2 mV.

b. Rotate the CH 1 VOLTS/DIV Variable control fully counterclockwise.

c. Position the trace on the center horizontal graticule line using the Channel 1 POSITION control.

d. Rotate the CH 1 VOLTS/DIV Variable control clockwise to the CAL detent.

e. ADJUST—Var Bal (R25) to set the trace to the center horizontal graticule line.

f. Repeat parts b through e until there is no trace shift between the fully clockwise and the fully counterclockwise positions of the CH 1 VOLTS/DIV Variable control.

g. Return the CH 1 VOLTS/DIV Variable control to the CAL detent.

4. Adjust Channel 2 Invert Balance (R75)

a. Set the VERTICAL MODE switch to CH 2.

b. Position the trace on the center horizontal graticule line using the Channel 2 POSITION control.

c. Set the INVERT button to On (button in).

d. ADJUST—Invert Bal (R75) to set the trace to the center horizontal graticule line.

e. Set the INVERT button to Off (button out).

f. Repeat parts b through e until there is no trace shift when switching the INVERT button between the On and Off positions.

5. Adjust MF/LF Compensation and Gain Balance (C53, R97, C3, and R47)

a. Set:

VERTICAL MODE	CH 2
VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	DC
A SEC/DIV	20 μs

b. Connect the high-amplitude square wave output via a 50 Ω cable, a 10X attenuator, and a 50 Ω termination to the CH 2 OR Y input connector.

c. Set the generator to produce a 10 kHz, 5-division display.

d. Set the top of the display on the center horizontal graticule line using the Channel 2 POSITION control.

e. ADJUST—MF/LF Comp (C53) and MF/LF Gain Bal (R97) for the best front corner and flat top.

f. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the VERTICAL MODE switch to CH 1.

g. Set the top of the display on the center horizontal graticule line using the Channel 1 POSITION control.

h. ADJUST—MF/LF Comp (C3) and MF/LF Gain Bal (R47) for the best front corner and flat top.

i. Disconnect the test equipment from the instrument.

6. Adjust Vertical Gain (R145, R195, R76, and R26)

a. Connect a 50 mV standard-amplitude signal from the Calibration Generator via a 50 Ω cable to the CH 1 OR X input connector.

b. Set the A SEC/DIV switch to 0.2 ms.

c. Center the display within the graticule using the Channel 1 POSITION control.

d. ADJUST—Ch 1 Gain (R145) for an exact 5-division display.

e. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the VERTICAL MODE switch to CH 2.

f. Center the display within the graticule using the Channel 2 POSITION control.

g. ADJUST—Ch 2 Gain (R195) for an exact 5-division display.

h. Change the generator output to 10 mV and set both VOLTS/DIV switches to 2 mV.

i. Repeat parts d and g until the gain of the two channels is identical.

j. ADJUST—2 mV Gain (R76) for an exact 5-division display.

k. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the VERTICAL MODE switch to CH 1.

l. ADJUST—2 mV Gain (R26) for an exact 5-division display.

m. Set both AC-GND-DC switches to GND.

n. CHECK—That no trace shift occurs when switching between the 5 mV and 2 mV positions of the CH 1 VOLTS/DIV switch. If trace shift is observed, repeat Step 2 of this procedure.

o. Set the VERTICAL MODE switch to CH 2.

p. CHECK—That no trace shift occurs when switching between the 5 mV and 2 mV positions of the CH 2 VOLTS/DIV switch. If trace shift is observed, repeat Step 2 of this procedure.

7. Check Deflection Accuracy and Variable Range

a. Set:

VERTICAL MODE	CH 1
AC-GND-DC (both)	DC

b. CHECK—Deflection accuracy is within the limits given in Table 5-3 for each CH 1 VOLTS/DIV switch setting and corresponding standard-amplitude signal. When at the 20 mV VOLTS/DIV switch setting, rotate the CH 1 VOLTS/DIV Variable control fully counterclockwise and CHECK that the display decreases to 2 divisions or less. Then return the CH 1 VOLTS/DIV Variable control to the CAL detent and continue with the 50 mV check.

Table 5-3

Deflection Accuracy Limits

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Accuracy Limits (Divisions)
2 mV	10 mV	4.90 to 5.10
5 mV	20 mV	3.92 to 4.08
10 mV	50 mV	4.90 to 5.10
20 mV	0.1 V	4.90 to 5.10
50 mV	0.2 V	3.92 to 4.08
0.1 V	0.5 V	4.90 to 5.10
0.2 V	1 V	4.90 to 5.10
0.5 V	2 V	3.92 to 4.08
1 V	5 V	4.90 to 5.10
2 V	10 V	4.90 to 5.10
5 V	20 V	3.92 to 4.08

c. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the VERTICAL MODE switch to CH 2.

d. Repeat part b using the Channel 2 controls.

8. Check Input Coupling

a. Set both VOLTS/DIV switches to 10 mV.

b. Set the calibration generator to produce a 20 mV signal.

c. Set the bottom of the signal on the center horizontal graticule line using the Channel 2 POSITION control.

d. Set the Channel 2 AC-GND-DC switch to AC.

e. CHECK—Display is centered about the center horizontal graticule line.

f. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the VERTICAL MODE switch to CH 1.

g. Repeat parts c through e using the Channel 1 controls.

9. Check Position Range

a. Set both VOLTS/DIV switches to 50 mV.

b. Set the calibration generator to produce a 0.5 V signal.

c. Adjust the CH 1 VOLTS/DIV Variable control to produce a 4.4-division display. Set the CH 1 VOLTS/DIV switch to 10 mV.

d. CHECK—The bottom and top of the trace may be positioned above and below the center horizontal graticule line by rotating the Channel 1 POSITION control fully clockwise and counterclockwise respectively.

e. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the VERTICAL MODE switch to CH 2.

f. Repeat parts c and d using the Channel 2 controls.

10. Adjust/Check Acquisition Vertical Position Registration (R2138) and Horizontal Position Registration (R6430 SN-B022102 & Above)

a. Set:

VERTICAL MODE	BOTH and ALT
VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	GND
A SEC/DIV	10 μs

b. Position both traces exactly on the center horizontal graticule line using the Channel 1 and Channel 2 POSITION controls.

c. Position the sweep start of the display to the left most vertical graticule line using the Horizontal POSITION control.

d. Set STORE/NON STORE switch to STORE (button in).

e. ADJUST—Vertical Acq Offset (R2138) to position the traces exactly on the center horizontal graticule line.

NOTE

Instruments with serial numbers below B022102; skip to part g and continue with this step.

f. ADJUST—Horizontal Acq Offset (R6430) to position the sweep start of the display to the left most vertical graticule line.

g. Set:

VERTICAL MODE	CH 2
STORE/NON STORE	NON STORE (button out)

h. Set STORE/NON STORE switch to STORE (button in).

i. CHECK—Trace remains within 0.5 division of the center horizontal graticule line and the sweep start remains within 0.5 division of the left vertical graticule line.

j. Set:

VERTICAL MODE	CH 1
STORE/NON STORE	NON STORE (button out)

k. Repeat parts h and i for Channel 1 trace.

l. Position the trace 0.5 division below the top horizontal graticule line using the Channel 1 POSITION control.

m. Set SAVE/CONTINUE switch to SAVE (button in).

n. CHECK—Trace shift of 0.5 division or less.

o. Set SAVE/CONTINUE switch to CONTINUE (button out).

p. Position the trace 0.5 division above the bottom horizontal graticule line using the Channel 1 POSITION control.

q. Set SAVE/CONTINUE switch to CONTINUE (button out).

r. CHECK—Trace shift of 0.5 division or less.

s. Set the VERTICAL MODE switch to CH 2.

t. Repeat parts l through r for Channel 2 trace.

11. Adjust Acquisition Gain (R2108 and R2118)

a. Set:

AC-GND-DC (both)	DC
STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)
1K/4K	1K (button in)

b. Set the calibration generator output to 50 mV.

c. Center the display within the graticule using the Channel 2 POSITION control.

d. ADJUST—Ch 2 Acq Gain (R2108) for an exact 5-division display.

e. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the VERTICAL MODE switch to CH 1.

f. Center the display within the graticule using the Channel 2 POSITION control.

g. ADJUST—Ch 1 Acq Gain (R2118) for an exact 5-division display.

12. Check Store Deflection Accuracy

a. Set:

CH 1 VOLTS/DIV	2 mV
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)

b. Set the calibration generator output to 10 mV.

c. Use the CURSORS control and SELECT C1/C2 switch to set one cursor at the bottom and the other cursor at the top of the square wave.

d. CHECK—Deflection accuracy is within the limits given in Table 5-4 for each CH 1 VOLTS/DIV switch setting and corresponding standard-amplitude signal.

e. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the VERTICAL MODE switch to CH 2.

f. Repeat parts c and d for each CH 2 VOLTS/DIV switch setting.

Table 5-4

Store Deflection Accuracy

VOLTS/ DIV Switch Setting	Standard Amplitude Signal	Divisions of Deflection	Voltage Readout Limits
2 mV	10 mV	4.90 to 5.10	9.80 to 10.20 mV
5 mV	20 mV	3.92 to 4.08	19.6 to 20.4 mV
10 mV	50 mV	4.90 to 5.10	49.0 to 51.0 mV
20 mV	0.1 V	4.90 to 5.10	98.0 to 102.0 mV
50 mV	0.2 V	3.92 to 4.08	198.0 to 204.0 mV
0.1 V	0.5 V	4.90 to 5.10	0.490 to 0.510 V
0.2 V	1 V	4.90 to 5.10	0.980 to 1.020 V
0.5 V	2 V	3.92 to 4.08	1.960 to 2.040 V
1 V	5 V	4.90 to 5.10	4.90 to 5.10 V
2 V	10 V	4.90 to 5.10	9.80 to 10.20 V
5 V	20 V	3.92 to 4.08	19.60 to 20.40 V

13. Adjust Store Y Offset and Gain (R9224 and R9222)

a. Set the WAVEFORM REFERENCE/MENU SELECT switch to MENU SELECT (button out).

b. Use the Menu controls to display the rectangle test waveforms on the screen by selecting ADVANCE FUNCTIONS, DIAGNOSTICS, CAL AIDS, and BOX in that order.

c. ADJUST—Store Y Offset (R9224) so that the bottom trace of the outside box is exactly aligned with the bottom horizontal graticule line.

d. ADJUST—Store Y Gain (R9222) so that the height of the inside box is exactly 6 vertical divisions.

e. INTERACTION—Repeat parts c and d until the height of the inside box is exactly 6 vertical divisions and the bottom trace of the outside box is aligned with the bottom horizontal graticule line.

14. Adjust Acquisition Position Offset (R7325 and R7335)

a. Set:

VERTICAL MODE	BOTH and ALT
AC-GND-DC (both)	GND

b. Use the Menu controls to call up Calibrate Vertical Position procedure on the screen by selecting CAL__V__ POS in the Menu. The display will consist of three short and two baseline traces on the screen.

c. Vertically position the two baseline traces exactly on the short center stationary trace.

d. Press in momentary the SELECT C1/C2 switch to advance to the next level of the test routine. The two short movable traces should be vertically centered near the two overlapping baseline traces.

e. Vertically position Channel 1 baseline trace to the top and bottom of the screen using the Channel 1 POSITION control. Note the separation of the short trace from the baseline trace at the top and bottom of the screen.

f. ADJUST—Ch 1 Acq Pos Offset (R7325) for minimum separation of the Channel 1 baseline and the short trace at the top and bottom of the screen.

g. Repeat part e for Channel 2 baseline trace.

h. ADJUST—Ch 2 Acq Pos Offset (R7335) for minimum separation of the Channel 2 baseline and the short trace at the top and bottom of the screen.

15. Check Save Expansion and Compression

a. Set:

VERTICAL MODE	CH 2
VOLTS/DIV (both)	0.1 V
AC-GND-DC (both)	DC
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

b. Set the calibration generator to produce a 50 mV signal.

c. Set the SAVE/CONTINUE switch to SAVE (button in).

d. Set the CH 2 VOLTS/DIV switch to 10 mV and reposition the dispiay.

e. CHECK—The display is expanded to 5 divisions in amplitude.

f. Set:

CH 2 VOLTS/DIV	0.1 V
SAVE/CONTINUE	CONTINUE (button out)

g. Set the calibration generator to produce a 0.5 V signal.

h. Set the SAVE/CONTINUE switch to SAVE (button in).

i. Set the CH 2 VOLTS/DIV switch to 1 V.

j. CHECK—The display is compressed to 0.5 division in amplitude.

k. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

i. Set:

VERTICAL MODE	CH 1
SAVE/CONTINUE	CONTINUE (button out)

m. Repeat parts c through j.

n. Disconnect the test equipment from the instrument.

16. Adjust Attenuator Compensation (C12, C11, C5, C4, C62, C61, C55, C54)

a. Set:

VOLTS/DIV (both)	0.1 V
STORE/NON STORE	NON STORE (button out)

b. Connect the high-amplitude square wave output via a 50 Ω termination, a probe-tip-to-BNC adapter, and the 10X probe to the CH 1 OR X input connector.

c. Set the generator to produce a 1 kHz, 5-division display and compensate the probe using the probe compensation adjustment (see the probe instruction manual).

d. Set the CH 1 VOLTS/DIV switch to 0.1 V.

e. Replace the probe and probe-tip-to-BNC adapter with a 50 Ω cable.

f. Set the generator to produce a 5-division display.

NOTE

Use Table 5-5 to identify the correct capacitor for each channel adjustment.

g. ADJUST—The 10X Attn (C12) for best front corner.

Table 5-5

Attenuator Compensation Adjustments

Adjustment	Channel 1	Channel 2
10X Attn (LF Comp)	C12	C62
10X Attn (Input C)	C11	C61
100X Attn (LF Comp)	C5	C55
100X Attn (Input C)	C4	C54

h. Replace the 50 Ω cable and 50 Ω termination with the probe and probe-tip-to-BNC adapter.

i. Set the generator to produce a 5-division display.

j. ADJUST—The 10X Attn (C11) for best flat top.

k. Repeat parts e through j until no further improvement is noted.

l. Set the CH 1 VOLTS/DIV switch to 1 V.

m. Replace the probe and probe-tip-to-BNC adapter with the 50 Ω cable and 50 Ω termination.

n. Set the generator to produce a 5-division display.

o. ADJUST—The 100X Attn (C5) for best front corner.

p. Replace the 50 Ω cable and 50 Ω termination with the probe and probe-tip-to-BNC adapter.

q. Set the generator to produce a 5-division display.

r. ADJUST—The 100X Attn (C4) for best flat top.

s. Repeat parts m through r until no further improvement is noted.

t. Set the VERTICAL MODE switch to CH 2.

u. Repeat parts b through s for Channel 2 attenuators.

v. Disconnect the test equipment from the instrument.

17. Check Alternate Operation

a. Set:

VERTICAL MODE	BOTH and ALT
AC-GND-DC (both)	GND
A and B SEC/DIV	50 ms
A&B INT	CH 1

b. Position the Channel 1 and Channel 2 traces about 2 divisions apart using the Channel 1 and Channel 2 POSITION controls.

c. CHECK—Sweeps alternate for all the A SEC/DIV switch settings.

NOTE

At sweep speeds of 2 ms per division or faster, the trace alternations occur too rapidly to be observed.

18. Check Chop Operation

a. Set:

VERTICAL MODE	BOTH and CHOP
A SEC/DIV	1 μs
A&B INT	VERT MODE
A SOURCE	EXT

b. Connect the 10X probe to the EXT INPUT connector.

c. Connect the 10X probe tip to TP537.

d. CHECK—Period of one complete square-wave cycle is between 1.6 and 2.6 horizontal divisions.

e. Disconnect the 10X probe from TP537 and the EXT INPUT connector.

f. CHECK—Two traces are visible for all A SEC/DIV switch settings.

19. Adjust High-Frequency Compensation (C237, R240 and R241) and Channel 2 High-Frequency Compensation (C180)

a. Set:

VERTICAL MODE	CH 1
BW LIMIT	Off (button out)
VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	DC
A SEC/DIV	0.05 μs
A SOURCE	INT

b. Connect the positive-going fast-rise square wave output via a 50 Ω cable, a 10X attenuator, and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 1 MHz, 5-division display.

d. Set the top of the display to the center horizontal graticule line using the Channel 1 POSITION control.

e. ADJUST—HF Comp (C237) for 2% overshoot (0.1 division) on the displayed signal.

f. ADJUST—HF Comp (R240 and R241) for best flat top on the front corner.

g. Repeat parts e and f until no further improvement is noted.

h. Set the CH 1 VOLTS/DIV switch to 5 mV.

i. Set the generator to produce a 5-division display.

j. CHECK—Display aberrations are within 4% (0.2 division or less).

k. Repeat part j for each of the following CH 1 VOLTS/DIV switch settings: 5 mV through 0.5 V. Adjust the generator output and add or remove the 10X attenuator as necessary to maintain a 5-division display at each VOLTS/DIV switch setting.

l. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the VERTICAL MODE switch to CH 2.

m. Set the generator to produce a 5-division display.

n. Set the top of the display to the center horizontal graticule line using the Channel 2 POSITION control.

o. ADJUST—Ch 2 HF Comp (C180) for 2% overshoot (0.1 division) on the displayed signal.

p. Set the CH 2 VOLTS/DIV switch to 5 mV.

q. Repeat parts i through k for Channel 2.

20. Adjust 2-mV Peaking Compensation (C76 and C26)

a. Set both VOLTS/DIV switches to 2 mV.

b. Set the generator to produce a 5-division display.

c. Set the top of the display to the center horizontal graticule line using the Channel 2 POSITION control.

d. ADJUST—2mV Peak (C76) for 2% overshoot of the displayed signal.

e. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector. Set the VERTICAL MODE switch to CH 1.

f. ADJUST—2mV Peak (C26) for 2% overshoot of the displayed signal.

21. Adjust Acquisition High Frequency Peaking (C2103, R2149, and C2113)

a. Set:

VOLTS/DIV (both)	10 mV
STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)

b. Set the WAVEFORM REFERENCE/MENU SELECT switch to MENU SELECT (button out).

c. Use the Menu controls to call up SELECT MODE Table on the screen and select AVERAGE with the SELECT C1/C2 button. Reset the WAVEFORM REFERENCE/MENU SELECT switch to WAVEFORM REFERENCE (button out).

d. Set the generator to produce a 5-division display.

e. Set the top of the display to the center horizontal graticule line using the Channel 1 POSITION control.

f. ADJUST—Ch 1 Acq HF Peak (C2103) and Acq HF Peak (R2149) for best front corner.

g. Set the SAVE/CONTINUE switch to SAVE (button in).

h. CHECK—Display aberrations are within 4% (0.2 division or less).

i. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the VERTICAL MODE switch to CH 2.

j. Set the SAVE/CONTINUE switch to CONTINUE (button out).

k. Repeat part e using Channel 2 POSITION control.

l. ADJUST—Ch 2 Acq HF Peak (C2113) for best front corner.

m. Repeat parts g and h for Channel 2.

n. INTERACTION—It may be necessary to compromise the Ch 1 Acq HF Peak (C2103) and Acq HF Peak (R2149) adjustments in part f and the Ch 2 Acq HF peak (C2113) adjustment in part l, to obtain the best high-frequency match between Channel 1 and Channel 2.

o. Disconnect the test equipment from the instrument.

22. Check Store Mode Cross Talk

a. Set:

VERTICAL MODE	BOTH and CHOP
Channel 1 AC-GND-DC	GND
Channel 2 AC-GND-DC	AC
VOLTS/DIV (both)	0.1 V
A SEC/DIV	10 μs
STORE/NON STORE	STORE (button in)

b. Connect the Pulse Generator pulse-period output via a 50 Ω cable and a 50 Ω termination to CH 2 OR Y input connector.

c. Set the generator to produce a 100 kHz, 5-division display.

d. Use the Channel 2 POSITION control to center the display.

e. Set CH 2 VOLTS/DIV switch to 50 mV for a 10-division display.

f. CHECK—Display amplitude on Channel 1 is less than 1% (0.1 division).

g. Set the A SEC/DIV switch to 10 ms.

h. CHECK—Display amplitude on Channel 1 is less than 1% (0.1 division).

i. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

j. Set:

CH 2 VOLTS/DIV	0.1 V
Channel 1 AC-GND-DC	AC
Channel 2 AC-GND-DC	GND

k. Use the Channel 1 POSITION control to center the display.

l. Set the CH 1 VOLTS/DIV switch to 50 mV for a 10-division display.

m. Repeat parts f through h for Channel 2.

23. Check Store Pulse Width Amplitude

a. Set:

AC-GND-DC (both)	DC
VERTICAL MODE	CH 2
SEC/DIV	1 ms
STORE/NON STORE	NON STORE (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	1K (button in)

b. Set the generator to produce a 1 ms period, 100 ns duration, 5-division display.

c. Set the STORE/NON STORE switch to STORE (button in).

d. CHECK—The amplitude of the display is 2.5 divisions or greater.

e. Set the A SEC/DIV switch to 0.1 sec.

f. CHECK—The amplitude of the display is 2.5 divisions or greater.

g. Set ROLL/SCAN switch to ROLL (button in).

h. CHECK—The amplitude of the display is 2.5 divisions or greater.

i. Set:

VERTICAL MODE	BOTH and CHOP
A SEC/DIV	1 ms
STORE/NON STORE	NON STORE (button out)
ROLL/SCAN	SCAN (button out)

j. Set the generator to produce a 0.1 s period, 2 ms duration, 5-division display.

k. Repeat parts c through h.

l. Set:

A SEC/DIV	1 ms
STORE/NON STORE	NON STORE (button out)
ROLL/SCAN	SCAN (button out)

m. Set the generator to produce a 1 ms period, 20 μs duration, 5-division display.

n. Repeat parts c and d.

o. Disconnect the test equipment from the instrument.

24. Check Average Mode

a. Set the WAVEFORM REFERENCE/MENU SELECT switch to MENU SELECT (button out).

b. Use the Menu controls to select SWP LIMIT.

c. CHECK—The SWP LIMIT is adjustable from 1 to 2047 or NO LIMIT by rotating the CURSORS control.

NOTE

Install the instrument cabinet for the remaining vertical checks and allow a 20-minute warm-up period before continuing with the Adjustment Procedure. See the "Cabinet" remove and replace instructions located in the "Maintenance" section of the manual.

25. Check Bandwidth Limit Operation

a. Set:

Vertical POSITION (both)	Midrange
VERTICAL MODE	CH 1
BW LIMIT	On (button in)
VOLTS/DIV Variable (both)	CAL detent
AC-GND-DC (both)	DC
A SEC/DIV	20 μs
STORE/NON STORE	NON STORE (button out)

b. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50 kHz, 6-division display.

d. Increase the generator output frequency until the display amplitude decreases to 4.2 divisions.

e. CHECK—Generator output frequency is between 18 MHz and 22 MHz.

26. Check Bandwidth

a. Set:

BW LIMIT	Off (button out)
VOLTS/DIV (both)	2 mV

b. Set the generator to produce a 50 kHz, 6-division display.

c. CHECK—Display amplitude is 4.2 divisions or greater as the generator output frequency is increased up to the value shown in Table 5-6 for the corresponding VOLTS/DIV switch setting.

Table 5-6

Settings for Bandwidth Checks

VOLTS/DIV Switch Setting	Generator Output Frequency
2 mV	80 MHz
5 mV to 5 V	100 MHz

d. Repeat parts b and c for all CH 1 VOLTS/DIV switch settings, up to the output-voltage upper limit of the sine-wave generator being used.

e. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Set the VERTICAL MODE switch to CH 2.

f. Repeat parts b and c for all CH 2 VOLTS/DIV switch settings, up to the output-voltage upper limit of the sine-wave generator being used.

27. Check Repetitive Store Mode and Bandwidth

a. Set:

CH 2 VOLTS/DIV	10 mV
A SEC/DIV	0.2 ms

b. Set the generator to produce a 50 kHz, 6-division display.

c. Set:

A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

d. Set the generator to produce a 100 MHz display.

e. Set:

STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)

NOTE

Allow the points to accumulate for a few seconds before saving the display.

f. CHECK—The 100 MHz display will accumulate and store.

g. CHECK—The display amplitude is 4.2 divisions or greater.

h. Set:

VERTICAL MODE	BOTH and ALT
SAVE/CONTINUE	CONTINUE (button out)

i. Repeat parts f and g.

28. Check Single Sweep Sample Acquisition

a. Set:

VERTICAL MODE	CH 2
A SEC/DIV	5 μs
X10 Magnifier	Off (knob in)
A TRIGGER Mode	NORM
A&B INT	CH 2
SAVE/CONTINUE	CONTINUE (button out)
1K/4K	1K (button in)

b. Set the generator to produce a 50 kHz, 6-division display.

c. Press in the A TRIGGER Mode SGL SWP button.

d. Set the generator output to 2 MHz.

e. Press in the A TRIGGER Mode SGL SWP button.

f. CHECK—The minimum peak-to-peak envelope amplitude is greater than 5.6 divisions.

29. Check Non Store and Store Channel Isolation

a. Set:

VOLTS/DIV (both)	0.1 V
VOLTS/DIV Variable (both)	CAL detent
INVERT	Off (button out)
Channel 1 AC-GND-DC	GND
A SEC/DIV	0.1 μs
A TRIGGER Mode	P-P AUTO
A&B INT	VERT MODE
STORE/NON STORE	NON STORE (button out)

b. Set the generator to produce a 50 MHz, 5-division display.

c. Set the VERTICAL MODE switch to CH 1.

d. CHECK—Display amplitude is 0.05 division or less.

e. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

f. Set:

VERTICAL MODE	CH 2
Channel 1 AC-GND-DC	DC
Channel 2 AC-GND-DC	GND

g. CHECK—Display amplitude is 0.05 division or less.

h. Set:

CH 1 VOLTS/DIV	50 mV
STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)

i. CHECK—Display amplitude is 0.1 division or less.

j. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

k. Set:

VERTICAL MODE	CH 1
CH 1 VOLTS/DIV	0.1 V
CH 2 VOLTS/DIV	50 mV
Channel 1 AC-GND-DC	GND
Channel 2 AC-GND-DC	DC

l. CHECK—Display amplitude is 0.1 division or less.

m. Disconnect the test equipment from the instrument.

30. Check Common-Mode Rejection Ratio

a. Set:

VOLTS/DIV (both)	10 mV
INVERT	On (button in)
AC-GND-DC (both)	DC
STORE/NON STORE	NON STORE (button out)

b. Connect the leveled sine-wave generator output via a 50 Ω cable, a 50 Ω termination, and a dual-input coupler to the CH 1 OR X and CH 2 OR Y input connectors.

c. Set the generator to produce a 50 MHz, 6-division display.

d. Vertically center the display using the Channel 1 POSITION control. Then set the VERTICAL MODE switch to CH 2 and vertically center the display using the Channel 2 POSITION control.

e. Set the VERTICAL MODE switches to BOTH and ADD.

f. CHECK—Display amplitude is 0.6 division or less.

g. If the check in part f meets the requirement, skip to part p. If it does not, continue with part h.

h. Set the VERTICAL MODE switch to CH 1.

i. Set the generator to produce a 50 kHz, 6-division display.

j. Set the VERTICAL MODE switch to BOTH.

k. Adjust the CH 1 or CH 2 VOLTS/DIV Variable control for minimum display amplitude.

l. Set the VERTICAL MODE switch to CH 1.

m. Set the generator to produce a 50 MHz, 6-division display.

n. Set the VERTICAL MODE switch to BOTH.

o. CHECK—Display amplitude is 0.6 division or less.

p. Disconnect the test equipment from the instrument.

31. Check Probe Encoding

a. Set:

VOLTS/DIV (both)	0.1 V
VERTICAL MODE	CH 1

b. Read the 0.1 V on the Channel 1 VOLTS/DIV portion of the crt readout.

c. Connect the standard accessory 10X probe to the CH 1 OR X connector.

d. CHECK—The Channel 1 VOLTS/DIV portion of the crt readout changes from 0.1 V to 1 V.

e. Set VERTICAL MODE to CH 2.

f. Move the 10X probe from the CH 1 OR X input connector to the CH 2 OR Y input connector.

g. CHECK—The Channel 2 VOLTS/DIV portion of the crt readout changes from 100 mV to 1 V.

h. Disconnect the 10X probe from the instrument.

NOTE

To continue with the Adjustment Procedure, remove the instrument cabinet and allow a 20-minute time period to elapse before continuing with the Adjustment Procedure. See the "Cabinet" removal instructions located in the "Maintenance" section of the manual.

HORIZONTAL

Equipment Required (See Table 4-1):

Calibration Generator (Item 1)	50 Ω Cable (Item 8)
Leveled Sine-Wave Generator (Item 2)	50 Ω BNC Termination (Item 12)
Time-Mark Generator (Item 3)	Low-Capacitance Alignment Tool (Item 18)
Test Oscilloscope (Item 6)	Screwdriver (Item 19)

See ADJUSTMENT LOCATIONS 1, ADJUSTMENT LOCATIONS 3, *and* ADJUSTMENT LOCATIONS 4 *at the back of this manual for test point and adjustment locations.*

INITIAL CONTROL SETTINGS

Vertical

POSITION (both)	Midrange
VERTICAL MODE	CH 1
X-Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	0.5 V
CH 1 VOLTS/DIV Variable	CAL detent
Channel 1 AC-GND-DC	DC

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
A and B SEC/DIV	0.1 ms
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)
B DELAY TIME POSITION	Fully counterclockwise

B TRIGGER

SLOPE	OUT
LEVEL	Fully clockwise

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Adjust Horizontal Amplifier Gain (R740 and R730)

a. Connect 0.1 ms time markers from the time-mark generator via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

b. Use the Horizontal POSITION control to align the 1st time marker with the 1st vertical graticule line.

c. ADJUST—A Sweep Gain (R740) for 1 time marker per division over the center 8 divisions.

NOTE

When making timing measurements, use as a reference the tips of the time markers positioned at the center horizontal graticule line.

d. Set the HORIZONTAL MODE switch to B.

e. ADJUST—B Sweep Gain (R730) for 1 time marker per division.

2. Adjust X10 Horizontal Amplifier Gain (R754)

a. Set:

HORIZONTAL MODE	A
X10 Magnifier	On (knob out)

b. Select 10 μs time markers from the time-mark generator.

c. Align the nearest time marker to the 1st vertical graticule line with the 1st graticule line.

d. ADJUST—X10 Gain (R754) for 1 time marker per division.

3. Adjust Magnifier Registration (R749)

a. Set the A SEC/DIV switch to 0.2 ms.

b. Select 1 ms time markers from the time-mark generator.

c. Position the middle time marker to the center vertical graticule line using the Horizontal POSITION control.

d. Set the X10 Magnifier to Off (knob in).

e. ADJUST—Mag (R749) to position the middle time marker to the center vertical graticule line.

f. Set the X10 Magnifier to On (knob out) and CHECK for no horizontal shift in the time marker.

g. Repeat parts c through f until no further improvement is noted.

4. Check Sweep Length

a. Set:

Channel 1 AC-GND-DC	GND
X10 Magnifier	Off (knob in)

b. Position the start of the sweep at the 1st vertical graticule line using the Horizontal POSITION control.

c. CHECK—End of the sweep is to the right of the 11th vertical graticule line.

5. Check Position Range

a. Set:

Channel 1 AC-GND-DC	DC
A SEC/DIV	10 μs

b. Select 10 μs time markers from the time-mark generator.

c. CHECK—Start of the sweep can be positioned to the right of the center vertical graticule line by rotating the Horizontal POSITION control fully clockwise.

d. CHECK—The 11th time marker can be positioned to the left of the center vertical graticule line by rotating the Horizontal POSITION control fully counterclockwise.

e. Select 50 μs time markers from the time-mark generator.

f. Align the 3rd time marker with the center vertical graticule line using the Horizontal POSITION control.

g. Set the X10 Magnifier to On (knob out).

h. CHECK—Magnified time marker can be positioned to the left of the center vertical graticule line by rotating the Horizontal POSITION control fully counterclockwise.

i. CHECK—Start of the sweep can be positioned to the right of the center vertical graticule line by rotating the Horizontal POSITION control fully clockwise.

6. Check Variable Range

a. Set:

Horizontal POSITION	Midrange
A SEC/DIV	0.2 ms
SEC/DIV Variable	Fully counterclockwise
X10 Magnifier	Off (knob in)

b. Select 0.5 ms time markers from the time-mark generator.

c. CHECK—Time markers are 1 division or less apart.

7. Adjust/Check 4K to 1K Display Compress (R7507)

a. Set:

A SEC/DIV	50 μs
STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)
1K/4K	4K (button out)

b. Set Store Reset plug (P9104) to reset position.

c. Select 0.2 ms time markers from the time-mark generator.

d. ADJUST—Ratio Adj (R7507) for 1 time marker per division over the center 8 divisions.

e. Set the Store Reset plug (P9104) to normal position.

f. Select 0.1 ms time markers from the time-mark generator and check that the time markers are 2 divisions apart.

g. Rotate the SEC/DIV Variable control out of detent.

h. CHECK—For 2 time markers per division over the center 8 divisions.

8. Adjust Delay Timing and Readout (R646, R652, and R6119)

a. Set:

HORIZONTAL MODE	BOTH
A SEC/DIV	0.1 ms
B SEC/DIV	1 μs
SEC/DIV Variable	CAL detent
STORE/NON STORE	NON STORE (button out)

b. Select 0.l ms time markers from the time-mark generator.

c. Adjust the A/B SWP SEP control to separate the A and B Sweeps.

d. Position the start of the trace exactly on the 1st vertical graticule line using the Horizontal POSITION control.

e. Rotate the B DELAY TIME POSITION control fully counterclockwise.

f. ADJUST—Delay Start (R646) so that the intensified zone starts at 0.2 divisions.

g. Rotate the B DELAY TIME POSITION control fully clockwise.

h. ADJUST—D-End (R652) so that the intensified zone starts at 10.05 divisions.

i. Repeat parts e through h until no further improvement is noted.

j. Rotate the B DELAY TIME POSITION control until the 2nd A-Sweep time marker is aligned with a selected reference vertical graticule line on the B Sweep. Record the DLY> readout for part l.

k. Rotate the B DELAY TIME POSITION control until the 10th A-Sweep time marker is aligned with the same selected reference vertical graticule line on the B Sweep as in part j.

l. ADJUST—Delay Readout (R6119) until the DLY> readout display between the 2nd time marker and the 10th time marker is 0.800 ms.

9. Adjust High-Speed Timing (C703 and C713)

a. Set:

HORIZONTAL MODE	A
A SEC/DIV	1 μs
A SEC/DIV Variable	CAL detent

b. Select 1 μs time markers from the time-mark generator.

c. ADJUST—A High Speed Timing (C703) for 1 time marker per division over the center 8 divisions.

d. Set:

HORIZONTAL MODE	B
A SEC/DIV	2 μs
B SEC/DIV	1 μs

e. ADJUST—B High Speed Timing (C713) for 1 time marker per division over the center 8 divisions.

10. Adjust 5 ns Timing and Linearity (C775 and C785)

a. Set:

CH 1 VOLTS/DIV	0.2 V
Horizontal POSITION	Midrange
HORIZONTAL MODE	A
A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

b. Select 10 ns time markers from the time-mark generator.

c. Align the time markers with the vertical graticule lines using the Horizontal POSITION control.

d. ADJUST—5 ns Timing (C775 and C785 alternately) for one time marker every 2 divisions over the center 8 divisions of the magnified sweep.

e. CHECK—Time markers between the 2nd and 4th vertical graticule lines should be aligned within 0.05 division. If not, a slight compromise between timing and linearity should be made by readjusting the 5 ns Timing capacitors (C775 and C785).

11. Check Timing Accuracy and Linearity

a. Set:

CH 1 VOLTS/DIV	0.5 V
X10 Magnifier	Off (knob in)

b. Select 50 ns time markers from the time-marker generator.

c. Adjust the A TRIGGER LEVEL control for a stable, triggered display.

d. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

e. CHECK—Timing accuracy is within 2% (0.16 division at the 10th vertical graticule line), and linearity is within 5% (0.1 division over any 2 of the center 8 divisions).

NOTE

For checking the timing accuracy of the A SEC/DIV switch settings from 50 ms to 0.5 s, watch the time marker tips only at the 2nd and 10th vertical graticule lines while adjusting the Horizontal POSITION control.

f. Repeat parts c through e for the remaining A SEC/DIV and time-mark generator setting combinations shown in Table 5-7 under the "Normal (X1)" column.

g. Set:

A SEC/DIV	0.05 μs
X10 Magnifier	On (knob out)

h. Select 10 ns time markers from the time-mark generator.

i. Use the Horizontal POSITION control to align the 1st time marker that is 25 ns beyond the start of the sweep with the 2nd vertical graticule line.

j. CHECK—Timing accuracy is within 3% (0.24 division at the 10th vertical graticule line), and linearity is within 5% (0.1 division over any 2 of the center 8 divisions). Exclude any portion of the sweep past the 100th magnified division.

k. Repeat parts i and j for the remaining A SEC/DIV and time-mark generator setting combinations shown in Table 5-7 under the "X10 Magnified" column.

l. Set:

HORIZONTAL MODE	B
A SEC/DIV	0.1 μs
B SEC/DIV	0.05 μs
X10 Magnifier	Off (knob in)

Table 5-7

Settings for Timing Accuracy Checks

SEC/DIV Switch Setting	Time-Mark Generator Setting	
	Normal (X1)	X10 Magnified
0.05 μs	50 ns	10 ns
0.1 μs	0.1 μs	10 ns
0.2 μs	0.2 μs	20 ns
0.5 μs	0.5 μs	50 ns
1 μs	1 μs	0.1 μs
2 μs	2 μs	0.2 μs
5 μs	5 μs	0.5 μs
10 μs	10 μs	1 μs
20 μs	20 μs	2 μs
50 μs	50 μs	5 μs
0.1 ms	0.1 ms	10 μs
0.2 ms	0.2 ms	20 μs
0.5 ms	0.5 ms	50 μs
1 ms	1 ms	0.1 ms
2 ms	2 ms	0.2 ms
5 ms	5 ms	0.5 ms
10 ms	10 ms	1 ms
20 ms	20 ms	2 ms
50 ms	50 ms	5 ms
A Sweep Only		
0.1 s	0.1 s	10 ms
0.2 s	0.2 s	20 ms
0.5 s	0.5 s	50 ms

m. Repeat parts b through k for the B Sweep. Keep the A SEC/DIV switch one setting slower than the B SEC/DIV switch.

12. Check Delay Time Differential Accuracy

a. Set:

Channel 1 AC-GND-DC	GND
HORIZONTAL MODE	BOTH
A and B SEC/DIV	0.2 ms
X10 Magnifier	Off (knob in)
A TRIGGER MODE	P-P AUTO

b. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

c. Set the B DELAY TIME POSITION control fully counterclockwise.

d. CHECK—Intensified portion of the trace starts within 0.5 division of the start of the sweep.

e. Rotate the B DELAY TIME POSITION control fully clockwise.

f. CHECK—Intensified portion of the trace is past the 11th vertical graticule line.

g. Set the A and B SEC/DIV switch to 0.5 μs.

h. Repeat parts b through f.

i. Set:

Channel 1 AC-GND-DC	DC
B SEC/DIV	0.05 μs
B DELAY TIME POSITION	Fully counterclockwise

j. Select 0.5 μs time markers from the time-mark generator.

k. Rotate the B DELAY TIME POSITION control so that the top of the 2nd time marker on the B Sweep is aligned with a selected reference vertical line. Record the DLY> readout for part m.

l. Rotate the B DELAY TIME POSITION control fully clockwise until the top of the 10th time marker on the B Sweep is aligned with the same selected reference vertical line as in part k. Record the DLY> readout for part m.

m. CHECK—Delay time readout is within the limits given in Table 5-8 (Delay Readout Limits column) by subtracting the delay time reading in part k from part l.

n. Repeat parts k through m for the remaining B SEC/DIV and time-mark generator settings given in Table 5-8, check the 8-division delay time accuracy for each A SEC/DIV switch setting given in column 1 of the table.

Table 5-8

Settings for Delay Time Differential Checks

Time-Mark Generator and A SEC/DIV Settings	B SEC/DIV Setting	Eight Division Delay	Delay Readout Limits
0.5 μs	0.05 μs	4.000 μs	3.948 to 4.052 μs
5 μs	0.5 μs	40.00 μs	39.48 to 40.52 μs
50 μs	5 μs	400.0 μs	394.8 to 405.2 μs
0.5 ms	50 μs	4.000 ms	3.948 to 4.052 ms
5 ms	0.5 ms	40.00 ms	39.48 to 40.52 ms
50 ms	5 ms	400.0 ms	394.8 to 405.2 ms
0.5 s	50 ms	4.000 s	3.948 to 4.052 s

13. Check Delay Jitter

a. Set:

A SEC/DIV	0.5 ms
B SEC/DIV	0.5 μs
B DELAY TIME POSITION	Fully clockwise

b. Select 50 μs time markers from the time-mark generator.

c. Rotate the B DELAY TIME POSITION control counterclockwise to position a time marker within the graticule area for each major dial division and CHECK that the jitter on the leading edge does not exceed 0.5 division. Disregard slow drift.

14. Adjust Vector Generator (R6312 and R6321)

a. Set the WAVEFORM REFERENCE/MENU SELECT switch to MENU SELECT (button out).

b. Use the Menu controls to display rectangle test waveforms on the screen by selecting ADVANCE FUNCTIONS, DIAGNOSTICS, CAL AIDS, and BOX in that order.

c. ADJUST—X and Y Vector/Dot Alignment (R6312 and R6321) for best displays of the delta symbols (no tails or tilting) located at each of the four corners on the screen.

15. Adjust Store X Offset and Gain (R9214 and R9212)

a. ADJUST—Store X Offset (R9214) so that the left trace of the outside box is exactly aligned with the 1st vertical graticule line.

b. ADJUST—Store X Gain (R9212) so that the inside box is exactly 8 divisions wide. The inside box is horizontally centered with the Horizontal POSITION control.

c. INTERACTION—Repeat parts a and b until the inside box is exactly 8 horizontal divisions wide and the left trace of the outside box is aligned with the 1st vertical graticule line.

16. Adjust Clock Delay Timer (R4213 and C4202)

a. Use the Menu controls to select CAL__CLK__DLY.

b. ADJUST—CDT XY (R4213) to vertically align the horizontal trace with the center horizontal graticule line.

c. ADJUST—CDT X (C4202) to horizontally align the vertical trace with the center vertical graticule line. Both traces will intersect within the center box.

d. Repeat part b and c until both traces are aligned with the center graticule lines within the boxes.

17. Check Store Differential and Cursor Time Difference Accuracy

a. Set:

Channel 1 AC-GND-DC	GND
HORIZONTAL MODE	A
A SEC/DIV	0.1 ms
STORE/NON STORE	STORE (button in)
1K/4K	1K (button in)

b. Use the Channel 1 POSITION control to center the base line vertically and the Horizontal POSITION control to align the start of the trace with the 1st vertical graticule line.

c. Use the CURSORS control and SELECT C1/C2 switch to set one cursor exactly on the 2nd vertical graticule line and position the active cursor to the right using the CURSORS control until ΔT readout displays 0.800 ms.

d. CHECK—Graticule indication of cursor difference at the 10th vertical graticule line is within 0.16 division.

e. Set the Channel 1 AC-GND-DC switch to DC.

f. Select 0.1 ms time markers from the time-mark generator.

g. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

h. Set the SAVE/CONTINUE switch to SAVE (button in) for a stable display.

i. Use the CURSORS control and SELECT C1/C2 switch to set the first cursor on the trailing edge of the 2nd time marker.

j. Press in the C1/C2 button to activate the second cursor.

k. Set the second cursor on the trailing edge of the 10th time marker at the same voltage level as on the 2nd time marker.

l. CHECK—The ΔT readout is between 0.798 ms and 0.802 ms.

m. Set the SAVE/CONTINUE switch to CONTINUE (button out).

n. Set the A SEC/DIV switch to 0.5 μs.

o. Select 0.5 μs time markers from the time-mark generator.

p. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

NOTE

Allow the points to accumulate for a few seconds before saving the display.

q. Repeat parts h through k.

NOTE

Pulses with fast rise and fall times have only a few sample points, and it may not be possible to place the cursors at exactly the same voltage levels.

r. CHECK—The ΔT readout is between 397.0 ns and 403.0 ns.

18. Check Store Expansion Range

a. Set:

A SEC/DIV	0.1 ms
SAVE/CONTINUE	CONTINUE (knob out)

b. Select 10 μs time markers from the time-mark generator.

c. Use the Horizontal POSITION control to align the start of the A Sweep with the 1st vertical graticule line.

d. Set the X10 Magnifier knob to On (knob out).

e. CHECK—The time markers are 1 division apart.

19. Check A/B Sweep Separation

a. Set:

HORIZONTAL MODE	BOTH
A and B SEC/DIV	0.5 ms
STORE/NON STORE	NON STORE

b. Use the Channel 1 POSITION control to set the A Sweep at the center horizontal graticule line.

c. CHECK—The B Sweep can be positioned more than 3.5 divisions above and below the A Sweep when the A/B SWP SEP control is rotated fully clockwise and counterclockwise respectively.

20. Adjust X Gain (R760)

a. Set:

X-Y	On (button in)
CH 1 VOLTS/DIV	10 mV
Horizontal POSITION	Midrange

b. Connect the standard-amplitude signal from the Calibration Generator via a 50 Ω cable to the CH 1 OR X input connector.

c. Use the Channel 2 POSITION and Horizontal POSITION controls to center the display.

d. Set the generator to produce a 50 mV signal.

e. ADJUST—X-Gain (R760) for exactly 5 divisions of horizontal deflection.

f. Disconnect the test equipment from the instrument.

21. Check X-Y Store

a. Set the STORE/NON STORE switch to STORE (button in).

b. Set the generator to produce a 50 mV signal.

c. CHECK—The display can be move vertically and horizontally with the Channel 2 POSITION and Horizontal POSITION controls.

d. Set the SAVE/CONTINUE switch to SAVE (button in).

e. Repeat part c.

f. Disconnect the test equipment from the instrument.

22. Check X Bandwidth

a. Set:

CH 2 AC-GND-DC	GND
STORE/NON STORE	NON STORE (button out)

b. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 5-division horizontal display at an output frequency of 50 kHz.

d. Increase the generator output frequency to 2.5 MHz.

e. CHECK—Display is at least 3.5 horizontal divisions.

f. Disconnect the test equipment from the instrument.

23. Check A-Sweep Holdoff

a. Set:

X-Y	Off (button out)
HORIZONTAL MODE	A
A SEC/DIV	1 ms
VAR HOLDOFF	NORM

b. Connect the test oscilloscope and its 10X probe tip to the front end of R707 (toward the front panel) which is located on the Timing circuit board.

c. CHECK—The A-Sweep holdoff is greater then 3 ms but less than 7 ms.

d. Rotate the VAR HOLDOFF control to the maximum clockwise position (MAX).

e. CHECK—The A-Sweep holdoff has increased by a factor of 10 or more.

f. Disconnect the test oscilloscope 10X probe from R707.

TRIGGER

Equipment Required (See Table 4-1):

- Leveled Sine-Wave Generator (Item 2)
- Low-Frequency Generator (Item 4)
- 50 Ω BNC Cable (Item 8)
- Dual-Input Coupler (Item 9)
- BNC T-Connector (Item 11)
- 50 Ω BNC Termination (Item 12)
- 600 Ω BNC Termination (Item 13)
- Screwdriver (Item 19)

See ADJUSTMENT LOCATIONS 1 *and* ADJUSTMENT LOCATIONS 3 *at the back of the manual for test points and adjustment locations.*

INITIAL CONTROL SETTINGS

Vertical (Both Channels)

POSITION	Midrange
VERTICAL MODE	BOTH-ALT
X-Y	Off (button out)
BW LIMIT	Off (button out)
VOLTS/DIV	0.5 V
VOLTS/DIV Variable	CAL detent
INVERT	Off (button out)
AC-GND-DC	GND

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
A and B SEC/DIV	1 ms
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)
B DELAY TIME POSITION	Fully counterclockwise

B TRIGGER

SLOPE	OUT
LEVEL	Midrange

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT
A EXT COUPLING	AC

Storage

STORE/NON	STORE
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Adjust Channel 1 Trigger Offset (R309)

a. Set the Channel 1 trace and the Channel 2 trace to the center horizontal graticule line using the Channel 1 and Channel 2 POSITION controls.

b. Connect the digital voltmeter low lead to chassis ground and the high (volts) lead to TP460, located on the bottom side of the Main circuit board.

c. CHECK—Note the offset voltage reading at TP460 for use in part e.

d. Set the A&B INT switch to CH 1.

e. ADJUST—Trig Offset (R309) so that the voltage reading is the same as that obtained in part c.

f. Set the A&B INT switch to CH 2.

g. Repeat parts c through f until there is 1 mV or less difference in the voltmeter readings between the CH 1 and CH 2 positions of the A&B INT switch.

h. Disconnect the test equipment from the instrument.

2. Adjust A and B Trigger Sensitivity (R471 and R627)

a. Set:

VERTICAL MODE	CH 1
CH 1 VOLTS/DIV	0.1 V
AC-GND-DC (both)	AC
A SEC/DIV	10 μs

b. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 50 kHz, 2.2-division display.

d. Set the CH 1 VOLTS/DIV switch to 1 V.

e. ADJUST—Trig Sens (R471) while rotating the A TRIGGER LEVEL control slowly so that the A Trigger is just able to be maintained.

f. Set the HORIZONTAL MODE switch to B.

g. ADJUST—B Trig Sens (R627) while rotating the B TRIGGER LEVEL control slowly so that the B Trigger is just able to be maintained.

3. Adjust P-P Auto Level (R434 and R435)

a. Set:

CH 1 VOLTS/DIV	50 mV
A TRIGGER SLOPE	OUT
A TRIGGER LEVEL	Fully clockwise

b. Set the leveled sine-wave generator to produce a 50 kHz, 6-division display.

c. Set the CH 1 VOLTS/DIV switch to 0.5 V.

d. ADJUST—(+) P-P Auto Level (R434) so that the vertical display just solidly triggers on the positive peak of the signal.

e. Set:

A TRIGGER SLOPE	IN
A TRIGGER LEVEL	Fully counterclockwise

f. ADJUST—(−) P-P Auto Level (R435) so that the display just solidly triggers on the negative peak of the signal.

g. Disconnect the test equipment from the instrument.

4. Check Internal A and B Triggering

a. Set:

CH 1 VOLTS/DIV	5 mV
CH 2 VOLTS/DIV	50 mV
HORIZONTAL MODE	A
A and B SEC/DIV	0.2 μs
A&B INT	CH 1
A SOURCE	INT

b. Connect the leveled sine-wave generator output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 10 MHz, 3-division display.

d. Set the CH 1 VOLTS/DIV switch to 50 mV.

e. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 5-9.

Table 5-9

Switch Combinations for A Triggering Checks

A TRIGGER Mode	A TRIGGER SLOPE
NORM	OUT
NORM	IN
P-P AUTO	IN
P-P AUTO	OUT

f. Set the HORIZONTAL MODE switch to B.

g. CHECK—Stable display can be obtained by adjusting the B TRIGGER LEVEL control in a position other than the B RUNS AFTER DLY position for both the OUT and IN positions of the B TRIGGER SLOPE switch.

h. Set:

VERTICAL MODE	CH 2
HORIZONTAL MODE	A
A&B INT	CH 2

i. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

j. Repeat parts e through g.

k. Set:

HORIZONTAL MODE	A
A SEC/DIV	0.1 μs
X10 Magnifier	On (knob out)

l. Set the generator to produce a 60 MHz, 1.0-division display.

m. Repeat parts e through g.

n. Set:

VERTICAL MODE	CH 1
HORIZONTAL MODE	A
A&B INT	CH 1

o. Move the cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.

p. Repeat parts e through g.

q. Set:

HORIZONTAL MODE	A
A SEC/DIV	0.05 μs

r. Set the generator to produce a 100 MHz, 1.5-division display.

s. Repeat parts e through g.

t. Set:

VERTICAL MODE	CH 2
HORIZONTAL MODE	A
A&B INT	CH 2

u. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

v. Repeat parts e through g.

w. Disconnect the test equipment from the instrument.

5. Check HF Reject A Triggering

a. Set:

VERTICAL MODE	CH 1
VOLTS/DIV (both)	50 mV
HORIZONTAL MODE	A
A SEC/DIV	5 μs
A TRIGGER Mode	NORM
A TRIGGER LEVEL	Midrange
A&B INT	CH 1

b. Connect the low-frequency generator output via a 50 Ω cable and a 600 Ω termination to the CH 1 OR X input connector.

c. Set the low-frequency generator output to produce a 250 kHz, 1-division display.

d. Adjust the A TRIGGER LEVEL control for a stable display.

e. Set HF REJECT switch to ON.

f. CHECK—Stable display cannot be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 5-9.

g. Set:

VERTICAL MODE	CH 2
A&B INT	CH 2

h. Move the cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.

i. Repeat part f.

j. Disconnect the test equipment from the instrument.

6. Check External Triggering

a. Set:

VERTICAL MODE	CH 1
CH 1 VOLTS/DIV	5 mV
HORIZONTAL MODE	A
A SEC/DIV	0.1 μs
X10 Magnifier	Off (knob in)
HF REJECT	OFF
A&B INT	CH 1
A SOURCE	EXT

b. Connect the leveled sine-wave generator output via a 50 Ω cable, a 50 Ω termination, and a dual-input coupler to both the CH 1 OR X and EXT INPUT connectors.

c. Set the leveled sine-wave generator output voltage to 35 mV and the frequency to 10 MHz.

d. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control for each switch combination given in Table 5-9.

e. Set CH 1 VOLTS/DIV switch to 50 mV.

f. Set the generator output voltage to 120 mV and the frequency to 60 MHz. Set the X10 Magnifier to On (knob out).

g. Repeat part d.

h. Set the generator output voltage to 150 mV and the frequency to 100 MHz.

i. Repeat part d.

7. Check External Trigger Ranges

a. Set:

CH 1 VOLTS/DIV	0.5 V
A SEC/DIV	20 μs
X10 Magnifier	Off (knob in)
A TRIGGER SLOPE	OUT
A TRIGGER Mode	NORM

b. Set the generator to produce a 50 kHz, 6.4-division display.

c. CHECK—Display is triggered along the entire positive slope of the waveform as the A TRIGGER LEVEL control is rotated.

d. CHECK—Display is not triggered (no trace) at either extreme of rotation.

e. Set the A TRIGGER SLOPE button to IN.

f. CHECK—Display is triggered along the entire negative slope of the waveform as the A TRIGGER LEVEL control is rotated.

g. CHECK—Display is not triggered (no trace) at either extreme of rotation.

8. Check Single Sweep Operation

a. Adjust the A TRIGGER LEVEL control to obtain a stable display.

b. Set:

Channel 1 AC-GND-DC	GND
A SOURCE	INT

c. Press in the SGL SWP button. The READY LED should illuminate and remain on.

d. Set the Channel 1 AC-GND-DC switch to DC.

NOTE

The A INTENSITY control may require adjustment to observe the single-sweep trace.

e. CHECK—READY LED goes out and a single sweep occurs.

f. Press in the SGL SWP button several times.

g. CHECK—Single-sweep trace occurs, and the READY LED illuminates briefly every time the SGL SWP button is pressed in and released.

h. Disconnect the test equipment from the instrument.

9. Check Acquisition Window Trigger Point

a. Set:

A TRIGGER Mode	P-P AUTO
1K/4K	4K (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
WAVEFORM REFERENCE/ MENU SELECT	MENU SELECT (button out)

b. Use the Menu controls to select A TRIG POS.

c. CHECK—The A TRIG POS default number is 512.

d. Press in momentarily the PRETRIG/POST TRIG switch to activate the trigger point display on the crt. Return the PRETRIG/POST TRIG switch to POST TRIG (button out).

e. CHECK—The trigger point (T) appears near the 2nd vertical graticule line below the Menu.

f. Set the PRETRIG/POST TRIG switch to PRETRIG (button in).

g. CHECK—The A TRIG POS default number is 3584 and the trigger point (T) appears near the 9th vertical graticule line below the Menu.

h. Set the 1K/4K switch to 1K (button in).

i. CHECK—The A TRIG POS default number is 896 and the trigger point (T) appears near the 9th vertical graticule line below the Menu.

j. Set the PRETRIG/POST TRIG switch to POST TRIG (button out).

k. CHECK—The A TRIG POS default number is 128 and the trigger point (T) appears near the 2nd vertical graticule line below the Menu.

l. CHECK—The trigger point (T) can be moved between the 1st and the center vertical graticule lines as the CURSORS control is rotated.

m. Set the PRETRIG/POST TRIG switch to PRETRIG (button in).

n. CHECK—The trigger point (T) can be moved between the 10th and the center vertical graticule lines as the CURSORS control is rotated.

o. Set the 1K/4K switch to 4K (button out).

p. Repeat part n for PRETRIG mode and part l for POST TRIG mode.

EXTERNAL Z-AXIS, PROBE ADJUST, EXTERNAL CLOCK, AND X-Y PLOTTER

Equipment Required (see Table 4-1):

- Leveled Sine-Wave Generator (Item 2)
- Pulse Generator (Item 5)
- Two 50 Ω BNC Cables (Item 8)
- BNC T-Connector (Item 11)
- 50 Ω BNC Termination (Item 12)
- BNC Male-to-Tip Plug (Item 17)
- 10X Probe (Proveded with Instrument)

INITIAL CONTROL SETTINGS

Vertical

Channel 1 POSITION	Midrange
VERTICAL MODE	CH 1
X-Y	Off (button out)
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	1 V
CH 1 VOLTS/DIV Variable	CAL detent
Channel 1 AC-GND-DC	DC

Horizontal

POSITION	Midrange
HORIZONTAL MODE	A
A SEC/DIV	20 μs
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE/ MENU SELECT	WAVEFORM REFERENCE (button in)

PROCEDURE STEPS

1. Check External Z-Axis Operation

a. Connect the leveled sine-wave generator output via a 50 Ω cable and a T-connector to the CH 1 OR X input connector. Then connect a 50 Ω cable and a 50 Ω termination from the T-connector to the EXT Z AXIS INPUT connector on the rear panel.

b. Set the generator to produce a 5 V, 50 kHz signal.

c. CHECK—For noticeable intensity modulation. The positive part of the sine wave should be of lower intensity than the negative part.

d. Disconnect the test equipment from the instrument.

2. Check Probe Adjust Operation

a. Set:

CH 1 VOLTS/DIV	10 mV
A SEC/DIV	0.5 ms

b. Connect the 10X Probe to the CH 1 OR X input connector and insert the probe tip into the PROBE ADJUST jack on the instrument front panel. If necessary, adjust the probe compensation for a flat-topped square-wave display.

c. CHECK—Display amplitude is 4.75 to 5.25 divisions.

d. Disconnect the probe from the instrument.

3. Check External Clock

a. Set:

CH 1 VOLTS/DIV	1 V
X-Y	Off (button out)
A SEC/DIV	1 ms

b. Connect the pulse generator high-amplitude output via a 50 Ω cable and a 50 Ω termination to the CH 1 OR X input connector.

c. Set the generator to produce a 1 kHz, 5-division display.

d. Disconnect the cable from the CH 1 OR X input connector and connect it to the BNC male-to-tip plug via BNC female-to-BNC-female connector.

e. Insert the BNC male-to-tip plug signal lead and ground lead into pin 1 and pin 9 respectively of the X-Y Plotter connector.

f. Set the A SEC/DIV switch to 0.1 sec.

g. Connect the calibration generator high-amplitude output via a 50 Ω cable and a 50 Ω termination to CH 1 OR X input connector.

h. Set the generator to produce a 100 Hz, 5-division display.

i. Set:

A SEC/DIV	EXT CLK
STORE/NON STORE	STORE (button in)
SAVE/CONTINUE	CONTINUE (button out)

j. CHECK—The 100 Hz signal is displayed on the screen and updated.

k. Set the SAVE/CONTINUE switch to SAVE (button in).

l. CHECK—The display is saved.

m. Disconnect the test equipment from the instrument.

4. Check X-Y Plotter

a. Connect the digital voltmeter low lead to either chassis ground or pin 9 (signal ground) of the X-Y Plotter connector. Connect the volts lead to pin 3 (X Output) of the X-Y Plotter connector.

b. Set the digital voltmeter to the 20 V scale.

c. Set the WAVEFORM REFERENCE/MENU SELECT switch to MENU SELECT (button out).

d. Use the Menu controls to select PLOT and then ON for GRATICULE.

e. Press in momentarily the CURSORS button to activate the X-Y Plotter.

NOTE

Voltage reading of the X Output will be negative left of the center vertical graticule line and positive to the right of the center vertical graticule line. Voltage reading of the Y Output will be negative below the center horizontal graticule line and positive above the center horizontal graticule line.

f. Record the voltage reading as the instrument plots the 1st and the 10th graticule line (as the intensity spot moves along the graticule line).

g. CHECK—The voltage difference between the 1st and 10th graticule line is between 4.5 V and 5.5 V.

h. Move the volts lead of the voltmeter from pin 3 (X Output) to pin 5 (Y Output) of the X-Y Plotter connector.

i. Press in momentarily the CURSORS button to activate the X-Y Plotter.

j. Record the voltage reading as the instrument plots the top and the bottom graticule line (as the intensity spot moves along the graticule line).

k. CHECK—The voltage difference between the top and bottom graticule lines is between 3.6 V and 4.4 V.

l. Disconnect the test equipment from the instrument.

MAINTENANCE

This section contains information for conducting preventive maintenance, troubleshooting, and corrective maintenance on the instrument. Circuit board removal procedures are included in the corrective maintenance part of this section.

STATIC-SENSITIVE COMPONENTS

The following precautions are applicable when performing any maintenance involving internal access to the instrument.

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.

3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by their bodies, never by their leads.

Table 6-1

Relative Susceptibility to Static-Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a]Voltage equivalent for levels (voltage discharged from a 100 pF capacitor through a resistance of 100 ohms):

1 = 100 to 500 V
2 = 200 to 500 V
3 = 250 V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V (est)
8 = 900 V
9 = 1200 V

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

PREVENTIVE MAINTENANCE

INTRODUCTION

Preventive maintenance consists of cleaning, visual inspection, and checking instrument performance. When performed regularly, it may prevent instrument malfunction and enhance instrument reliability. The severity of the environment in which the instrument is used determines the required frequency of maintenance. An appropriate time to accomplish preventive maintenance is just before instrument adjustment.

GENERAL CARE

The cabinet minimizes accumulation of dust inside the instrument and should normally be in place when operating the oscilloscope. The front cover supplied with the instrument provides both dust and damage protection for the front panel and crt. The front cover should be on whenever the instrument is stored or is being transported.

INSPECTION AND CLEANING

The instrument should be visually inspected and cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket, preventing efficient heat dissipation. It also provides an electrical conduction path that could result in instrument failure, especially under high-humidity conditions.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue-type cleaner, preferably isopropyl alcohol or a solution of 1% mild detergent with 99% water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Exterior

INSPECTION. Inspect the external portions of the instrument for damage, wear, and missing parts; use Table 6-2 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance. Deficiencies found that could cause personal injury or could lead to further damage to the instrument should be repaired immediately.

CAUTION

To prevent getting moisture inside the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

CLEANING. Loose dust on the outside of the instrument can be removed with a soft cloth or small soft-bristle brush. The brush is particularly useful for dislodging dirt on and around the controls and connectors. Dirt that remains can be removed with a soft cloth dampened in a mild detergent-and-water solution. Do not use abrasive cleaners.

A plastic light filter is provided with the oscilloscope. Clean the light filter and the crt face with a soft lint-free cloth dampened with either isopropyl alcohol or a mild detergent-and-water solution.

Interior

To gain access to internal portions of the instrument for inspection and cleaning, refer to the "Removal and Replacement Instructions" in the "Corrective Maintenance" part of this section.

INSPECTION. Inspect the internal portions of the instrument for damage and wear, using Table 6-3 as a guide. Deficiencies found should be repaired immediately. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

Table 6-2

External Inspection Check List

Item	Inspect For	Repair Action
Cabinet, Front Panel, and Cover	Cracks, scratches, deformations, damaged hardware or gaskets.	Touch up paint scratches and replace defective components.
Front-panel Controls	Missing, damaged, or loose knobs, buttons, and controls.	Repair or replace missing or defective items.
Connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective parts. Clean or wash out dirt.
Carrying Handle	Correct operation.	Replace defective parts.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective parts.

Table 6-3

Internal Inspection Checklist

Item	Inspect For	Repair Action
Circuit Boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating.	Clean solder corrosion with an eraser and flush with isopropyl alcohol. Resolder defective connections. Determine cause of burned items and repair. Repair defective circuit runs.
Resistors	Burned, cracked, broken, blistered.	Replace defective resistors. Check for cause of burned component and repair as necessary.
Solder Connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.
Capacitors	Damaged or leaking cases. Corroded solder on leads or terminals.	Replace defective capacitors. Clean solder connections and flush with isopropyl alcohol.
Semiconductors	Loosely inserted in sockets. Distorted pins.	Firmly seat loose semiconductors. Remove devices having distorted pins. Carefully straighten pins (as required to fit the socket), using long-nose pliers, and reinsert firmly. Ensure that straightening action does not crack pins, causing them to break off.
Wiring and Cables	Loose plugs or connectors. Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace defective wires or cables.
Chassis	Dents, deformations, and damaged hardware.	Straighten, repair, or replace defective hardware.

If any electrical component is replaced, conduct a Performance Check for the affected circuit and for other closely related circuits (see Section 4). If repair or replacement work is done on any of the power supplies, conduct a complete Performance Check and, if so indicated, an instrument readjustment (see Sections 4 and 5).

CAUTION

To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the instrument.

CLEANING. To clean the interior, blow off dust with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft brush or a cloth dampened with a solution of mild detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards. If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of 5% mild detergent and 95% water as follows:

1. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see "Removal and Replacement Instructions").

2. Spray wash dirty parts with the detergent-and-water solution; then use clean water to thoroughly rinse them.

3. Dry all parts with low-pressure air.

4. Dry all components and assemblies in an over or drying compartment using low-temperature (125°F to 150°F) circulating air.

SWITCH CONTACTS. The VOLTS/DIV and SEC/DIV switches are mounted on circuit boards within the instrument. Care must be exercised to preserve the high-frequency characteristics of these switches. Switch maintenance is seldom necessary, but if required, use this procedure.

1. Cam-activated VOLTS/DIV Attenuator switches.

CAUTION

Most spray-type circuit coolants contain Freon 12 as a propellant. Because many Freons adversely affect switch contacts, do not use spray-type coolants on the switches or attenuators.

The only recommended circuit coolants for the VOLT/DIV attenuators are dry ice (CO_2) and isopropyl alcohol.

a. Use only isopropyl alcohol as a cleaning agent for switches, especially in the area of the Vertical Attenuator circuit board. Carbon based solvents will damage the board material.

b. Apply the alcohol with a small, camel-hair brush. Do not use cotton tipped applicators as the cotton tends to snag and possibly damage the switch contacts.

2. Rotary-activated SEC/DIV switch contacts.

CAUTION

Use only deionized or distilled water at about 55°C (131°F) to clean the SEC/DIV timing switch. Tap water contains impurities that remain as residual deposits after evaporation.

a. Spray hot water into the slots at the top of each switch housing while rotating the switch control knob. Use an atomizing spray device, and spray for only about five seconds.

b. Dry the switch and circuit board on which it is mounted with dry low-pressure air.

c. Bake the switch and circuit board in an oven or drying compartment using dry circulating air at about 75°C (167°F) for 15 minutes.

LUBRICATION

Most of the potentiometers used in this instrument are permanently sealed and generally do not require periodic lubrication. All switches, both rotary- and lever-type, are installed with proper lubrication applied where necessary and will rarely require any additional lubrication. A regular periodic lubrication program for the instrument is therefore, not recommended.

SEMICONDUCTOR CHECKS

Periodic checks of the transistors and other semiconductors in the oscilloscope are not recommended. The best check of semiconductor performance is actual operation in the instrument.

PERIODIC READJUSTMENT

To ensure accurate measurements, check the performance of this instrument every 2000 hours of operation, or if used infrequently, once each year. In addition, replacement of components may necessitate readjustment of the affected circuits.

Complete Performance Check and Adjustment instructions are given in Sections 4 and 5. The Performance Check Procedure can also be helpful in localizing certain troubles in the instrument. In some cases, minor problems may be revealed or corrected by readjustment. If only a partial adjustment is performed, see the interaction chart, Table 5-1, for possible adjustment interaction with other circuits.

TROUBLESHOOTING

INTRODUCTION

Preventive maintenance performed on a regular basis should reveal most potential problems before an instrument malfunctions. However, should troubleshooting be required, the following information is provided to facilitate location of a fault. In addition, the material presented in the "Theory of Operation" and "Diagrams" sections of this manual may be helpful while troubleshooting.

TROUBLESHOOTING AIDS

Diagnostic Firmware

The operating firmware in this instrument contains diagnostic routines that aid in locating malfunctions of the digital storage portions of the instrument. When instrument power is applied, power-up kernel tests are performed to verify proper operation of the instrument's microprocessor, RAM and ROM. If a failure is detected, this information is passed on to the operator, if possible. The failure information directs the operator to the failing block of memory. If the failure is such that the processor can still execute the diagnostic routines, the user can call up specific tests to further check the failing circuitry. The specific diagnostic routines are explained later in this section.

Schematic Diagrams

Complete schematic diagrams are located on tabbed foldout pages in the "Diagrams" section. Portions of circuitry mounted on each circuit board are enclosed by heavy black lines. The assembly number and name of the circuit are shown near either the top or the bottom edge of the enclosed area.

Functional blocks on schematic diagrams are outlined with a wide grey line. Components within the outlined area perform the function designated by the block label. The "Theory of Operation" uses these functional block names when describing circuit operation as an aid in cross-referencing between the theory and the schematic diagrams.

Component numbers and electrical values of components in this instrument are shown on the schematic diagrams. Refer to the first page of the "Diagrams" section for the reference designators and symbols used to identify components. Important voltages and waveform reference numbers (enclosed in hexagonal-shaped boxes) are also shown on each diagram. Waveform illustrations are located adjacent to their respective schematic diagram.

Circuit Board Illustrations

Circuit board illustrations showing the physical location of each component are provided for use in conjunction with each schematic diagram. Each board illustration is found in the "Diagrams" section on the back of a foldout page, preceding the first schematic diagram(s) to which it relates.

The locations of waveform test points are marked on the circuit board illustrations with hexagonal outlined numbers corresponding to the waveform numbers on both the schematic diagram and the waveform illustrations.

Also provided in the "Diagrams" section is an illustration of the bottom side of the Main circuit board. This illustration aids in troubleshooting by showing the connection pads for the components mounted on the top side of the circuit board. By using this illustration, circuit tracing and probing for voltages and signals that are inaccessible from the top side of the board may be achieved without dismantling portions of the instrument.

Circuit Board Locations

The placement of each circuit board in the instrument is shown in board locator illustrations. These illustrations are located on foldout pages along with the circuit board illustration.

Circuit Board Interconnections

A circuit board interconnection diagram is provided in the "Diagrams" section to aid in tracing a signal path or power source between boards. All wire, plug, and jack numbers are shown along with their associated wire or pin numbers.

Power Distribution

Power Distribution diagrams (diagrams 10, 11, and 21) are provided to aid in troubleshooting power supply problems. This diagram shows the service jumper connections used to apply power to the various circuit boards. Excessive loading on a power supply by a circuit board fault may be isolated by disconnecting the appropriate service jumpers.

Grid Coordinate System

Each schematic diagram and circuit board illustration has a grid border along its left and top edges. A table located adjacent to each diagram lists the grid coordinates of each component shown on that diagram. To aid in physically locating components on the circuit board, this table also lists the grid coordinates of each component on the circuit board illustration.

Near each circuit board illustration is an alphanumeric listing of all components mounted on that board. The second column in each listing identifies the schematic diagram in which each component can be found. These component-locator tables are especially useful when more than one schematic diagram is associated with a particular circuit board.

Component Color Coding

Information regarding color codes and markings of resistors and capacitors is located on the color-coding illustration (Figure 9-1) at the beginning of the "Diagrams" section.

RESISTOR COLOR CODE. Resistors used in this instrument are carbon-film, composition, or precision metal-film types. They are usually color coded with the EIA color code; however, some metal-film type resistors may have the value printed on the body. The color code is interpreted starting with the stripe nearest to one end of the resistor. Composition resistors have four stripes; these represent two significant digits, a multiplier, and a tolerance value. Metal-film resistors have five stripes representing three significant digits, a multiplier, and a tolerance value.

CAPACITOR MARKINGS. Capacitance values of common disc capacitors and small electrolytics are marked on the side of the capacitor body. White ceramic capacitors are color coded in picofarads, using a modified EIA code.

Dipped tantalum capacitors are color coded in microfarads. The color dot indicates both the positive lead and the voltage rating. Since these capacitors are easily destroyed by reversed or excessive voltage, be careful to observe the polarity and voltage rating when replacing them.

DIODE COLOR CODE. The cathode end of each glass-encased diode is indicated by either a stripe, a series of stripes or a dot. For most diodes marked with a series of stripes, the color combination of the stripes identifies three digits of the Tektronix Part Number, using the resistor color-code system. The cathode and anode ends of a metal-encased diode may be identified by the diode symbol marked on its body.

Semiconductor Lead Configurations

Figure 9-2 in the "Diagrams" section shows the lead configurations for semiconductor devices used in the instrument. These lead configurations and case styles are typical of those used at completion of the instrument design. Vendor changes and performance improvement

changes may result in changes of case styles or lead configurations. If the device in question does not appear to match the configuration shown in Figure 9-2, examine the associated circuitry or consult the manufacturer's data sheet.

Multipin Connectors

Multipin connector orientation is indexed by two triangles; one on the holder and one on the circuit board. Slot numbers are usually molded into the holder. When a connection is made to circuit board pins, ensure that the index on the holder is aligned with the index on the circuit board (see Figure 6-1).

Storage Board Latch

WARNING

Turn off POWER switch before placing the Storage circuit board in Servicing Position.

While servicing the interior of the instrument, the Storage circuit board may be latched in the Servicing Position. See the "Storage Circuit Board in Servicing Position" in the "Removal and Replacement Instructions" part of this section. The two signal leads of the four-wire connectors P2111 and P2112 need to be grounded when disconnected from the Storage circuit board. Grounding the signal leads of P2111 and P2112 permits the VERTICAL POSITION controls to work properly.

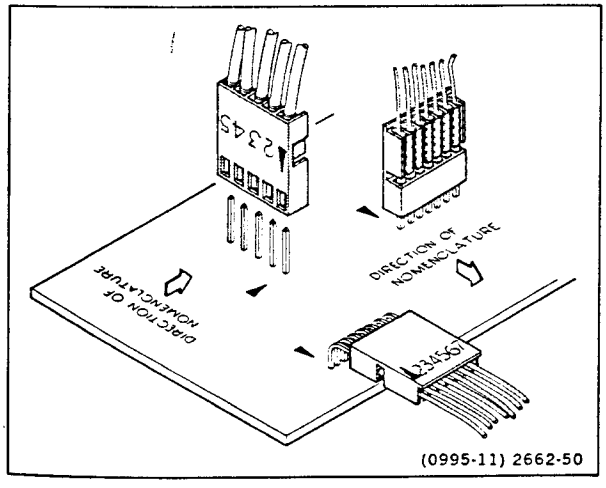


Figure 6-1. Multi-connector holder orientation.

The center signal leads may be connected to the outside ground leads of P2111 and P2112 by using four 1-inch long number 22 tinned copper wires (two wires for each connector). Bend the wires in a U-shape and insert the wires between pins 1 and 2, and between pins 3 and 4 of the connectors (see Figure 6-2).

Analog Isolation

The digital portion of the instrument may be isolated from the analog portion of the instrument. Use of this procedure enables disabling and isolation of the digital portion of the instrument while permitting troubleshooting on the analog portion.

1. Disconnect connectors P6110, P6120, and P6130 from the right edge of the Input/Output board (A11A1).

2. Disconnect connectors P6410 and P6420 from the right edge of the Vector Generator board (A11A2).

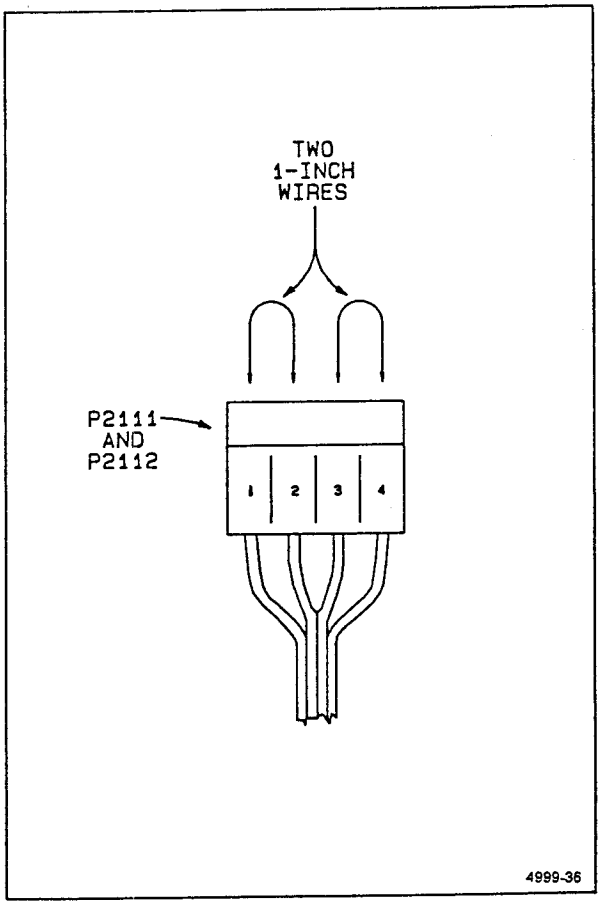


Figure 6-2. Grounding the signal lines of P2111 and P2112.

3. Disconnect connector P6421 from the Sweep Interface board (A13).

4. Disconnect connector P9010 from the middle right edge of the Main board (A1).

5. Latch Storage circuit board in the servicing position (see "Storage Circuit Board in the Servicing Position" in the "Removal and Replacement Instructions" part of this section.

6. Ground the two signal leads (pins 2 and 3) of four-wire connectors P2111 and P2112 (see preceding "Storage Board Latch" part of this section).

7. Disconnect connector P9410 from the Sweep Reference board (A16).

8. Connect together pins 2 and 4 of J9410.

9. Disconnect connector P4220 from the middle right side of the Alternate Sweep board (A5).

10. Disconnect connector P4210 from the middle right half of the Main board (A1).

11. Disconnect connector P9050 from the middle of the Main board (A1).

12. Disconnect connector P9060 from the middle of the Main board (A1).

13. Disconnect connector P9320 from the front of the Main board (A1).

14. Disconnect connector P9301 (P8100 if the instrument contains Option 10 or Option 12) from the middle left corner of the X/Y Plotter board.

Kernel Isolation

The Kernel (Microprocessor, Clock, and Address Latch) may be isolated from the rest of the circuitry. The Kernel can then be troubleshot. When the Kernel is functional, the power-up diagnostics may be used to further troubleshoot the digital circuitry. Isolate the Kernel by:

1. Removing P9105A.
2. Moving P9105B to its TEST position.
3. Moving P9105C to its TEST position.
4. Moving P9105D to its TEST position.

Figure 6-3 shows the isolated Kernel timing diagrams. After the Kernel is repaired, restore normal operation by using the reverse of the preceding procedure.

Switch Interface Voltages

Voltages generated by the interface to front-panel switches may be used to troubleshoot the instrument. Timing switch interface voltages are shown in Table 6-4. VERTICAL VOLTS/DIV switch interface voltages are shown in Table 6-5. Interface voltages for the AC GND DC switches are shown in Table 6-6.

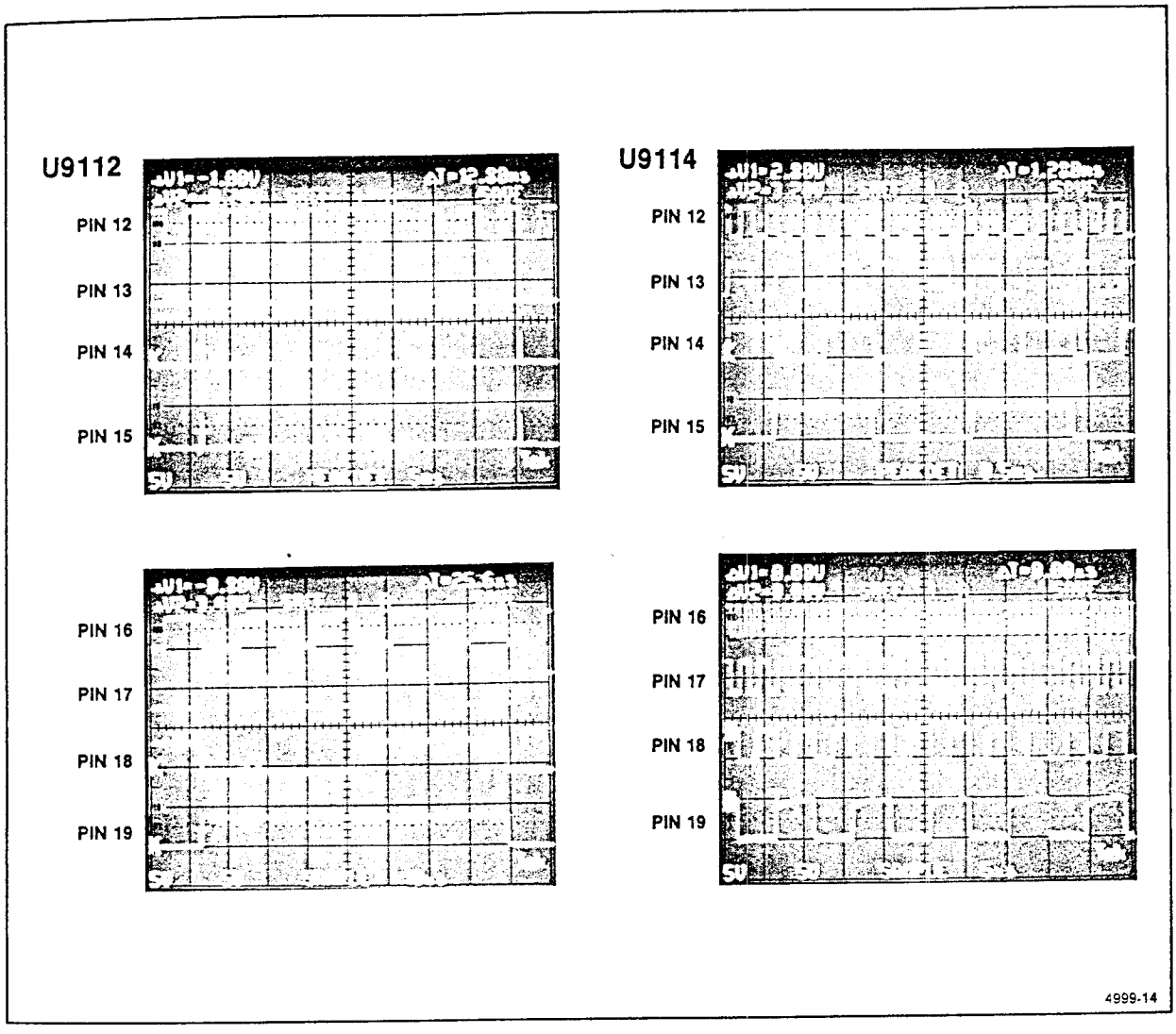


Figure 6-3. Isolated kernel timing.

Table 6-4

Timing Switch Interface Voltages

A and B SEC per DIV	ARES1 J6421 pin 2 Voltage Range	AC1 W6123 pin 1	AC2 W6123 pin 2	ARES2 J6421 pin 1 Voltage Range	B RES J6421 pin 5 Voltage Range	B CAPS J6421 pin 4
EXT CLK	4.591 to 5.100	5 V	5 V	3.742 to 4.590	2.510 to 3.546	3.2 to 5.0
0.5 s	4.591 to 5.100	0 V	5 V	4.591 to 5.100	2.510 to 3.546	3.2 to 5.0
0.2 s	4.591 to 5.100	0 V	5 V	3.742 to 4.590	2.510 to 3.546	3.2 to 5.0
0.1 s	4.591 to 5.100	0 V	5 V	2.716 to 3.742	2.510 to 3.546	3.2 to 5.0
50 ms	−0.250 to 1.150	0 V	5 V	4.591 to 5.100	2.510 to 3.546	3.2 to 5.0
20 ms	4.591 to 5.100	0 V	5 V	1.109 to 2.715	1.548 to 2.509	3.2 to 5.0
10 ms	4.591 to 5.100	0 V	5 V	−0.350 to 1.108	−0.200 to 0.612	3.2 to 5.0
5 ms	1.151 to 2.715	0 V	5 V	4.591 to 5.100	0.613 to 1.547	3.2 to 5.0
2 ms	3.743 to 4.590	0 V	5 V	4.591 to 5.100	4.227 to 4.752	3.2 to 5.0
1 ms	2.716 to 3.742	0 V	5 V	4.591 to 5.100	3.547 to 4.226	3.2 to 5.0
0.5 ms	−0.250 to 1.150	5 V	0 V	4.591 to 5.100	2.510 to 3.546	1.3 to 3.2
0.2 ms	4.591 to 5.100	5 V	0 V	1.109 to 2.715	1.548 to 2.509	1.3 to 3.2
0.1 ms	4.591 to 5.100	5 V	0 V	−0.350 to 1.108	−0.200 to 0.612	1.3 to 3.2
50 µs	1.151 to 2.715	5 V	0 V	4.591 to 5.100	0.613 to 1.547	1.3 to 3.2
20 µs	3.743 to 4.590	5 V	0 V	4.591 to 5.100	4.227 to 4.752	1.3 to 3.2
10 µs	2.716 to 3.742	5 V	0 V	4.591 to 5.100	3.547 to 4.226	1.3 to 3.2
5 µs	−0.250 to 1.150	0 V	0 V	4.591 to 5.100	2.510 to 3.546	−1.0 to 1.3
2 µs	4.591 to 5.100	0 V	0 V	1.109 to 2.715	1.548 to 2.509	−1.0 to 1.3
1 µs	4.591 to 5.100	0 V	0 V	−0.350 to 1.108	−0.200 to 0.612	−1.0 to 1.3
0.5 µs	1.151 to 2.715	0 V	0 V	4.591 to 5.100	0.613 to 1.547	−1.0 to 1.3
0.2 µs	3.743 to 4.590	0 V	0 V	4.591 to 5.100	4.227 to 4.752	−1.0 to 1.3
0.1 µs	2.716 to 3.742	0 V	0 V	4.591 to 5.100	3.547 to 4.226	−1.0 to 1.3
0.05 µs	4.591 to 5.100	0 V	0 V	4.591 to 5.100	4.753 to 5.100	−1.0 to 1.3

Table 6-5

Vertical VOLTS/DIV Switch Interface Voltages

SWITCH SETTING	CH1 ATN and CH2 ATN (J6111 pin 2 and J6112 pin 2)
2 mV per division	2.104 to 2.340
5 mV per division	4.167 to 4.712
10 mV per division	3.199 to 3.440
20 mV per division	2.502 to 2.702
50 mV per division	0 to 2.104
0.1 V per division	2.938 to 3.199
0.2 V per division	2.340 to 2.502
0.5 V per division	4.712 to 5.000+
1 V per division	3.731 to 4.167
2 V per division	3.440 to 3.731
5 V per division	2.702 to 2.938

Table 6-6

AC GND DC Switch Interface Voltages

Variable VOLTS/DIV	SWITCH POSITION	CH1 STAT and CH2 STAT (J6111 pin 3 and J6112 pin 3)
OUT OF DETENT	AC	0 to 2.423
	GND	2.696 to 3.070
	DC	3.623 to 4.457
IN DETENT	AC	2.423 to 2.696
	GND	3.070 to 3.623
	DC	4.457 to 5.000+

TROUBLESHOOTING EQUIPMENT

The equipment listed in Table 4-1 of this manual, or equivalent equipment, may be useful when troubleshooting this instrument.

TROUBLESHOOTING TECHNIQUES

The following procedure is arranged in an order that enables checking simple trouble possibilities before requiring more extensive troubleshooting. The first two steps use diagnostic aids inherent in the instrument's operating firmware and will locate many circuit faults. The next four steps ensure proper control settings, connections, operation, and adjustment. If the trouble is not located by these checks, the remaining steps will aid in locating the defective component. When the defective component is located, replace it using the appropriate replacement procedure given under "Corrective Maintenance" in this section.

CAUTION

Before using any test equipment to make measurements on static-sensitive, current-sensitive, or voltage-sensitive components or assemblies, ensure that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

1. Power-up Tests

The instrument performs automatic verification of the instrument's Microprocessor, ROM, and RAM (the operating kernel) when power is first applied. If all Kernel tests pass, a second level of diagnostic tests are performed. The Diagnostic tests, when passed, give the user a high degree of assurance that the instrument's storage circuitry is functioning properly.

If a diagnostic test fails, the faulty circuitry is identified by a message on the crt (if the instrument is able to produce a display), and by an LED display. If a failure occurs, refer to the "Diagnostics" discussion later in this section for definitions of error messages.

2. Diagnostic Test Routines

Many of the diagnostic routines may be selected from the front panel to further clarify the nature of a suspected failure. The desired test is selected using the MENU. The Diagnostics are explained in the "Diagnostics" discussion later in this section.

3. Check Control Settings

Incorrect control settings can give a false indication of instrument malfunction. If there is any question about the correct function or operation of any control, refer to either the "Operating Information" in Section 2 of this manual or to the Operators Manual.

4. Check Associated Equipment

Before proceeding, ensure that any equipment used with the instrument is operating correctly. Verify that input signals are properly connected and that the interconnecting cables are not defective. Check that the ac-power-source voltage to all equipment is correct.

5. Visual Check

WARNING

To avoid electrical shock, disconnect the instrument from the ac power source before making a visual inspection of the internal circuitry.

Perform a visual inspection. This check may reveal broken connections or wires, damaged components, semiconductors not firmly mounted, damaged circuit boards, or other clues to the cause of an instrument malfunction.

6. Check Instrument Performance and Adjustment

Check the performance of either those circuits where trouble appears to exist or the entire instrument. The apparent trouble may be the result of misadjustment. Complete performance check and adjustment instructions are given in Sections 4 and 5 of this manual.

7. Isolate Trouble to a Circuit

To isolate problems to a particular area, use any symptoms noticed to help locate the trouble. Refer to the "Diagnostics" discussion in this section as an aid in locating a faulty circuit.

8. Check Power Supplies

WARNING

For safety reasons, an isolation transformer must be connected whenever troubleshooting is done in the Preregulator and Inverter Power Supply sections of the instrument.

When trouble symptoms appear in more that one circuit, first check the power supplies; then check the affected circuits by taking voltage and waveform readings. Check first for the correct output voltage of each individual supply. These voltages are measured between the power supply test points and ground (see the associated circuit board illustration and Table 6-7).

Voltages levels may be measured either with a DMM or with an oscilloscope. Voltage ripple amplitudes must be measured using an oscilloscope. Before checking power-supply circuitry, set the INTENSITY control to normal brightness, the A and B SEC/DIV switch to 0.1 ms, the HORIZONTAL MODE to B, the ON/OFF READOUT TOGGLE to display the readout, the A TRIGGER Mode to P-P AUTO, and set the VERTICAL MODE switch to CH 1.

When measuring ripple, use a 1X probe having a bayonet ground assembly (see Table 6-7) attached to the probe tip to minimize stray pickup. Insert the bayonet assembly signal tip into the first test point indicated in Table 6-7, and touch the bayonet assembly ground tip to the chassis near the test point. The ripple values listed are based on a system limited in bandwidth to 30 kHz. Using a system with wider bandwidth will result in higher readings.

Table 6-7

Power Supply Voltage and Ripple Limits

Power Supply	Test Point	Reading (Volts)	P-P Ripple (mV)
−8.6 V	W961	−8.56 to −8.64	<1.5
−5.0 V	W9020	−4.75 to −5.25	<20
+5.0 V	W9068	+5.75 to +5.25	<20
+8.6 V	W960	+8.43 to +8.77	<8
+30 V	W956	+29.1 to +30.9	<30
+100 V	W954	+97.0 to +103.0	<100

If the power-supply voltages and ripple are within the ranges listed in Table 6-7, the supply can be assumed to be working correctly. If they are outside the range, the supply may be either misadjusted or operating incorrectly. Use the "Power Supply and CRT Display" subsection in the "Adjustment" procedure to adjust the −8.6 V supply.

A defective component elsewhere in the instrument can create the appearance of a power-supply problem and may also affect the operation of other circuits.

9. Check Circuit Board Interconnections

After the trouble has been isolated to a particular circuit, again check for loose or broken connections, improperly seated semiconductors, and heat-damaged components.

10. Check Voltages and Waveforms

Often the defective component can be located by checking circuit voltages or waveforms. Typical voltages are listed on the schematic diagrams. Waveforms indicated on the schematic diagrams by hexagonal-outlined numbers are shown adjacent to the diagrams. Waveform test points are shown on the circuit board illustrations.

NOTE

Voltages and waveforms indicated on the schematic diagrams are not absolute and may vary slightly between instruments. To establish operating conditions similar to those used to obtain these readings, see the "Voltage and Waveform Setup Conditions" preceding the waveform illustrations in the "Diagrams" section.

Note the recommended test equipment, front-panel control settings, voltage and waveform conditions, and cable-connection instructions. Any special control settings required to obtain a given waveform are noted under the waveform illustration. Changes to the control settings from the initial setup, other than those noted, are not required.

11. Check Individual Components

WARNING

To avoid electric shock, always disconnect the instrument from the ac power source before removing or replacing components.

The following procedures describe methods of checking individual components. Two-lead components that are soldered in place are most accurately checked by first disconnecting one end from the circuit board. This isolates the measurement from the effects of the surrounding circuitry. See Figure 9-1 for component value identification and Figure 9-2 for semiconductor lead configurations.

CAUTION

When checking semiconductors, observe the static-sensitivity precautions located at the beginning of this section.

TRANSISTORS. A good check of a transistor is actual performance under operating conditions. A transistor can most effectively be checked by substituting a known-good component. However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic-type transistor checker for testing. Static-type transistor checkers are not recommended, since they do not check operation under simulated operating conditions.

When troubleshooting transistors in the circuit with a voltmeter, measure both the emitter-to-base and emitter-to-collector voltages to determine whether they are consistent with normal circuit voltages. Voltages across a transistor may vary with the type of device and its circuit function.

Some of these voltages are predictable. The emitter-to-base voltage for a conducting silicon transistor will normally range from 0.6 V to 0.8 V. The emitter-to-collector voltage for a saturated transistor is about 0.2 V. Because these values are small, the best way to check them is by connecting a sensitive voltmeter across the junction rather that comparing two voltages taken with respect to ground. If the former method is used, both leads of the voltmeter must be isolated from ground.

If voltage values measured are less that those just given, either the device is shorted or no current is flowing in the external circuit. If values exceed the emitter-to-base values given, either the junction is reverse biased or the device is defective. Voltages exceeding those given for typical emitter-to-collector values could indicate either a nonsaturated device operating normally or a defective (open-circuited) transistor. If the device is conducting, voltage will be developed across the resistors in series with it; if open, no voltage will be developed across the resistors unless current is being supplied by a parallel path.

CAUTION

When checking emitter-to-base junctions, do not use an ohmmeter range that has a high internal current. High current may damage the transistor. Reverse biasing the emitter-to-base junction with a high current may degrade the current-transfer ratio (Beta) of the transistor.

A transistor emitter-to-base junction also can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter set to a range having a low internal source current, such as the R X 1 kΩ range. The junction resistance should be very high in one direction and much lower when the meter leads are reversed.

When troubleshooting a field-effect transistor (FET), the voltage across its elements can be checked in the same manner as previously described for other transistors. However, remember that in the normal depletion mode of operation, the gate-to-source junction is reverse biased; in the enhanced mode, the junction is forward biased.

INTEGRATED CIRCUITS. An integrated circuit (IC) can be checked with a voltmeter, test oscilloscope, or by direct substitution. A good understanding of circuit operation is essential when troubleshooting a circuit having IC components. Use care when checking voltages and waveforms around the IC so that adjacent leads are not shorted together. An IC test clip provides a convenient means of clipping a test probe to an IC.

CAUTION

When checking a diode, do not use an ohmmeter scale that has a high internal current. High current may damage a diode. Checks on diodes can be performed in much the same manner as those on transistor emitter-to-base junctions. Do not check tunnel diodes or back diodes with an ohmmeter; use a dynamic tester, such as the TEKTRONIX 576 Curve Tracer.

DIODES. A diode can be checked for either an open or a shorted condition by measuring the resistance between terminals with an ohmmeter set to a range having a low internal source current, such as the R X 1 kΩ range. The diode resistance should be very high in one direction and much lower when the meter leads are reversed.

Silicon diodes should have 0.6 V to 0.8 V across their junctions when conducting; Schottky diodes about 0.2 V to 0.4 V. Higher readings indicate that they are either reverse biased or defective, depending on polarity.

RESISTORS. Check resistors with an ohmmeter. Refer to the "Replaceable Electrical Parts" list for the tolerances of resistors used in this instrument. A resistor normally does not require replacement unless its measured value varies widely from its specified value and tolerance.

INDUCTORS. Check for open inductors by checking continuity with an ohmmeter. Shorted or partially shorted inductors can usually be found by checking the waveform response when high-frequency signals are passed through the circuit.

CAPACITORS. A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter set to one of the highest ranges. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after the capacitor is charged to the output voltage of the ohmmeter. An open capacitor can be detected with a capacitance meter or by checking whether the capacitor passes ac signals.

12. Repair and Adjust the Circuit

If any defective parts are located, follow the replacement procedures given under "Corrective Maintenance" in this section. After any electrical component has been replaced, the performance of that circuit and any other closely related circuit should be checked. Since the power supplies affect all circuits, performance of the entire instrument should be checked if work has been done on the power supplies or if the power transformer has been replaced. Readjustment of the affected circuitry may be necessary. Refer to the "Performance Check" and "Adjustment Procedure," Sections 4 and 5 of this manual and to Table 5-1 (Adjustment affected by repairs).

DIAGNOSTICS

Introduction

A list of the instrument diagnostic tests is shown in Table 6-8. The diagnostics are run automatically during power-up and/or manually via the menu. The location in the menu of each test is shown in Figure 6-4. Only the *digital storage* portion of the instrument is checked. Circuitry checked, and/or used by each test is shown in Table 6-9. During a normal power-up, only the first error of each test is displayed. If the CURSORS SELECT C1/C2 button is held in during power-up (invoking extended DIAGNOSTICS) the first 15 errors from all tests are displayed. If the instrument contains the RS-232-C Option, an ASCII version of all errors found during power-up is sent to the option. In addition to displaying the errors on the crt, the errors are also displayed on U4119 (see Table 6-10). Timing for the error codes displayed on U4119 is shown in Figure 6-5. A list of all possible error messages is shown in Table 6-11.

Table 6-8

Diagnostic Messages and Tests

MESSAGE[a]	POWER-UP	MENU
PU : <message>	X	
MI : <message>	X	
SYS_ROM_n : <message>		X
SYS_RAM : <message>		X
NIB_RAM : <message>		X
ACQ_AB : <message>	X	X
ACQ_MEM : <message>	X	X
PRC : <message>	X	X
HS_ACQ : <message>	X	X
TBD <rng> : <message>	X	X
MM_ACQ : <message>	X	X
XY_ACQ : <message>	X	X
CDT : <message>	X	X
FP_A2D : <message>	X	X

[a]Each n, message, and rng depend upon the detected failure.

Table 6-9

Circuitry Checked by Each Test and Exerciser

Test	Circuitry Checked
PU	KERNEL = Y4100, U4102, U9104, U9102, U9108, U9101, U9111, U9109, U9110, U9112, U9114, U9103, U9107, and U9113
MI	KERNEL, U9200, and U9105
SYS_ROM	KERNEL, and IO_BLOCK_DECODING = U9105, and U9106
SYS_RAM	KERNEL
NIB_RAM	KERNEL
ACQ_AB	KERNEL, IO_BLOCK_DECODING, U3423, U3424, U3425, U3427, U3428, and U3426
ACQ_MEM	KERNEL, IO_BLOCK_DECODING, U3423, U3424, U3425, U3427, U3428, U3426, U3418, U3419, U3421, U3422, U3417, U3416, U3420, and U3422
PRC	KERNEL, IO_BLOCK_DECODING, U4115, U4116, U4117, U4123, U4124, U4122, U4114, U4121, U4118, and U4119
HS_ACQ	KERNEL, IO_BLOCK_DECODING, PRC, ACQ_AB, ACQ_MEM, U4104, U4102, U4103, U4125, U4114, U4119, U4118, U4126, U4127, U4128, U4227, U4320, U3310, U3306, U3309, U3308, U3307, U3313, U3426, U3229, U3230, U3231, U3232, U3234, U3236, U3239, U4104, U3101, U3105, U3307, U3104, U3105, and U3308
TBD	KERNEL, IO_BLOCK_DECODING, HS_ACQ, U4107, U4108, U4109, U4110, U4111, U4112, U6106, U4105, U4103, U4127, U4113, and U4114
MM_ACQ	HS_ACQ
XY_ACQ	HS_ACQ
CDT	HS_ACQ, U4230, U4231, U4122, U4232, U4229, U4127, U4120, U4108, U3428, Q4207, Q4203, Q4204, Q4205, Rs, and Cs
FP_A2D	KERNEL, IO_BLOCK_DECODING, U6103, U6104, U6106, U6108, U6102, U6101, and R4912
CAL_PU	NMI, U9111, U9109, U9110, U9201, U9202, U9203, U9231, U9232, U9233, U9208, U3310, U6301A, U6301B, U6301C, U6303, U6304, U6305, U6306, U6307, U6308, U6401A, U6401B, U6401C, U6401D, U6401E, U6402A, U6402B, U6402C, U6402D, U6403A, and U6403D
OUT_PORTS	U3423, U3424, U3425, (U3427 U3428), U3310, U4119, U4113, and U6104

Table 6-10

U4119 Error Code Display

Test	U4119 Signal and Pin Number							
	AD7 12	AD6 13	AD5 14	AD4 15	AD0 16	AD1 17	AD2 18	AD3 19
ACQ TESTS HS	0	0	1	0	FILL	ACQ MEM	PRC	EOR
TBD HS/2 PS/2	0 0	0 1	1 0	1 0	FILL FILL	ACQ MEM ACQ MEM	PRC PRC	EOR EOR
PS/5	0	1	0	1	FILL	ACQ MEM	PRC	EOR
PS/10	0	1	1	0	FILL	ACQ MEM	PRC	EOR
/10	0	1	1	1	FILL	ACQ MEM	PRC	EOR
/100	1	0	0	0	FILL	ACQ MEM	PRC	EOR
/1K	1	0	0	1	FILL	ACQ MEM	PRC	EOR
/10K	1	0	1	0	FILL	ACQ MEM	PRC	EOR
/100K	1	0	1	1	FILL	ACQ MEM	PRC	EOR
MM_ACQ	1	1	0	0	FILL	ACQ MEM	PRC	EOR
XY	1	1	0	1	FILL	ACQ MEM	PRC	EOR
CDT	1	1	1	0	DELT UNCAL	MIN UNCAL	PRE DETRIG	TIMEOUT
FPA/D	1	1	1	1	GND	DELTA POT	0	TIMEOUT
MI	0	0	0	1	0	STUCK HI	NO RESET	TIMEOUT
PU	0	0	0	0	1	1	1	1
ACQ AB	0	0	0	0	1	0	0	1
ACQ MEM 1	0	0	0	0	0	1	0	1
ACQ MEM 2	0	0	0	0	1	1	0	1
PRC	0	0	0	0	0	0	1	1

Table 6-11

Diagnostic Messages

Access Group		Message
Power-up	Menu	
Power-up		PU : ROM/RAM/NMI : <hex_value>
Power-up		MI : line stuck high MI : Display controller : TIMEOUT MI : Display controller : unable to reset mi
	Menu	SYS_ROM_0 : <actual_check_sum> <> <expected_check_sum> SYS_ROM_1 : <actual_check_sum> <> <expected_check_sum>
	Menu	SYS_RAM : @ <address>
	Menu	NIB_RAM : @ <address>
Power-up	Menu	ACQ_AB : read-back <actual> <> <expected> (this message may appear more than once)
Power-up	Menu	ACQ_MEM : @ <address>
Power-up	Menu	PRC : read-back <actual> <> <expected> (this message may appear more than once)
Power-up	Menu	HS_ACQ : latent END_OF_RECORD HS_ACQ : acq_mem cntr <mem_actual> <> <mem_expected> HS_ACQ : prc <prc_actual> <> <prc_expected> HS_ACQ : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	TBD hs/2 : latent END_OF_RECORD TBD hs/2 : acq_mem cntr <mem_actual> <> <mem_expected> TBD hs/2 : prc <prc_actual> <> <prc_expected> TBD hs/2 : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	TBD ps/2 : latent END_OF_RECORD TBD ps/2 : acq_mem cntr <mem_actual> <> <mem_expected> TBD ps/2 : prc <prc_actual> <> <prc_expected> TBD ps/2 : fill @ <fill•ddress> : <fill_actual> <> <fill_expected>
Power-up	Menu	TBD ps/5 : latent END_OF_RECORD TBD ps/5 : acq_mem cntr <mem_actual> <> <mem_expected> TBD ps/5 : prc <prc_actual> <> <prc_expected> TBD ps/5 : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	TBD ps/10 : latent END_OF_RECORD TBD ps/10 : acq_mem cntr <mem_actual> <> <mem_expected> TBD ps/10 : prc <prc_actual> <> <prc_expected> TBD ps/10 : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	TBD /10 : latent END_OF_RECORD TBD /10 : acq_mem cntr <mem_actual> <> <mem_expected> TBD /10 : prc <prc_actual> <> <prc_expected> TBD /10 : fill @ <fill_address> : <fill_actual> <> <fill_expected>

Table 6-11 (cont)

Acess Group		Message
Power-up	Menu	
Power-up	Menu	TBD /100 : latent END_OF_RECORD TBD /100 : acq_mem cntr <mem_actual> <> <mem_expected> TBD /100 : prc <prc_actual> <> <prc_expected> TBD /100 : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	TBD /1k : latent END_OF_RECORD TBD /1k : acq_mem cntr <mem_actual> <> <mem_expected> TBD /1k : prc <prc_actual> <> <prc_expected> TBD /1k : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	TBD /10k : latent END_OF_RECORD TBD /10k : acq_mem cntr <mem_actual> <> <mem_expected> TBD /10k : prc <prc_actual> <> <prc_expected> TBD /10k : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	TBD /100k : latent END_OF_RECORD TBD /100k : acq_mem cntr <mem_actual> <> <mem_expected> TBD /100k : prc <prc_actual> <> <prc_expected> TBD /100k : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	MM_ACQ : latent END_OF_RECORD MM_ACQ : prc <prc_actual> <> <prc_expected> MM_ACQ : acq_mem cntr <acq_mem_actual> <> <acq_mem_expected> MM_ACQ : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	XY_ACQ : latent END_OF_RECORD XY_ACQ : prc <prc_actual> <> <prc_expected> XY_ACQ : acq_mem cntr <acq_mem_actual> <> <acq_mem_expected> XY_ACQ : fill @ <fill_address> : <fill_actual> <> <fill_expected>
Power-up	Menu	CDT : TIMED-OUT <tb_mode_reg_pattern> CDT : PRE_DETRIG <tb_mode_reg_pattern> CDT : uncaled : min = <min_actual> CDT : uncaled : delta = <delta_actual>
Power-up	Menu	FP_A2D : cursor :a= <actual> b= <actual> FP_A2D : gnd = <actual> <> 5 FP_A2D : TIME OUT

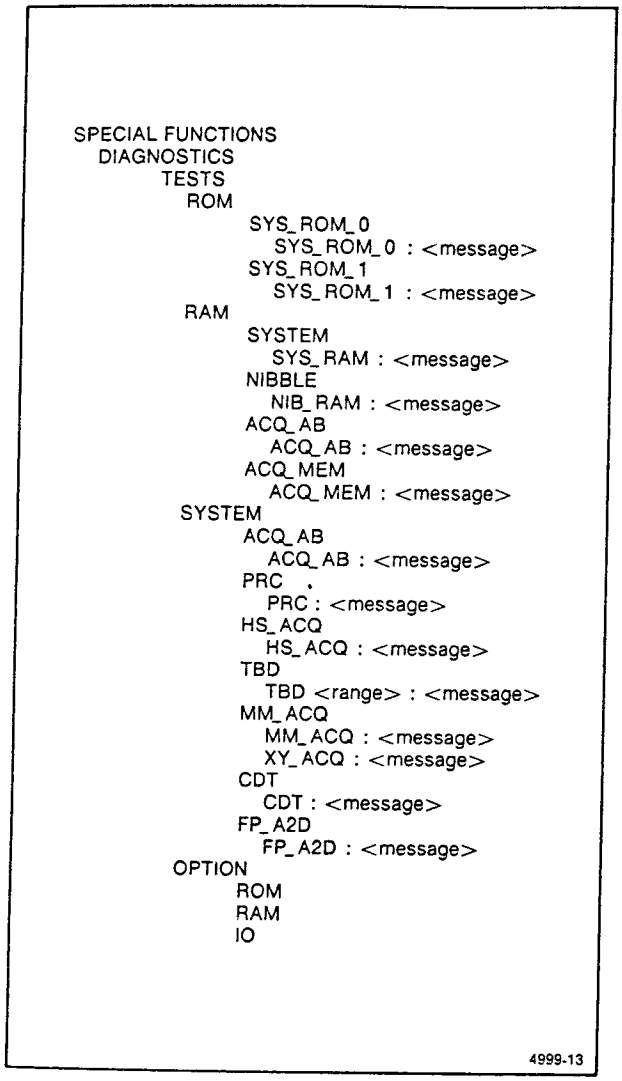


Figure 6-4. Diagnostic Menu.

Information in Table 6-12 is used to set up the acquisitions used in diagnostic tests. Start Address and Post Record Start data is valid just before ACQENA goes TRUE. Timebase Mode Register, Timebase Divider Register, and Acquisition Mode Register data is valid while ACQENA is TRUE, and causes the Timebase Divider to divide by the Real Divide Ratio. Record Length is the length of the record being acquired. RECCLK Period is the time that ACQENA is TRUE before ENDREC goes TRUE. Fill Test Start is the first value of the data being acquired. Fill Delta (B/CNT) is the increment used to select succeeding data points from the Diagnostic Generator. Effected Sweep Speed is the sweep speed used for the acquisition.

The following sequence of events occurs during power-up:

Set up temporary interrupt vectors (single task).

Do the power-up (PU) Kernel tests (each sets a bit in a q buffer).

ROM tests (Send error codes to U4113 and U4119 once for each detected error).

RAM tests (Send error codes to U4113 and U4119 once for each detected error).

Non maskable interrupt test (Send error codes to U4113 and U4119 once for each detected error).

Initialize system (two tasks: RAM refresh and diagnostics).

If the CURSORS SELECT C1/C2 button is pressed:

Enable extended error display.

Enable RS-232-C error reporting.

If a Menu/DISPLAY ON/OFF button is pressed:

Enable RS-232-C error reporting.

Do power-up calibration/diagnostic routines:

Rotate ones in control ports (OUT_PORTS).

Display the Box without maskable interrupt support (BOX).

Run Clock Delay Timer calibration routine (CAL_CLK_DLY).

Run Store/Nonstore Position Balance (CAL_V_POS).

Start building the power-up fault display.

Generate text about PU test results found in PU Q buffer.

Do System Diagnostic tests:

(when a failure is found, one line of text is generated for later display).

Maskable interrupt test (MI).

Acquisition memory address bus (ACQ mem access).

Acquisition memory (ACQ MEM).

Post record counter (PRC).

High speed acquisition (HS ACQ).

Time base divider (TBD).

Min/Max acquisition (MM ACQ).

X/Y acquisition (XY ACQ).

Clock delay timer (CDT).

Front panel A/D converter (FP A2D).

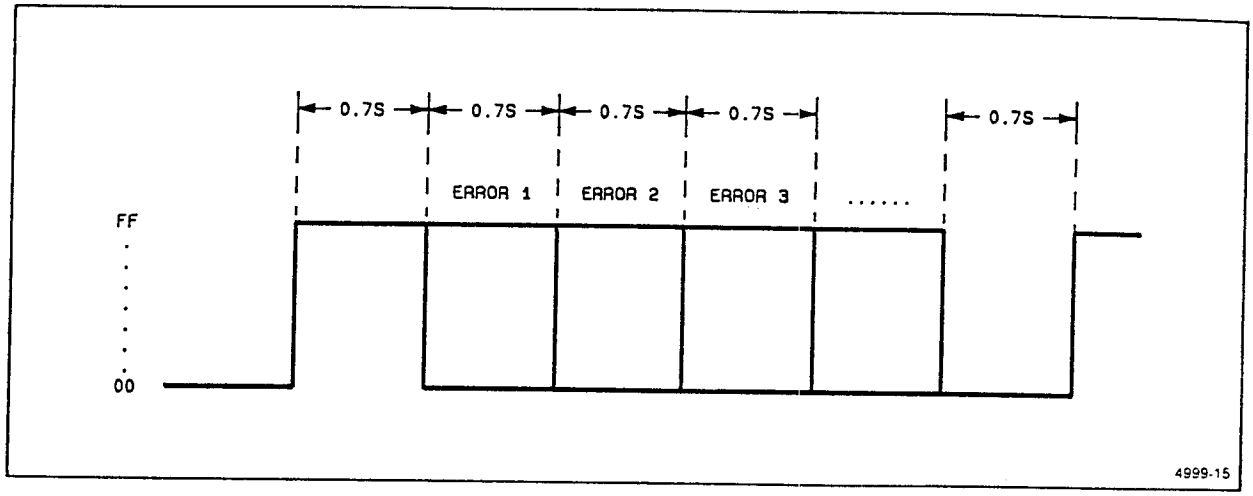


Figure 6-5. Error code timing (U4119).

Table 6-12

Diagnostic Acquisition Values

Test	TB MOD REG U41 19	TB DIV REG U41 13	ACQ MOD REG U33 10	Real DIV Ratio	REC LEN	Start ADDR	Post REC Start	Fill Text Start	RECCLK Period	Fill Delta (B/ CNT)	Effected SWP Speed
HS_ACQ	1E	00	85	1.	260.	0F9E	F4F	0FA0	50 ns	1.	5 μs
TBD											
hs/2	1A	00	85	2.	24.	0FFE	FDB	0000	100 ns	2.	10 μs
ps/2	15	FC	85	2.	24.	0FFE	FDB	0000	200 ns	2.	20 μs
ps/5	15	FB	85	5.	24.	0FFE	FDB	0000	500 ns	5.	50 μs
ps/10	15	F8	85	10.	24.	0FFE	FDB	0000	1 μs	10.	0.1 ms
/10	15	F5	85	10.	24.	0FFE	FDB	0000	1 σ	10.	0.2-1 ms
/100	15	ED	85	91.	24.	0FFE	FDB	0000	9.1 μs	91.	2-10 ms
/1k	15	DD	85	901.	24.	0FFE	FDB	0000	90.1 μs	133.	0.02-0.1 s
/10k	15	BD	85	9001.	8.	0FFE	FEB	0000	900.1 μs	41.	0.2-1 s
/100k	15	7D	85	90001.	8.	0FFE	FEB	0000	9000.1 μs	145.	2-5 s
MM_ACQ	16	E4	A5	200.	32.	0FFE	FD3	0000	100 ns	199. or 255.	
XY_ACQ	16	FC	8C	2.	16.	0FFE	FE3	0000	100 ns	1. or 3.	
CDT											
min	8E	00	8A	1.	4082.	0FFE	001	n/a	50 ns	n/a	
max	8F	00	9A	1.	4082.	0FFE	001	n/a	50 ns	n/a	

If there were power-up faults:

Display the power-up faults on U4119.

Display the power-up faults on the crt without maskable interrupt support:

Until a Menu button is changed.

Start normal instrument operation.

Diagnostic Tests

PU TEST. At power-up, this kernel test does a quick check of the instruments dynamic RAM (random access memory), ROM (read only memory), and NMI (non maskable interrupt) circuitry. If no errors are found, additional diagnostic tests are run.

If errors are found, their code is displayed (at power-up before NMI or MI go HI and before other tests are run) repeatedly, for approximately 2 sec, on U4113 and U4119 (see Table 6-13). The instrument also tries to display the errors on the crt as a four digit hexadecimal number:

PU : ROM/RAM/NMI : <hex_value>

For example: if ROM U9110, RAM U9232 and RAM U9231 fail, the instrument will:

1. Flash failure codes on U4113 and U4119:

PIN 12 . . . PIN 19
0100 0010
1000 0001
1010 0101

2. If possible, display error message on the crt (see Figure 6-6):

NOTE

More than one bad RAM usually means that something else is causing the problem.

MI. The maskable interrupt (MI) diagnostic creates and displays a single dark vector display (low resolution). Then a $\overline{\text{INT-RST}}$ (U9105 pin 11) is issued followed by a $\overline{\text{FRAME}}$ (U9105 pin 10). The MI (INTR at U9111 pin 18) should then go TRUE until another $\overline{\text{INT-RST}}$ is generated. All other MI sources are tested inherently by normal operation. The test sequence is:

Microprocessor (CPU) : pulse INT-RST LO (U9105 pin 11, U9208 pin 10)

DSP : set INTR (U9208 pin 6) FALSE

CPU : check MI by enabling MIs (U9136 pin 8)

Generate fault message.

Pulse FRAME LO (U9105.10, U9208.7)

Enable MIs

DSP : set INTR (U9208 pin 8) TRUE

CPU : if time is too great

Generate fault messages

Disable MIs

CPU : pulse INT-RST LO (U9105 pin 11, U9208 pin 10)

DSP : set INTR (U9208 pin 6) FALSE

CPU : check MI by enabling MIs (U9103G pin 8)

Generate fault messages

A fault generates one or more of the following error messages:

MI : line stuck high

MI : Display controller : TIMEOUT

MI : Display controller : unable to reset mi

SYS_ROM_n. SYS_ROM_n checks each ROM by calculating and then comparing its checksum to what is stored in the ROM.

If an error is found, the calculated value and the value expected are displayed on the crt:

SYS_ROM_n : calculated_value <> expected_value

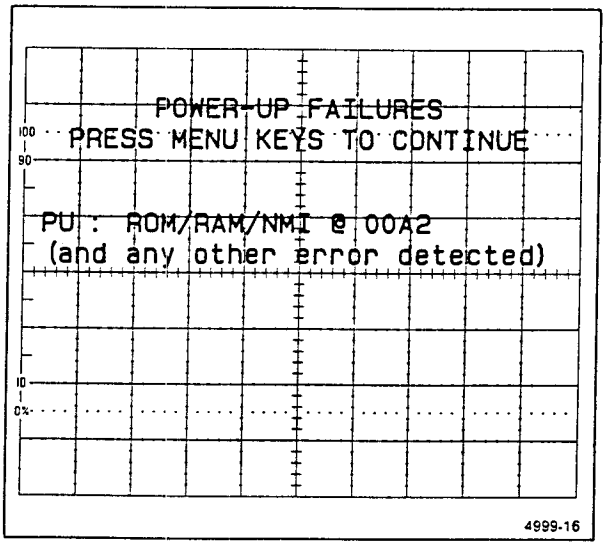


Figure 6-6. PU error display.

Table 6-13

PU TEST Failure Codes

Failed Part	U4113 and U4119 Code				Crt Failure Code
	Pins 12 19	Pins 13 18	Pins 14 17	Pins 15 16	In Binary (from pu q)
ROM					
U9109 (E0000)	0	0	1	0	xxxx xxxx xxxx xxx1
U9110 (E8000)	0	1	0	0	xxxx xxxx xxxx xx1x
RAM					
U9203	0	1	0	1	xxxx xxxx xxxx x1xx
U9202	0	1	1	0	xxxx xxxx xxxx 1xxx
U9233	0	1	1	1	xxxx xxxx xxx1 xxxx
U9232	1	0	0	0	xxxx xxxx xx1x xxxx
U9201	1	0	0	1	xxxx xxxx x1xx xxxx
U9231	1	0	1	0	xxxx xxxx 1xxx xxxx
NMI	1	0	1	1	xxxx xxx1 xxxx xxxx

For example, if the calculated value is A4D2 and the value stored in the ROM is 23DA the following error message is displayed on the crt:

SYS_ROM_1 : A4D2 <> 23DA

SYS_RAM. This test checks the system RAM. The test writes a 0xAA55 into 100 bytes of display memory. It then checks the data to make sure that the data has not changed. The test is then repeated using 0x55AA.

NOTE

Firmware version 01 only displays the address of the bad RAM.

If an error is found, the address (greater than 0 but less than 8000) of the error, the actual data found at the address, and the data that was expected at that address are displayed on the crt:

SYS_RAM : @ <address> <actual data> <> <expected data>

For example, if the address of the bad cell is 0x4000, the data found at that address is 0x0F, and the expected data for that address is 0x4F the following error message is displayed on the crt:

SYS_RAM : @ 4000 0F <> 4F

NIB_RAM. This test checks the nibble RAM. The test procedure and the error message format are the same as for SYS_RAM.

ACQ_AB. This test checks the address bus of the acquisition memory. Twenty one unique patterns are written into the address counters (U3423 U3424 and U3425) and read back through the acquisition address buffers (U3427 U3428).

NOTE

At power-up this test and all others are transient and not active at the time of the power-up failure messages.

Push the SELECT C1/C2 switch to stop pattern changes. The test loops using the pattern for the first error found. All patterns used are shown in Table 6-14.

If an error is found, the value read back and the value expected are displayed on the crt:

ACQ_AB : read-back <actual> <> <expected>

Table 6-14

Acquisition Address Bus Test Patterns

Binary A12 A1	Hexadecimal A1
0000 0000 0010	002
0000 0000 0110	006
0000 0000 1110	00E
0000 0001 1110	01E
0000 0011 1110	03E
0000 0111 1110	07E
0000 1111 1110	0FE
0001 1111 1110	1FE
0011 1111 1110	3FE
0111 1111 1110	7FE
1111 1111 1110	FFE
1111 1111 1100	FFC
1111 1111 1000	FF8
1111 1111 0000	FF0
1111 1110 0000	FE0
1111 1100 0000	FC0
1111 1000 0000	F80
1111 0000 0000	F00
1110 0000 0000	E00
1100 0000 0000	C00
1000 0000 0000	800

For example, if the value read back is 008 and the value expected is 00F the following error message is displayed on the crt:

ACQ_AB : read-back 008 <> 00F

NOTE

The outputs of the Record Counters should be about 50% duty cycle square waves of 1.1 seconds duration.

If the oscilloscope is operating in extended diagnostics mode, the error display is expanded to include all errors, not just the first error. Also, in extended diagnostics mode the RS-232-C Option can be used to send the error reports to a terminal or computer. This enables analysis of the data for pattern recognition. For example, if bit 5 (U3424 pin 15) is shorted to ground all patterns where bit 5 should be a one will have a zero in bit position 5 and therefore fail.

ACQ_MEM. This test checks the acquisition memory and it's microprocessor interface.

NOTE

Software version 01 always claims address 0 is bad no matter what errors are actually found.

Firmware version 01 fills the acquisition memory with a ramp and then checks to see if the values are correct. The value at each physical_address is the (physical_address-0x48000) mod 256. Firmware version 02 fills the acquisition memory with a checkerboard pattern of AA55 and 55AA and checks to see if the values are correct.

The microprocessor can not reliably write to acquisition memory without clobbering the adjacent byte (the microprocessor has byte wide memory). Each acquisition-memory device is tested separately (U3418 first and then U3419. An error message identifying a faulty address implies the faulty device via its address. An even address value implies that RAM (U3418) or transceiver (U3421) may be faulty. An odd address implies U3419 or U3422.

NOTE

Firmware version 01 only displays the address of an error.

If an error is found the address of the error, the actual data found at the address, and the data expected at the address are displayed on the crt:

ACQ_MEM : odd @ <address> <actual data> <> <expected data>

ACQ_MEM : even @ <address> <actual data> <> <expected data>

NOTE

The displayed address is offset from 0x40000 (acq_mem_block) and is a 4 digit hexadecimal number between 0 and 4096.

For example, if the address of an error is 48008, the actual data found at the address is F0, and the expected

data at that address is F4, the following error message is displayed on the crt:

ACQ_MEM : even @ 4008 F0 <> F4

PRC. This test checks the Post Record Counter write and the B-TRIG read circuitry. Twenty four unique patterns are written into the Post Record Counter (U4115 U4116 and U4117) and read through the B Delay Timer (U4123 U4124).

The B Delay Timer is clocked by a write to the Time Base Divider register (U4114 pin 8 through U4107 pin 4), the inactive B-GATE (U4121B pin 11), and the TRGD (U4121B pin 13) signals.

Push the SELECT C1/C2 switch to stop pattern changes. The test loops using the pattern for the first error found. All patterns used are shown in Table 6-15.

NOTE

If rec-clk is active unpredictable results occur.

If an error is found, the value read back and the value expected are displayed on the crt:

PRC : read-back <actual> <> <expected>

For example, if the value read back is 008 and the value expected is 00F the following error message is displayed on the crt:

PRC : read-back 008 <> 00f

If the oscilloscope is operating in extended diagnostics mode, the error display is expanded to include all errors, not just the first error. Also, in extended diagnostics mode the RS-232-C Option can be used to send the error reports to a terminal or computer. This enables analysis of the data for pattern recognition. For example, if bit 5 (U4116 pin 15) is shorted to ground all patterns where bit 5 should be a one will have a zero in bit position 5 and therefore fail.

HS_ACQ. This test checks the High Speed Acquisition using a 260 byte acquisition at the fastest record speed (record clock = convert clock = 20 MHz = 50 ns per byte) sampling the Diagnostic Code generators.

Table 6-15

PRC Test Patterns

Binary A11 A0	Hexadecimal A0
0000 0000 0001	001
0000 0000 0011	003
0000 0000 0111	007
0000 0000 1111	00F
0000 0001 1111	01F
0000 0011 1111	03F
0000 0111 1111	07F
0000 1111 1111	0FF
0001 1111 1111	1FF
0011 1111 1111	3FF
0111 1111 1111	7FF
1111 1111 1111	FFF
1111 1111 1110	FFE
1111 1111 1100	FFC
1111 1111 1000	FF8
1111 1111 0000	FF0
1111 1110 0000	FE0
1111 1100 0000	FC0
1111 1000 0000	F80
1111 0000 0000	F00
1110 0000 0000	E00
1100 0000 0000	C00
1000 0000 0000	800
0000 0000 0000	000

NOTE

This is the only test which absolutely origins the fill; others only test the slope of the fill.

Synchronous to NMI the Acquisition Address Counter (U3423, U3424, and U3425) is loaded with 0x1000 – 0x96 (0x0F6A) and the Post Record Counter (U4115, U4116,

and U4117) is loaded with 0xFF1 − 240 + 0x96 (0xF9F). The Time Base Divisor Register (U4113) is set to 0x00, the Acquisition Mode Register (U3310) is set to 0x85 and the Time Base Mode Register (U4119) is set to 0x1E. See Table 6-12 for more acquisition data.

To start the acquisition a 0x10 is ORed into the Time Base Mode Register (U4119), generating ACQENA TRUE synchronous to CONV CLK. Two activities are then done at the same time:

1. The microprocessor polls the Memory Address Buffer bit 16 (U3428 pin 9) $\overline{\text{ENDREC}}$ 4000 times before aborting the second activity.

2. The acquisition runs asynchronous to the microprocessor.

CONV clock propagates through U4103B, U4125A, and U4125B becoming SAVECLK. CONV and SAVECLK propagate through U4104B, U3101A, U3105B, U3105A (becoming ACQWRITE), and U3417 to clock the data from the swap (Acquisition Buffer Sequencer) registers (U3236 and U3239) into the Acquisition Memory (U3418 and U3419) in 16-bit chunks. The signals from U3417 also clock the acquisition Address Counters (U3423, U3424, and U3425).

The microprocessor sets $\overline{\text{TEST}}$ FALSE (U3310) disabling the DATA IN BUFFER (U3229). A LO $\overline{\text{TEST}}$ causes the output of the DIAGNOSTIC CODE GENERATORS (U3230 and U3231) to be used instead of the A/D CONVERTER data.

The microprocessor uses the ACQUISITION MODE REGISTER (U3310) to tie MAXCLK and MINCLK (U3309 pin 7 and U3309 pin 9) to $\overline{\text{EVENCLK}}$ and $\overline{\text{ODDCLK}}$ (U3101B pin 8 and U3103B pin 8) respectively through U3309. $\overline{\text{ODDCLK}}$ and $\overline{\text{EVENCLK}}$ are 50% duty cycle complements of each other and have a period of two CONV clocks. This means that the MIN REGISTER is latched with a test value and 50 ns later the MAX REGISTER is latched with a value one greater. After another 25 ns the swap (Acquisition Buffer/Sequencer) registers (U3236, U3237, U3238, and U3239) latch a 16-bit word comprised of the output of the MIN REGISTER and the MAX REGISTER.

When the Acquisition Address Counter overflows PREFULL (U3425 pin 7) goes HI. This in turn makes STO RDY (U4226A pin 5) HI. CALTIMER (from U3310 pin 12) makes multiplexer U4227 select STO RDY and pass it through to U4227 pin 7. Convert clock $\overline{\text{CONV}}$ then passes the signal through U4228A, U4127C, and U4226B making TRIGD (U4226B pin 9) HI. TRIGD enables the Post Record Counter to count at RECCLK (CONV clock) rates.

One RECCLK after the Post Record Counter reaches a hexadecimal count of FF0, U4105B creates $\overline{\text{ENDREC}}$ (not end of record) LO. When the microprocessor finds $\overline{\text{ENDREC}}$ LO, the values in the Acquisition Memory Address Counters (U3423, U3424, and U3425) and the Post Record Counter (U4115, U4116, and U4117) are analyzed. Then the Acquisition Memory is checked to see if it contains the proper values.

If an error is found, one of the following messages is displayed on the crt:

HS_ACQ : latent END_OF_RECORD

HS_ACQ : acq_mem cntr <mem_actual> ' <> <mem_expected>

HS_ACQ : prc <prc_actual> <> <prc_expected>

HS_ACQ : fill @ <fill_address> : <fill_actual> <> <fill_expected>

Where:

Latent END_OF_RECORD means the microprocessor polled for an $\overline{\text{ENDREC}}$ 4000 times and never saw one.

Acq_mem cntr means the completion value of the Acquisition Memory Counter was not what was expected (see Table 6-12).

Prc means the completion value of the Post Record Counter was not what was expected (see Table 6-12).

Fill means the fill value at the indicated address was not what was expected (see Table 6-12).

Prc_actual, prc_expected, mem_actual and mem_expected are all 3 digit hexadecimal numbers.

Fill_address is a 4 digit hexadecimal number representing an offset from 0x48000 (start of Acquisition Memory).

Fill_actual and fill_expected are each 2 digit hexadecimal numbers.

TBD. This test checks the Time Base Divider string using nine different Time Base Divider test ranges (rng).

An acquisition is run as in HS_ACQ except that U4103B selects an input that makes RECCLK a submultiple of CONV clock. As in HS_ACQ, $\overline{\text{ENDREC}}$ is polled and the Post Record Counter and Acquisition Memory completion values are checked. Although the acquisition is similar to the HS ACQ acquisition, the fill is different (see Table 6-12).

NOTE

See Table 6-12, (Diagnostic Acquisition Values) for specific signals, register values, and terms used in the following discussion.

If the SELECT C1/C2 button is held in while the test is running, the test loops on the first error. If an error is detected, one of the following messages is displayed on the crt:

TBD <rng> : <error>

Where:

Rng is one of the following:

hs/2
ps/2
ps/5
ps/10
/10
/100
/1k
/10k
/100k

Error is one of the following:

latent END_OF_RECORD

prc <prc_actual> <> <prc_expected>

acq_mem cntr <mem_actual> <> <mem_expected>

fill @ <address> : <fill_actual> <> <fill_expected>

MM_ACQ. This test checks the acquisition circuitry as it relates to MIN/MAX.

NOTE

This test also runs the XY_ACQ test.

RECCLK is set using the Time Base Divider to 1/200th of the CONV clock. Then an acquisition is performed as in HS ACQ, $\overline{\text{ENDREC}}$ is polled, and the Post Record Counter and Acquisition Memory Counter completion values are checked.

Fill testing starts at acq_mem address 0000. The fill is tested for max (odd) byte minus min (even) byte to give either 255 or 200.

NOTE

The error message values are as in HS_ACQ except for the fill values.

If an error is found, one of the following messages is displayed on the crt:

MM_ACQ : latent END_OF_RECORD

MM_ACQ : prc <prc_actual> <> <prc_expected>

MM_ACQ : acq_mem cntr <acq_mem_actual> <> <acq_mem_expected>

MM_ACQ : fill @ <fill_address> : <fill_actual> <> <fill_expected>

XY_ACQ. This test checks the acquisition circuitry as it relates to X-Y.

NOTE

This test has no menu entry, however it is run by MM_ACQ.

As in HS_ACQ, an acquisition is performed, $\overline{\text{ENDREC}}$ is polled, and the Post Record Counter and Acquisition Memory Counter completion values are checked. The fill is tested for n, n+1, n+4,n+5, n+8, n+9, ... starting at Acquisition Memory address 0000.

NOTE

The test and the error message values are as in HS_ACQ except for the fill values.

If an error is found, one of the following messages is displayed on the crt:

XY_ACQ : latent END_OF_RECORD

XY_ACQ : prc <prc_actual> <> <prc_expected>

XY_ACQ : acq_mem cntr <acq_mem_actual> <> <acq_mem_expected>

XY_ACQ : fill @ <fill_address> : <fill_actual> <> <fill_expected>

CDT. This test checks the Clock Delay Timer. The CDT (clock delay timer) is a dual-slope integrator used to

measure the time between an asynchronous trigger (either the A or the B Gate) and the acquisition systems master clock. The timer divides the 50 ns convert clock (CONV) into 200 time periods.

The CDT diagnostic checks the Clock Delay Timer circuit using two self-triggered acquisitions. Each test acquisition is started when the microprocessor sets CAL-TIMER (U4247 pin 2) TRUE and $\overline{\text{TEST}}$ (U4228 pin 10) is set first LO and then HI. When PREFULL (U4228 pin 2) goes HI, U4127 pin 4 goes TRUE causing the charge cycle of the CDT (C4201) to start. The discharge cycle begins 100 to 150 ns later when TRGD goes TRUE forward biasing Q4203.

The time that the voltage on C4201 is above the voltage at U4229 pin 2 (set by R4214, R4215 and R4216) during the discharge cycle is proportional to the time difference between U4127 pin 4 going HI and TRGD (U4226 pin 9) going TRUE. This time is counted by U4230 (at the CONV clock rate) and U4231B. The MSB of the CDT word (bit 8) is shared with BYTEINT (the hardware flag signifying that a byte interrupt has occurred). This shared bit is read by the microprocessor through U3428 pin 8.

If an error is found, one of the following messages is displayed on the crt:

CDT : TIME-OUT <tb_mode_reg_pattern>

CDT : PRE-DETRIG <tb_mode_reg_pattern>

CDT : uncaled : min = <min_actual>

CDT : uncaled : delta = <delta_actual>

Where:

TIME-OUT is caused by not receiving a $\overline{\text{ENDREC}}$.

Tb_mode_reg_pattern is a 2-digit hexadecimal value indicating the pattern used in the Time Base Mode Register during the test acquisition.

PRE-DETRIG is caused by the CDT counter overflowing (CNTCLR U4231 pin 6).

Tb_mode_reg_pattern is a 2-digit hexadecimal value indicating the pattern used in the Time Base Mode Register during the test acquisition.

Min_actual is the value (85.0 to 115.0) read from U4230 + CDT msb (U3428 pin 8) during a test acquisition with $\overline{\text{TEST}}$ LO.

Delta_actual is the value (200 to 210) read from U4230 + CDT msb (U3428 pin 8) during a test acquisition with $\overline{\text{TEST}}$ HI minus the value of the previous min cycle.

FP_A2D. This test checks the front panel A/D converter circuitry. A conversion is done on three of the analog inputs (A CURS, U6106 pin 12, B CURS, U6106 pin 13, and ground, U6108 pin 5). The algebraic sum of A CURS and B CURS are checked. Their sum should be between 0x100 and 0x700. Ground is also checked. It should be between 0 and 5 front panel A/D converter counts (5 ÷ 1024 of VREF).

During power-up this test defines a variable (FP_POLLED) that controls how the microprocessor works with the front panel. If during testing a MI is not generated, it is assumed that the front panel will never generate a MI and the microprocessor must poll the front panel to see when to transfer front-panel data.

If an error is found one of the following messages is displayed on the crt:

NOTE

In firmware version 02, the Gnd message should be FP_A2D : gnd = <actual> > 5 (greater than only)

FP_A2D : cursor :a= <actual> & b= <actual>

FP_A2D : gnd = <actual> <> 5

FP_A2D : TIME-OUT

Where:

Actual is a 3-digit hexadecimal number representing the result of a front-panel digitization.

TIME-OUT indicates A/D INT FLAG (U6101D pin 13) did not occur within 0x800 polls by the microprocessor.

CAL_AIDS. The instrument calibration aids are used to help calibrate the instrument.

CAL_V_POS. This calibration aid is used to calibrate the storage position control (see "Adjustment Procedure").

CAL_CLK_DLY. Clock Delay Timer (CDT) calibration uses a graphic display. The horizontal position of the display cross hairs is attached to the min count and the vertical position is attached to the delta count (see "Adjustment Procedure").

NOTE

Only BOX and OUT_PORTS is run by version 01 software.

CAL_PU. Depressing one of the Menu Select/DISPLAY ON/OFF controls during power-up runs four calibration routines, BOX, OUT_PORTS, CAL_CLK_DLY, and the Storage Acquisition Offset. Each routine is run until one of the menu buttons is again pushed. The BOX and OUT-PORTS routines are run at the same time. Each routine is used to adjust the instrument (see "Adjustment Procedure") except for OUT_PORTS. OUT_PORTS is used to check instrument circuitry (see OUT_PORTS).

Exercisers

Instrument exercisers are used to aid in the repair of the instrument.

CONFIGURATION. This exerciser lists the ROM part numbers used in the instrument and the options installed in the instrument.

BOX. This exerciser displays a box (rectangle) on the crt. Two places in the Menu generate the Box. Gains and offsets of the storage display system integrators are set using the Box display (see the "Adjustment Procedure"). The Display Controller (U9208) is synchronously stimulated (at a multiple cf NMI) to display the box not using MIs.

CIRCLE. A high resolution circle is displayed on the crt by this exerciser. This is the only diagnostic that uses all 10 bits of the display DACs (U9210 and U9220).

FP_VALUES. Raw internal front-panel data is displayed on the crt by this exerciser. Table 6-16 shows the display format, and Table 6-17 shows the bit definitions for the display.

NOTE

Digital data is intensified when a control is changed. All other data is intensified if the data has changed more than 5 counts since the last display update.

Table 6-16

Display Format

Data	Signal Names			
Digital	AD DATA (R6101)	ISTAT (U6103)	SWB1 (U9302)	SWB2 (U9301)
Cursors	A CURSOR	B CURSOR	B DELAY	
CH 1	E114 E115	CH1 ATT	CH1 STAT	CH1 PROBE
CH 2	E164 E165	CH2 ATT	CH2 STAT	CH2 PROBE
A Sweep	ARES1	ARES2		
B Sweep	B RES	B CAPS		
Ground	GROUND			

Table 6-17

Display Format Bit Definitions

Signal Names	Displayed Bit Positions							
	8	7	6	5	4	3	2	1
AD DATA			CH2 INV	T MAG	PP	$\overline{\text{TRL}}$	SS RST	$\overline{\text{XY}}$
ISTAT	$\overline{\text{VALT}}$	SGL SWP	AC1	AC2	$\overline{\text{CH1 SEL}}$	$\overline{\text{CH2 SEL}}$	$\overline{\text{CHOP}}$	A/D INT FLAG
SWB1	STORE ON	$\overline{\text{B ONLY}}$	HOLD	ROLL	HOR MAG	HOR CAL	PRE/POST	$\overline{\text{A ONLY}}$
SWB2	SELECT C1/C2	MENU ADV	MEM 2	MENU	1K/4K	POS/SEL	MEM 1	MEM 3

OUT_PORTS. All microprocessor output ports of the instrument are exercised by this exerciser. If entered from the menu, rotating the cursor knob selects either a single port or all ports at once. If entered from power-up, the exerciser is run with the box display. Test patterns used in each port are shown in Table 6-18 through Table 6-22.

NOTE

The ones and zeros patterns are observed using an LED dip clip on the registers. The pattern seen on Address Counters U3423, U3424, and U3425 (U3427 and U3428) will occasionally have other data superimposed upon it.

Table 6-18

ACQ_MEM 0x48000

U3427 Pins 2 3 4 5 6 7 8 9	U3428 Pins 2 3 4 5 6 7 8 9
0 0 0 x 0 0 0 0	0 0 0 0 x x x x
0 0 1 x 0 0 0 0	0 0 0 0 x x x x
0 1 0 x 0 0 0 0	0 0 0 0 x x x x
1 0 0 x 0 0 0 0	0 0 0 0 x x x x
0 0 0 x 1 0 0 0	0 0 0 0 x x x x
0 0 0 x 0 1 0 0	0 0 0 0 x x x x
0 0 0 x 0 0 1 0	0 0 0 0 x x x x
0 0 0 x 0 0 0 1	0 0 0 0 x x x x
0 0 0 x 0 0 0 0	1 0 0 0 x x x x
0 0 0 x 0 0 0 0	0 1 0 0 x x x x
0 0 0 x 0 0 0 0	0 0 1 0 x x x x
0 0 0 x 0 0 0 0	0 0 0 1 x x x x
0 0 0 x 0 0 0 0	0 0 0 0 x x x x
0 0 1 x 0 0 0 0	0 0 0 0 x x x x

Table 6-19

ACQ_MODE 0x437BE

U3310 Pins							
2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
0	1	0	0	0	0	1	0
0	0	1	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1

Table 6-20

TB_MODE 0x407DE

U4119 Pins							
2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	1	0	0	0	0	1	0
1	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0

Table 6-21

TB_SWP_RATE 0x407EE

U4113 Pins							
2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	1	1	1	0	0
0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0

Table 6-22

FP_A/D_CTL 0x437F6

U6104 Pins							
2	3	4	5	6	7	8	9
1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1
1	1	0	0	1	1	1	1
1	1	0	0	0	1	1	1
1	1	0	0	0	0	1	1
1	1	0	0	0	0	0	1
1	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1

INPUT_PORTS. This exerciser displays the input data for all microprocessor input ports. An explanation of the displayed data is shown in Table 6-23.

A_TO_D_TESTS/SAMPLES. This exerciser sets the number of acquisitions used to test the A/D Converter.

Turn the CURSORS control to select the number of 4096 byte acquisitions (a power of 2 is best) used to test the A/D Converter (see LINEARITY exerciser).

A_TO_D_TESTS/LINEARITY. This exerciser tests the acquisition A/D converter for missing bits.

Inject a highly linear 11 division vertically centered, (2 × 4096 × 50) ns duration triangle wave signal into the CH 1 or X input. Set the trigger so that the oscilloscope triggers close to the negative peak.

If any codes are missing in samples × 4096 acquisitions a message indicating that there were missing codes is displayed (and sent to the communications option if operating in extended diagnostics).

Setting the trigger point close to the positive peak tests negative going conversions.

The display is a histogram with a vertical scale of 5 × samples × (codes converted) per division and a horizontal scale of 0 to 255 codes across 10 divisions left to right (25.5 codes per division).

COM_OPTION/DEBUG. This exerciser is used in debuging the communications option. Debug outputs a test message and displays any incoming messages (data) on the crt.

PICTURES. The picture exercisers use line drawings to exercise the instruments display system. The Tekbug is a line drawing of the Tektronix symbol. The Wizard is a multi function display. The gain of the display controller is controlled by the CURSORS control. The position of the display is controlled by the CH 1 and CH 2 POSITION controls. If the VERTICAL POSITION and CURSORS controls are not turned for about 5 seconds, the display is automatically moved through its gain (CURSORS) and POSITION ranges.

Table 6-23

Display Format Digit Definitions

Input Port Name	U Number	Crt Name	Number of Bits Displayed
Acquisition Address Buffer	U3427 and U3428	ACQ_ADDR_BUF	16
Clock Delay Register	U4230	CLK_DELAY_REG	8
B Delay Timer	U4123 and U4124	B_DELAY_TIMER	12
Front Panel Instrument Status	U6103	FP_INSTAT	8
Front Panel Address Data	U6102	FP_AD_DATA	8

CORRECTIVE MAINTENANCE

INTRODUCTION

Corrective maintenance consists of component replacement and instrument repair. This part of the manual describes special techniques and procedures required to replace components in this instrument. If it is necessary to ship your instrument to a Tektronix Service Center for repair or service, refer to the "Repackaging" information in Section 2 of this manual.

MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions.

1. Disconnect the instrument from the ac-power source before removing or installing components.

2. Verify that the line-rectifier filter capacitors are discharged prior to performing any servicing.

3. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).

4. When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components can usually be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., please check the "Replaceable Electrical Parts" list for the proper value, rating, tolerance, and description.

NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special Parts

In addition to the standard electronic components, some special parts are used in the instrument. These components are manufactured or selected by Tektronix, Inc. to meet specific performance requirements, or are manufactured for Tektronix, Inc. in accordance with our specifications. The various manufacturers can be identified by referring to the "Cross Index-Manufacturer's Code number to Manufacturer" at the beginning of the "Replaceable Electrical Parts" list. Most of the mechanical parts used in this instrument were manufactured by Tektronix, Inc. Order all special parts directly from your local Tektronix Field Office or representative.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., be sure to include all of the following information:

1. Instrument type (include all modification and option numbers).

2. Instrument serial number.

3. A description of the part (if electrical, include its full circuit component number).

4. Tektronix part number.

Selectable Components

Several components in the instrument are selectable to obtain optimum circuit operation. Value selection of these components is done during the initial factory adjustment procedure. Usually, further selection is not necessary for subsequent adjustments unless a component has been changed that affects circuitry for which a selected component has been specifically chosen.

MAINTENANCE AIDS

The maintenance aids listed in Table 6-24 include items required for performing most of the maintenance procedures in this instrument. Equivalent products may be substituted for those given, provided their characteristics are similar.

Table 6-24
Maintenance Aids

Description	Specification	Usage	Example
1. Soldering Iron	15 to 25 W.	General soldering and unsoldering.	Antex Precision Model C.
2. Torx Screwdriver Tips and Handle	Torx tips: #T7, #T9, #T10, #T15, and #T20. Handle: 1/4 inch hex drive.	Assembly and disassembly.	Tektronix Part Numbers: #T7 003-1293-00 #T9 003-0965-00 #T10 003-0814-00 #T15 003-0966-00 #T20 003-0866-00. Handles: 8 1/2 in. 003-0293-00 3 1/2 in. 003-0445-00.
3. Nutdrivers	1/4 inch, 5/16 inch, 1/2 inch, and 9/16 inch.	Assembly and disassembly.	Xcelite #8, #10, #16, and #18.
4. Open-end Wrench	9/16 inch and 1/2 inch.	Channel Input and Ext Trig BNC Connectors.	Tektronix Part Numbers: 9/16 003-0502-00 1/2 003-0822-00.
5. Hex Wrenches	0.050 inch, 1/16 inch.	Assembly and disassembly.	Allen Wrenches.
6. Long-nose Pliers		Component removal and replacement.	Diamalloy Model LN55-3.
7. Diagonal Cutters		Component removal and replacement.	Diamalloy Model M554-3.
8. Vacuum Solder Extractor	No static charge retention.	Unsoldering static sensitive devices and components on multilayer boards.	Pace Model PC-10.
9. Contact Cleaner	No-Noise R.	Switch and pot cleaning.	Tektronix Part Number 006-0442-02.
10. Pin-Replacement Kit		Replace circuit board connector pins.	Tektronix Part Number 040-0542-01.
11. IC-Removal Tool		Removing DIP IC packages.	Augat T114-1.
12. Isopropyl Alcohol	Reagent grade.	Cleaning attenuator and front panel assemblies.	2-Isopropanol.
13. Isolation Transformer		Isolate the instrument from the ac power source for safety.	Tektronix Part Number 006-5953-00.
14. 1X Probe		Power supply ripple check.	TEKTRONIX P6101A.
15. Bayonet Ground Assembly		Signal interconnect for power supply ripple check.	Tektronix Part Number 013-0085-00.
16. LED Dip Clip		Troubleshooting.	HP 548A.

INTERCONNECTIONS

Interconnections in this instrument are made with pins soldered onto the circuit boards. Several types of mating connectors are used for the interconnecting pins. The following information provides the replacement procedures for the various type connectors.

End-Lead Pin Connectors

Pin connectors used to connect the wires to the interconnect pins are factory assembled. They consist of machine-inserted pin connectors mounted in plastic holders. If the connectors are faulty, the entire wire assembly should be replaced.

Multipin Connectors

When pin connectors are grouped together and mounted in a plastic holder, they are removed, reinstalled, or replaced as a unit. If any individual wire or connector in the assembly is faulty, the entire cable assembly should be replaced. To provide correct orientation of a multipin connector, an index arrow is stamped on the circuit board, and either a matching arrow is molded into or the numeral 1 is marked on the plastic housing as a matching index. Be sure these index marks are aligned with each other when the multipin connector is reinstalled (see Figure 6-1).

TRANSISTORS AND INTEGRATED CIRCUITS

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets or unsoldered from the circuit board during routine maintenance, return them to their original board locations. Unnecessary replacement or transposing of semiconductor devices may affect the adjustment of the instrument. When a semiconductor is replaced, check the performance of any circuit that may be affected.

Any replacement component should be of the original type or a direct replacement. Bend transistor leads to fit their circuit board holes, and cut the leads to the same length as the original component. See Figure 9-2 in the "Diagrams" section for lead-configuration illustrations.

The chassis-mounted power supply transistor is insulated from the chassis by a heat-transferring mounting block. Reinstall the mounting block and bushings when replacing these transistors. Use a thin layer of heat-transferring compound between the insulating block and chassis when reinstalling the block.

NOTE

After replacing a power transistor, check that the collector is not shorted to the chassis before applying power to the instrument.

To remove socketed dual-in-line packaged (DIP) integrated circuits, pull slowly and evenly on both ends of the device. Avoid disengaging one end of the integrated circuit from the socket before the other, since this may damage the pins.

To remove a soldered DIP IC when it is going to be replaced, clip all the leads of the device and remove the leads from the circuit board one at a time. If the device must be removed intact for possible reinstallation, do not heat adjacent conductors consecutively. Apply heat to pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

SOLDERING TECHNIQUES

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used to remove or replace parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument.

WARNING

To avoid an electric-shock hazard, observe the following precautions before attempting any soldering: turn the instrument off, disconnect it from the ac power source, and wait at least three minutes for the line-rectifier filter capacitors to discharge.

Use rosin-core wire solder containing 63% tin and 37% lead. Contact your local Tektronix Field Office or representative to obtain the names of approved solder types.

When soldering on circuits boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron may cause etched circuit conductors to separate from the board base material and melt the insulation on small wires. Always keep the soldering-iron tip properly tinned to ensure best heat transfer from the iron tip to the solder joint. Apply only enough solder to make a firm joint. After soldering, clean the area around the solder connection with an approved flux-removing solvent (such as isopropyl alcohol) and allow it to air dry.

Circuit boards in this instrument may have many conductive layers. Conductive paths between the top and bottom board layers may connect to one or more inner layers. If any inner-layer conductive path becomes broken due to poor soldering practices, the board becomes unusable and must be replaced, Damage of this nature can void the instrument warranty.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment should attempt repair of any circuit board in this instrument.

Desoldering parts from multilayer circuit boards is especially critical. Many integrated circuits are static sensitive and may be damaged by solder extractors that generate static charges. Perform work involving static-sensitive devices only at a static-free work station while wearing a grounded antistatic wrist strap. Use only an antistatic vacuum-type solder extractor approved by a Tektronix Service Center.

CAUTION

Attempts to unsolder, remove, and resolder leads from the component side of a circuit board may cause damage to the reverse side of the circuit board. The following techniques should be used to replace a component on a circuit board:

1. Touch the vacuum desoldering tool to the lead at the solder connection. Never place the iron directly on the board; doing so may damage the board.

NOTE

Some components are difficult to remove from the circuit board due to a bend placed in the component leads during machine insertion. To make removal of machine-inserted components easier, straighten the component leads on the reverse side of the circuit board.

2. When removing a multipin component, especially an IC, do not heat adjacent pins consecutively. Apply heat to the pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

CAUTION

Excessive heat can cause the etched circuit conductors to separate from the circuit board. Never allow the solder extractor tip to remain at one place on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for desoldering multipin components) must not be used. Damage caused by poor soldering techniques can void the instrument warranty.

3. Bend the leads of the replacement component to fit the holes in the circuit board. If the component is replaced while the board is installed in the instrument, cut the leads so they protrude only a small amount through the reverse side of the circuit board. Excess lead length may cause shorting to other conductive parts.

4. Insert the leads into the holes of the board so that the replacement component is positioned the same as the original component. Most components should be firmly seated against the circuit board.

5. Touch the soldering iron to the connection and apply enough solder to make a firm solder joint. Do not move the component while the solder hardens.

6. Cut off any excess lead protruding through the circuit board (if not clipped to the correct length in step 3).

7. Clean the area around the solder connection with an approved flux-removing solvent. Be careful not to remove any of the printed information from the circuit board.

REMOVAL AND REPLACEMENT INSTRUCTIONS

The exploded view drawings in the "Replaceable Mechanical Parts" list (Section 9) may be helpful during the removal and reinstallation of individual subassemblies or components. Circuit board and component locations are shown in the "Diagrams" section.

Cabinet

WARNING

To avoid electric shock, disconnect the instrument from the ac-power-input source before removing or replacing any component or assembly.

To remove the instrument cabinet, perform the following steps:

NOTE

For instruments with a power-cord securing clamp; remove the Phillips-head screw holding the power-cord securing clamp before disconnecting the power cord.

1. Disconnect the power cord from the instrument.

2. Remove two screws, one each from the right-rear side and bottom front of the cabinet.

3. Remove two screws from the rear panel (located on each side) and remove it from the instrument.

4. Remove four screws from the left rear side of the cabinet securing the side panel to the instrument side chassis.

5. Remove the side panel from the instrument.

6. Pull the front panel and attached chassis forward and out of the cabinet.

NOTE

To ensure that the cabinet is properly grounded to the instrument chassis, the screws at the right-rear side and the bottom front of the cabinet must be tightly secured.

7. To reinstall the cabinet, perform the reverse of the preceding steps. Ensure that the cabinet is flush with the rear of the chassis and that the cabinet and rear-panel holes are align with the screw holes in the chassis frame.

Storage Circuit Board in Servicing Position

The following procedure describes how to secure the Storage circuit board into the servicing position to facilitate instrument disassembly and reinstallation for individual components or subassemblies.

1. Remove the five MEMORY buttons, SELECT WAVEFORM button, four ACQUISITION buttons, STORE button, and extension shafts from their respective switches by inserting a small screwdriver between the extension shaft and the switch shaft. Push down and forward until the extension shaft is disengaged and pull the shafts straight back through the front panel.

2. Disconnect the following two connectors from the Storage circuit board.

   a. P2111, a four-wire connector located near the middle left edge of the Storage circuit board.

   b. P2112, a four-wire connector located near the middle left edge of the Storage circuit board.

3. Remove three Storage circuit board screws that are identified by the etched words "Remove To Lift Board" (see Figure 6-7 for the location of the Storage board three screws).

4. Lift the Storage circuit board up until the cable of P9430 (on the front edge of the Storage circuit board) clears the back of the CURSORS control.

5. Remove P9430, a six-wire connector from the Storage circuit board by pulling it toward the front panel.

6. Continue to raise up the Storage circuit board to it standing position ensuring that the Board Latch clears the top of the chassis side rail. Place the Board Latch tab in the chassis side rail slot.

To lower the Storage circuit board into the instrument and to reconnect the connectors, perform the reverse of the preceding steps.

Support Chassis

The support chassis divides the inside of the instrument into two parts by connecting the center of the rear chassis and the front chassis together. The support chassis can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Remove the crt anode lead and High-Voltage Multiplier lead connectors from the anode clip on the Power-Supply shield.

3. Remove the anode clip from the Power-Supply shield through the hole in the support chassis.

4. Remove the two recessed screws from the rear chassis (located directly above the Z-AXIS connector) securing the support chassis.

5. Remove the three screws securing the top attenuator shield to the support chassis.

6. Slide the front of the support chassis toward the center and over the top attenuator shield away from underneath the front chassis bracket.

7. Remove the support chassis from the instrument.

To reinstall the support chassis, perform the reverse of the preceding steps.

Side-Chassis Assembly

The Side-Chassis Assembly can be removed and reinstalled as follows:

1. Disconnect the following three connectors from the Side-Chassis Assembly.

a. P4110, a two-wire connector located at the rear of the Side-Chassis Assembly.

b. P6423, a four-wire connector located at the rear of the Side-Chassis Assembly.

c. P9301, a five-wire connector located at the rear of the Side-Chassis Assembly.

2. Remove two screws and ground clip from the top of the side chassis and two screws from the bottom of the side chassis that secures the Side-Chassis Assembly to the instrument.

3. Remove the Side-Chassis Assembly from the instrument.

To reinstall the Side-Chassis Assembly, perform the reverse of the preceding steps.

Storage Circuit Board

The Storage circuit board can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Perform the "Support Chassis" removal procedure.

3. Perform the "Side-Chassis Assembly" removal procedure.

4. Remove the ground clip near the center edge of the Storage chassis (towards the instrument).

5. Unsolder the strap from the ground clip near the center of the Storage chassis and slide the strap through the slot in the chassis when removing the Storage chassis from the instrument in step 7.

6. Remove the four circuit board shield screws from the Storage circuit board (see Figure 6-7 for location of the four circuit board shield screws). Remove the two screws located on top of the Storage circuit board last.

7. Remove the Storage chassis from the instrument by lifting it up out of the bracket spacer. See Figure 6-7 for location of the bracket spacer.

8. Disconnect the following eight connectors from the inside of the instrument. Note cable color, location, and routing for reinstallation reference.

a. P4210, a four-wire connector located on the Main circuit board behind the CH 2 VOLTS/DIV switch.

b. P4220, a two-wire connector located on the right side of the Alternate Sweep circuit board.

c. P9010, a nine-wire connector located on the right side of the Main circuit board between the Timing and Alternate Sweep circuit boards.

d. P9050, a single white-wire connector located between the Alternate Sweep circuit board and the Power-Supply shield.

e. P9060, a single black-wire connector located between the Alternate Sweep circuit board and the Power-Supply shield.

f. P9210, a seven-wire connector located on the Main Board underneath the CRT shield near the delay line.

h. P9320, a four-wire connector located on the front edge of the Main circuit board between the Attenuator and Position Interface circuit boards.

i. P9410, a seven-wire connector located on the Sweep Referenced circuit board.

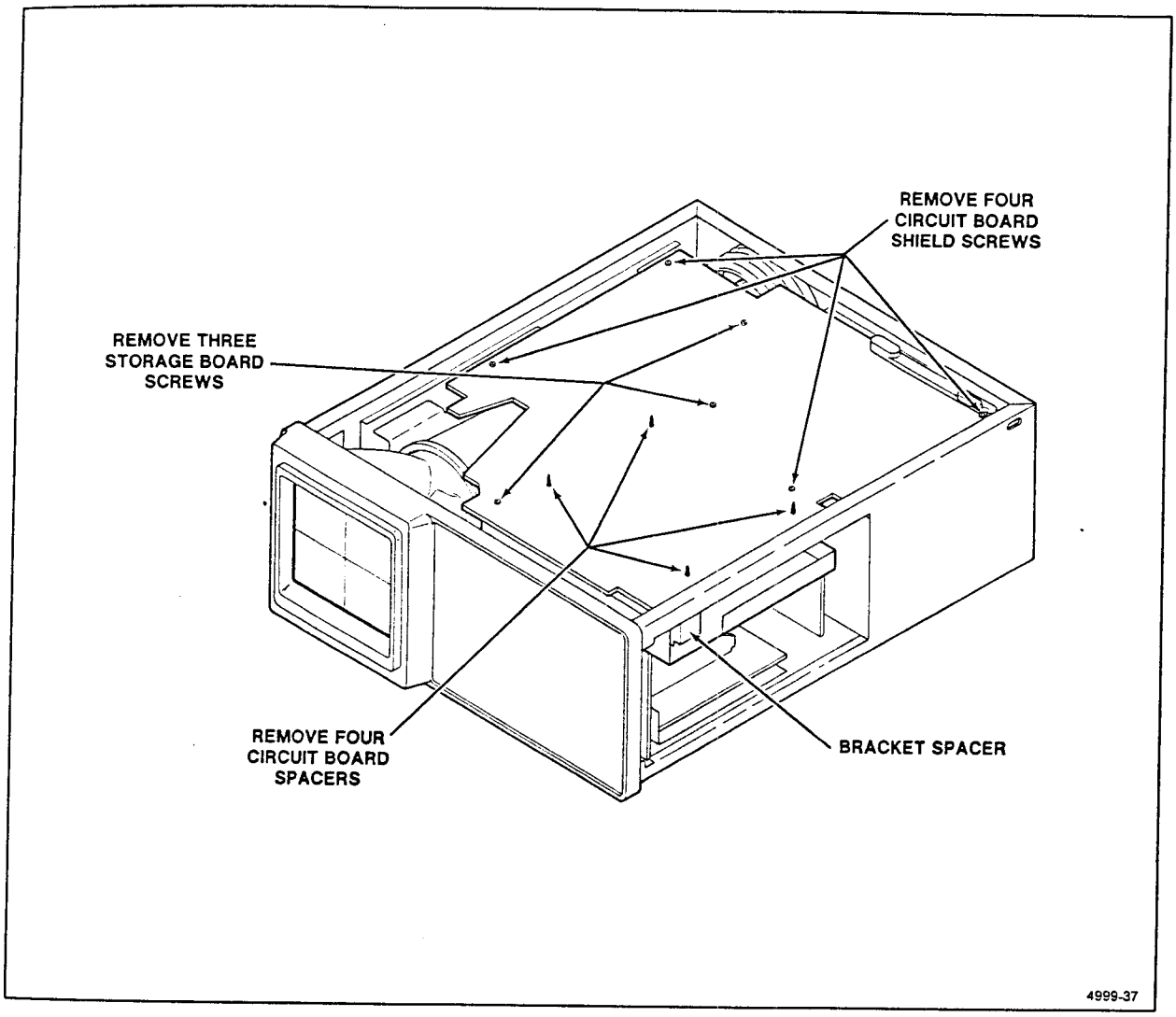


Figure 6-7. Location of screws and spacers on the Storage circuit board.

9. With one hand firmly holding the Input/Output and Vector Generator circuit board assembly and with the other hand use a long-nose pliers on the top side to squeeze and push the four circuit board spacers through the holes in the Storage circuit board (see Figure 6-7 for location of the circuit board spacers). Place the Input/Output and Vector Generator circuit board assembly inside the instrument temporarily to be reinstalled later.

10. Release the Board Latch and lower the Storage circuit board into the instrument.

11. Disconnect the ribbon connector (P6100) from the Input/Output and Vector Generator circuit board assembly.

12. Remove the Storage circuit board EMI clip from the side chassis rail located behind the front hinge.

13. Remove both the recessed screw and the chassis mounted rear hinge nearest to the Board Latch from the instrument (see Figure 6-8 for removal of the chassis recessed screw and hinge).

14. Slide the Storage circuit board back until the front and middle hinges separate and lift it out of the instrument. Ensure that P6100 is free from the Storage circuit board and the chassis rail.

NOTE

When installing the circuit board shield ensure that the black spacer tabs and the circuit board bracket are aligned with their respective holes in the shield. Also ensure that the strap (unsoldered in step 5) from the Input/Output circuit board is inserted through the circuit board shield slot to be resoldered to the ground clip.

To reinstall the Storage circuit board, perform the reverse of the preceding steps.

Input/Output and Vector Generator Circuit Boards Assembly

The Input/Output and Vector Generator circuit boards assembly can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Remove the circuit board shield (see "Storage Circuit Board" removal procedure steps 4 through 7).

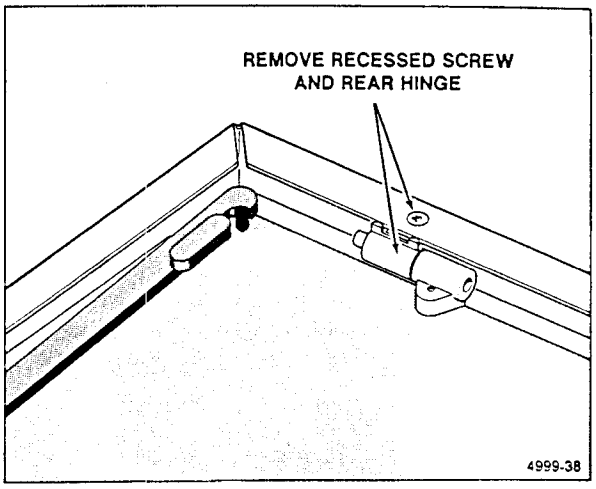


Figure 6-8. Recessed screw and rear hinge removal.

3. Disconnect the following five connectors from the Input/Output and Vector Generator circuit boards assembly. Note cable color, location, and routing for reinstallation reference.

a. Disconnect P6410 (ten-wire connector) and P6420 (nine-wire connector) from the Input/Output circuit board.

b. Disconnect P6110 (ten-wire connector), P6120 (nine-wire connector), and P6130 (eight-wire connector) from the Vector Generator circuit board.

4. Perform step 9 of "Storage Circuit Board" removal procedure and place the Input/Output and Vector Generator circuit assembly down inside the instrument temporarily for later removal in step 9 of this procedure.

5. Release the Board Latch and lower the Storage circuit board into the instrument.

6. Disconnect P6100, a ribbon connector on the Storage circuit board from the Input/Output and Vector Generator circuit board assembly.

7. Remove the screw from the chassis mounted hinge nearest to the Board Latch and separate it from the hinge on the Storage circuit board.

8. Unhinge the Storage circuit board from the chassis side rail to remove P6100 from the Storage circuit board. Set the Storage circuit board down on top of the Power Supply shield leaving enough space to lift the Input/Output and Vector Generator circuit boards assembly out of the instrument.

9. Remove the Input/Output and Vector Generator circuit boards assembly from the inside of the instrument (placed inside the instrument in step 4).

To reinstall the Input/Output and Vector Generator circuit boards assembly, perform the reverse of the preceding steps.

Cathode-Ray Tube

WARNING

Use care when handling a crt. Breakage of the crt may cause high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses should be worn. Avoid striking the crt on any object which may cause it to crack or implode. When storing a crt, either place it in a protective carton or set it face down on a smooth surface in a protected location with a soft mat under the faceplate.

The crt can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Perform the "Side-Chassis Assembly" removal procedure.

3. Disconnect four deflection-plate wires at the middle of the crt neck and unplug the Trace Rotation connector (P9006) from the Front-Panel circuit board (note the connection locations and wire colors for reinstallation reference).

WARNING

The crt anode lead and the High-Voltage Multiplier output lead retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, disconnect the High-Voltage Multiplier lead from the crt anode lead and ground both leads to the main instrument chassis.

4. Unplug the crt anode lead connector from the High-Voltage Multiplier lead located between the support chassis and the crt shield. Discharge both the anode lead connector and the High-Voltage Multiplier lead to chassis ground.

5. Remove two front-panel screws that retain the plastic crt frame and light filter to the front panel. Remove the crt frame and light filter from the instrument.

6. Remove the crt socket cap from the rear of the crt socket. Save the cap for reinstallation.

7. With the rear of the instrument facing you, place the fingers of both hands over the front edge of the front subpanel. Then, using both thumbs, press forward gently on the crt funnel near the front of the crt. When the crt base pins disengage from the socket, remove the crt and the crt shield through the instrument front panel. Place the crt in a safe place until it is reinstalled. If the plastic crt corner pads fall out, save them for reinstallation.

NOTE

When installing the crt into the instrument, reinstall any loose plastic crt corner pads that are out of place. Ensure all crt pins are straight and that the indexing keys on the crt base, socket, and shield are aligned. Ensure that the ground clip makes contact only with the outside of the crt shield.

To reinstall the crt, perform the reverse of the preceding steps.

Power-Supply Shield

The Power-Supply shield can be removed and reinstalled as follows:

1. Turn the instrument over (Main circuit board up) and remove the screw from the plastic power-supply cover (middle of the Main circuit board). Insert a small pointed tool into the hole in the left-rear corner of the rear chassis and gently push the power-supply cover tab in. Remove the power-supply cover by sliding it out from underneath the rear and side chassis.

2. Remove the screw securing the Power-Supply shield to the Main circuit board (located at the bottom of the Main circuit board near the middle of the side chassis frame). Turn the instrument over again (Storage circuit board on top) to continue with the Power-Supply Shield removal procedure.

3. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

4. Perform the "Support Chassis" removal procedure.

5. Remove one pan-head and two recessed screws securing the Power-Supply shield to the rear chassis frame. See Figure 6-9 for the location of the three screws on the rear chassis frame.

6. Remove the screw from the front upper-right hand corner of the Power-Supply shield.

7. Lift the Power-Supply shield up and out of the chassis frame by removing the right rear corner first.

NOTE

To reinstall the Power-Supply shield, ensure that the shield is placed in the frame guides on the rear chassis above the fuse holder and that the crt socket-wire assembly and crt anode lead are properly placed in their respective cutouts.

To reinstall the Power-Supply shield, perform the reverse of the preceding steps.

Line Filter Circuit Board and Cover

To remove the Line Filter circuit board and cover, perform the following steps:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Remove the Power-Supply shield (see the "Power-Supply Shield" removal procedure).

3. Remove the two recessed screws that secures the Filter circuit board to the rear chassis and lift the Line Filter circuit board out and away from the the filter capacitor.

4. Remove the four wires to the Line Filter circuit board by unsoldering two wires from the Main circuit board, one wire from the line filter, and one wire from the fuse holder (pull the protective cap completely off the fuse holder before unsoldering).

To reinstall the Line Filter circuit board and cover, perform the reverse of the preceding steps.

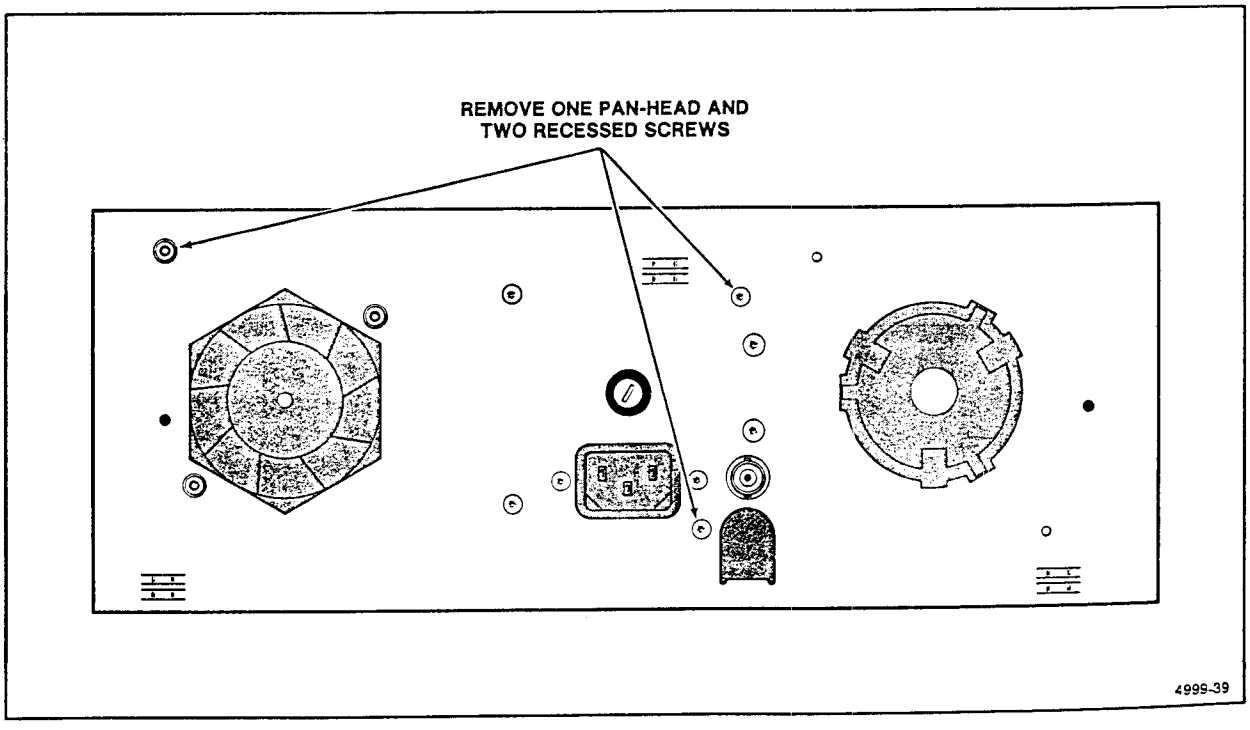


Figure 6-9. Location of screws securing Power-Supply shield and the support bracket to the rear chassis frame.

Fan

The fan can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Perform the "Power-Supply Shield" removal procedure.

3. Unsolder the two leads from the fan driver on the Main circuit board.

4. Remove two screws securing the fan to the rear chassis and two recessed screws securing the fan driver to the side chassis.

To reinstall the Fan, perform the reverse of the preceding steps.

Thermal Shutdown Circuit Board

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Perform the "Power-Supply Shield" removal procedure.

3. Perform the "Fan" removal procedure.

4. Stand the instrument up on its rear chassis (front panel up) and use a vacuum-desoldering tool to unsolder three pins from the Thermal Shutdown circuit board to the Main circuit board (W9070).

To reinstall the Thermal Shutdown circuit board, perform the reverse of the preceding steps.

Alternate Sweep Circuit Board

The Alternate Sweep circuit board can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Disconnect P4220, a two-wire connector located on the right side of the Alternate Sweep circuit board.

3. Remove the cable strap from the Alternate Sweep circuit board that secures the cable harness from the Storage circuit board.

4. Use a vacuum-desoldering tool to unsolder the 27 Alternate Sweep circuit board pins on the Main circuit board (W9400).

5. Unclip the plastic holder from the Power-Supply shield and remove the Alternate Sweep circuit board from the instrument.

To reinstall the Alternate Sweep circuit board, perform the reverse of the preceding steps.

Position Interface Circuit Board

The Position Interface circuit board can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Perform the "Support Chassis" removal procedure.

3. Disconnect P6113, a four-wire connector from Input/Output and Vector Generator circuit boards assembly.

4. Turn the instrument on its side and with a vacuum-desoldering tool, unsolder the six Position Interface circuit board wire straps from the Main circuit board.

5. Remove the Position Interface circuit board from the instrument and clean the wire-strap holes on the Main circuit board of any remaining solder.

To reinstall the Position Interface circuit board, perform the reverse of the preceding steps.

Channel 1 Logic and Channel 2 Logic Circuit Boards

The Channel 1 Logic and Channel 2 Logic Circuit Boards can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Perform the "Support Chassis" removal procedure.

3. Remove the remaining six screws that secure the top attenuator shield and ground strap (from the Front Panel circuit board) to the Attenuator circuit board and bottom shield.

4. Remove the top attenuator shield from the instrument.

5. Disconnect the following connectors from the Channel 1 Logic and Channel 2 Logic circuit boards, noting their locations for reinstallation reference:

a. P6111, a three-wire connector from Channel 1 Logic circuit board.

b. P6112, a three-wire connector from Channel 2 Logic circuit board.

6. Remove one screw each from the front of the Channel 1 Logic and Channel 2 Logic circuit boards.

7. Unsolder the two-wire strap from the rear of both the Channel 1 Logic and Channel 2 Logic circuit boards.

8. Remove the Channel 1 Logic and Channel 2 Logic circuit boards from the instrument.

To reinstall the Channel 1 Logic and Channel 2 Logic circuit boards, perform the reverse of the preceding steps.

Attenuator, Channel 1 Logic and Channel 2 Logic Circuit Boards Assembly

The Attenuator, Channel 1 and Channel 2 Logic Circuit Boards Assembly can be removed and reinstalled as follows:

1. Turn the instrument over (Main circuit board up) and remove two screws securing the Attenuator circuit board to the BNC bracket (located underneath the CH 1 OR X and CH 2 OR Y input connectors).

2. Unsolder the two resistors from the CH 1 OR X and CH 2 OR Y input connectors. Turn the instrument over again (Storage circuit board on top) to continue with the Attenuator, Channel 1 and Channel 2 Logic circuit boards assembly procedure.

3. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

4. Use a 1/16-inch hex wrench to loosen the set screws on both the CH 1 and CH 2 VOLTS/DIV Variable knobs and remove the knobs.

5. Set the CH 1 and CH 2 VOLTS/DIV switches to the same position. Note switch positions for reinstallation reference; then remove the knobs by pulling them straight out from the front panel.

6. Perform the "Support Chassis" removal procedure.

7. Remove the remaining six screws that secure the top attenuator shield and ground strap (from the Front Panel circuit board) to the Attenuator circuit board and bottom shield.

8. Remove the top attenuator shield from the instrument.

9. Disconnect the following connectors from the Channel 1 Logic, Channel 2 Logic and Attenuator circuit boards, noting their locations for reinstallation reference:

a. P6111, a three-wire connector from Channel 1 Logic circuit board.

b. P6112, a three-wire connector from Channel 2 Logic circuit board.

c. P9103, a four-wire connector located behind the CH 1 VOLTS/DIV switch assembly and underneath the Channel 1 Logic circuit board.

d. P9108, a four-wire connector located behind the CH 2 VOLTS/DIV switch assembly and underneath the Channel 2 Logic circuit board.

e. P9991, a three-wire connector located between CH 1 and CH 2 VOLTS/DIV Variable controls and Channel 1 and Channel 2 Logic circuit boards.

10. Remove the screw from the left rear corner of the Attenuator circuit board.

NOTE

The insulator on the left rear corner of the Timing circuit board may be loose. If the insulator is loose, remove and save it for the reinstallment of the Attenuator circuit board.

11. Pull the Attenuator, Channel 1 Logic and Channel 2 Logic circuit boards Assembly straight back from the front of the instrument until the circuit boards interconnecting pins are disengaged and the switch shafts are clear of both the Front-Panel circuit board and the two Input Coupling switch shafts (located between the front panel and the subpanel). Then lift out the entire assembly through the top of the instrument.

12. If removal of Channel 1 Logic and Channel 2 Logic circuit boards from the assembly is desired, perform the "Channel 1 Logic and Channel 2 Logic Circuit Boards" removal procedure steps 6 through 8.

NOTE

When reinstalling the Attenuator, Channel 1 and Channel 2 Logic circuit boards Assembly, ensure that the interconnecting pins are aligned with the Front-Panel circuit board, connectors and that the two resistors (soldered to the bottom of the Attenuator circuit board) are not touching the Front-Panel circuit board. Push the Attenuator circuit board forward and, at the same time, press the front end of the board down slightly. Align the two Input Coupling switch shafts with the front-panel holes by moving either the Channel 1 or the Channel 2 Input Coupling switch knob.

To reinstall the Attenuator, Channel 1 and Channel 2 Logic circuit boards assembly, perform the reverse of the preceding steps.

Sweep Reference Circuit Board

The Sweep Reference circuit board can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Disconnect P9410, an seven-wire connector located behind the SEC/DIV Variable control on the Sweep Reference circuit board.

3. Disconnect P5201, a three-wire connector located on the right side of the Sweep Reference circuit board.

4. Unsolder the two resistors from the Timing Circuit board on the right side of the SEC/DIV Variable control.

5. Remove the shaft extension by loosening the setscrew with a 0.50-hex wrench.

6. Remove the SEC/DIV variable control nut with a 9/16 inch open-end wrench.

7. Remove the Sweep Reference circuit board.

To reinstall the Sweep Reference circuit board, perform the reverse of the preceding steps.

Timing, Sweep Interface, and Sweep Reference Circuit Boards Assembly

The Timing, Sweep Interface, and Sweep Reference circuit boards assembly can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Use a 1/16-inch hex wrench to loosen the set screw of the SEC/DIV Variable knob. Remove the SEC/DIV Variable knob.

3. Set both A and B SEC/DIV knobs to the EXT CLK position. Use a 1/16-inch hex wrench to loosen the two set screws that secure the A and B SEC/DIV knob; pull off the knob from the shaft assembly.

4. Use a 1/16-inch hex wrench to loosen two set screws securing the A SEC/DIV dial to the shaft assembly. Remove the dial from the shaft.

5. Disconnect the following connectors from the assembly, noting their locations for reinstallation reference:

   a. P9700, a 10-wire connector located on the right edge of the Timing circuit board.

   b. P9705, an eight-wire connector located at the rear of the Timing circuit board.

   c. P6421, an five-wire connector located on the Sweep Interface circuit board.

   d. P9410, an seven-wire connector located behind the SEC/DIV Variable control on the Sweep Reference circuit board.

6. Remove the screw located at the right rear of the Attenuator circuit board (securing both the Attenuator and the Timing circuit boards to the Bottom shield).

7. Remove the three securing screws from the Timing circuit board (the screws are located at the right front corner, left front side by the SEC/DIV switch shaft, and at the right rear corner of the circuit board).

NOTE

The insulator on the left rear corner of the Timing circuit board may be loose. If the insulator is loose, remove and save it for the reinstallment of the Timing circuit board.

8. Pull the Timing circuit board straight back from the front of the instrument until the circuit board interconnecting pins are disengaged and the switch shaft is clear of the Front-Panel circuit board.

9. If removal of Sweep Reference circuit board from the assembly is desired, perform the "Sweep Reference Circuit Board" removal procedure steps 3 through 7.

NOTE

Ensure that the Timing circuit board interconnecting pins are aligned to the Front-Panel circuit board connectors before reinstallation.

To reinstall the Timing, Sweep Interface, and Sweep Reference circuit boards assembly, perform the reverse of the preceding steps.

SWEEP INTERFACE CIRCUIT BOARD SEPARATION. To remove the Sweep Interface circuit board from the Timing circuit board perform the following steps.

1. Use a vacuum-desoldering tool to unsolder the 22-wire strap W1304 from the Sweep Interface to the Timing circuit board.

2. Remove the Sweep Interface circuit board and clean the wire-strap holes in the Timing circuit board.

To reinstall the Sweep Interface circuit board, perform the reverse of the preceding steps.

Bottom Shield, Attenuator and Timing Circuit Boards Assembly

The Bottom Shield, Attenuator, and Timing circuit boards assembly can be removed and reinstalled as follows:

1. Place the instrument upside down and remove the three screws and one spacer post securing the Bottom shield to the Main circuit board.

2. Perform steps 1 through 9 of the "Attenuator, Channel 1 Logic and Channel 2 Logic Circuit Board" removal procedure.

3. Perform steps 2 through 5 of the "Timing, Sweep Interface, and Sweep Reference Circuit Boards" removal procedure.

4. Pull the Bottom shield, along with the attached circuit boards straight back from the front of the instrument until the interconnecting pins on the circuit boards are disengaged and the switch shafts are clear of the holes in the Front-Panel circuit board; then lift out the entire assembly through the top of the instrument.

5. If accessibility to the bottom of either the Attenuator or the Timing circuit board is desired, refer to step 10 of the "Attenuator, and Channel 1 and Channel 2 Logic Circuit Boards Assembly" removal procedure and to step 7 of the "Timing, Sweep Interface, and Sweep Reference Circuit Boards Assembly" removal procedure.

To reinstall the Bottom Shield, Attenuator, and Timing circuit boards assembly, perform the reverse of the preceding steps.

Front-Panel Circuit Board

The Front-Panel circuit board can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Perform the "Support Chassis" removal procedure.

3. Perform the "Cathode-Ray Tube" removal procedure.

4. Perform the "Bottom shield, Attenuator and Timing Circuit Boards Assembly" removal procedure.

5. Remove the knobs from the following control shafts by pulling them straight out from the front panel:

   a. Channel 1 and Channel 2 POSITION.

   b. A/B SWP SEP.

   c. Horizontal POSITION.

   d. B TRIGGER LEVEL.

6. Use a 1/16-inch hex wrench to loosen the setscrew of the HF REJECT knob. Remove the HF REJECT knob.

7. Use a 1/16-inch hex wrench to loosen the setscrew of the A TRIGGER LEVEL knob. Remove the A TRIGGER LEVEL knob.

8. Unsolder both the resistor to the EXT INPUT center connector and the wire strap to the EXT INPUT ground lug.

9. Unsolder the two wire straps from VAR HOLDOFF control.

10. Unsolder the single wire from the PROBE ADJUST connector and the two wires from the VAR HOLDOFF control (leading to the Front-Panel circuit board).

11. Remove the following screws:

a. Three screws (and ground strap) securing the upper part of the Front-Panel circuit board to the front panel.

b. Two recessed frame-securing screws at the left-rear corner of the chassis frame.

c. Two bottom screws securing the Main circuit board to the left bottom side of the chassis frame.

d. One screw securing the delay line to the chassis frame on the left side of the instrument.

e. Two recessed frame-securing screws at the right-front corner.

NOTE

At this point, any component on the Front-Panel circuit board may be accessed for removal and replacement. If circuit board replacement is intended, continue with the last two steps 10 and 11.

12. Pull the left-front frame assembly apart from the right-rear frame assembly.

NOTE

If a vacuum-desoldering tool is not available, lift each strap out of the Main circuit board as the joint is heated.

13. Use a vacuum-desoldering tool to unsolder the 45 (W9001) wire straps from the Main circuit board (connecting to the Front-Panel circuit board).

14. Remove the Front-Panel circuit board from the instrument and clean the wire-strap holes on the Main circuit board of any remaining solder.

To reinstall the Front-Panel circuit board, perform the reverse of the preceding steps.

Main Circuit Board

All components on the Main circuit board are accessible either directly or by removing either the Storage circuit board, the crt, the Bottom shield, Attenuator, Timing circuit-boards assembly, and the Power-Supply shield. Removal of the Main circuit board is required only when it is necessary to replace the circuit board with a new one.

The Main circuit board can be removed and reinstalled as follows:

1. Perform the "Storage Circuit Board in Servicing Position" removal procedure.

2. Perform the "Support Chassis" removal procedure.

3. Perform the "Side-Chassis Assembly" removal procedure.

4. Perform step 3 under the "Input/Output and Vector Generator Boards Assembly" removal procedure.

5. Disconnect the three-wire B DELAY TIME POSITION potentiometer connector (P9644) from the Main circuit board (located on the right side of the Main circuit board).

6. Perform the "Alternate Sweep Circuit Board" removal procedure.

7. Disconnect the connectors from the Attenuator and Timing circuit boards assembly, noting their locations for reinstallation reference.

8. Remove three screws and one spacer securing the Bottom shield to the Main circuit board.

9. Perform the "Power-Supply Shield" removal procedure.

10. Unsolder two wires from the Main circuit board to the Filter circuit board.

11. Unsolder the rear-panel EXT Z AXIS connector wire from the Main circuit board.

12. Unsolder the two leads on the Main circuit board from the fan driver.

13. Unsolder the three leads on the chassis mounted CR970 from the Main circuit board.

14. Disconnect P9070, a three-wire connector from the Main circuit board to the heat-sink mounted Q9070.

15. Remove the FOCUS control shaft assembly by pulling it straight out from the front panel.

16. Remove the POWER switch extension-shaft assembly by first pressing in the POWER button to the ON position. Then insert a scribe (or similar tool) into the notch between the end of the switch shaft and the end of the extension shaft and gently pry the connection apart. Push the extension shaft forward, then sideways, to clear the switch shaft. Finally, pull the extension shaft back and out of the instrument.

17. Remove two recessed screws securing the power-supply transistor heat-sink assembly to the right side of the chassis frame.

WARNING

The crt anode lead and the output terminal to the High-Voltage Multiplier will retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, ground the crt side of the anode lead to the main instrument chassis.

18. Disconnect the crt anode lead from the High-Voltage Multiplier anode lead by carefully pulling the anode plug out of the jack. Discharge the plug tip to the chassis.

19. Unsolder two sets of crt socket wires from the Main circuit board, noting wire color and position for reinstallation reference.

20. Unsolder two sets of delay-line wires from the Main circuit board, noting wire color and position for reinstallation reference.

21. Remove three screws securing the Main circuit board to the instrument chassis frame (one under the EXT Z AXIS connector and two along the left side of the Main circuit board).

22. Use a vacuum-desoldering tool to unsolder the 45 wire straps (W9001) connecting the Main circuit board to the Front-Panel circuit board) from the Main circuit board.

NOTE

If a vacuum-desoldering tool is not available, lift each wire strap out of the Main circuit board as the joint is heated. Use care to maintain, as nearly as possible, the original shape and spacing of the wire straps to facilitate replacing the circuit board.

23. Push the wire-strap connection end of the Main circuit board down until it is clear of all wire strap ends; then remove it through the bottom of the instrument frame. Ensure that the wire straps are not bent out of place.

NOTE

When installing the Main circuit board, ensure that the circuit board is in the guides at the rear and right side of the frame and that the 45 wire straps of W9001 are inserted into their corresponding holes.

To reinstall the Main circuit board, perform the reverse of the preceding steps.

OPTIONS

INTRODUCTION

This part contains a general description of instrument options available at the time of publication of this manual. Additional information about instrument options and option availability can be obtained either by consulting the current Tektronix Product Catalog or by contacting your local Tektronix Field Office or representative.

POWER CORD OPTIONS

Instruments are shipped with the detachable power-cord configuration ordered by the customer. Descriptive information about the international power-cord options is provided in "Preparation for Use" in Section 2. The following list identifies the Tektronix part numbers for the available power cords.

Standard (United States)	161-0104-00	Option A3 (Australian)	161-0104-05
Option A1 (Universal Euro)	161-0104-06	Option A4 (North American)	161-0104-08
Option A2 (United Kingdom)	161-0104-07	Option A5 (Switzerland)	161-0167-00

OPTION 33

Option 33, the **Travel Line** option, provides impact protection needed for rough industrial and service environments. When the instrument is ordered with Option 33, the instrument comes equipped with the Accessory Pouch and the Front Panel Cover, front and rear mounted shock absorbing rubber guards, an easy-to-use power cord wrap, and a carrying strap.

OPTION 10 AND OPTION 12

INTRODUCTION

Option 10 provides a communications interface and additional memory for the instrument. The interface implemented conforms to the specifications contained in IEEE Standard Digital Interface for Programmable Instrumentation (ANSI/IEEE Std 488-1978), commonly referred to as the General Purpose Interface Bus (GPIB). It also complies with a Tektronix Standard relating to GPIB Codes, Formats, Conventions and Features.

Option 12 provides a communications interface and additional memory for the instrument. The interface implemented conforms to RS-232-C specifications. It also complies with a subset of the Tektronix Codes, Formats, Conventions and Features standard.

Three indicators, displayed on the crt and labeled on the bezel tag, display the condition of the options. A battery backed-up CMOS memory and its battery are also included in the options. Option commands allow saving additional SAVE REF waveforms in the memory.

WARNING

The battery used in this device contains lithium. Do not expose to heat. Do not short terminals. See service information for complete instructions.

The communication options allow remote control of oscilloscope functions. This remote control is accomplished by messages sent to the instrument via either the GPIB (IEEE-488 Standard Bus) or the RS-232-C interface. Messages used are defined either in ANSI/IEEE-488-1978 or in the Tektronix standard on Codes, Formats, Conventions, and Features. Messages to the option can have one of three purposes:

1. Query the state of the oscilloscope.
2. Query the results of measurements made.
3. Set the instrument operation mode.

The main purpose of the communication options is to allow digitized waveform data to be sent and received by the instrument.

STANDARD FUNCTIONS, FORMATS, AND FEATURES

The interface-function repertoire of a GPIB instrument, in terms of interface-function subsets, is identified in ANSI/IEEE Std 488-1978. The status of subsets applicable to this instrument with Option 10 are listed in Table 7-1.

Both the GPIB interface and the RS-232-C interface conform to a Tektronix standard on Codes, Formats, Conventions, and Features of messages sent over the bus to communicate with other instruments equipped with a like interface. Specific features implemented in this instrument are listed in Table 7-2, and specific formats implemented are shown in Table 7-3.

Table 7-1
Function Subsets Implemented

Function Subset	Capability	States Omitted	Other Requirements	Other Subsets Required
SH1 (Source Handshake)	Complete Capability	None	None	T6
AH1 (Acceptor Handshake)	Complete Capability	None	None	None
T6 (Talker)	Basic Talker, Serial Poll, Talker Only, Unaddress if MLA	None	Include [MLA (ACDS)]	SH1 and L3
L3 (Listener)	Basic Listener, Listen Only, Unaddress if MTA	None	Include [MTA (ACDS)]	AH1 and T6
SR1 (Service Request)	Complete Capability	None	None	T6
RL2 (Remote/Local)	No Local Lock Out	LWLS and RWLS	None	L3
PP0 (Parallel Poll)	No Capability	All	None	None
DC1 (Device Clear)	Complete Capability (Selective Device Clear)	None	None	L3
DT0 (Device Trigger)	No Capability	All	None	None
C0 (Controller)	No Capability	All	None	None
E2 (Drivers)	Three-state			

Table 7-2
Specific Format Choices

Format Parameter	Choice Made
Format Characters	Not transmitted; ignored on reception.
Message Terminator	Either EOI or LF modes can be selected for implementation.
Measurement Terminator	Follows program message-unit syntax.
Link Data (Arguments)	Used in Listen and Talk.
Multiple Event Reporting	Not implemented.
Instrument Identification Query	Descriptors added for all options, including GPIB.
Set Query	Extended by using other commands.
Device Trigger (DT)	Not implemented.
Init Command	Causes the instrument to return to a power-on condition. All operating modes will then agree with front-panel settings.
Time/Date Commands	Not implemented.
Stored Setting Commands	Not implemented.
Waveform Transmission	Implemented.
Return to Local (rtl)	Asserted when any front-panel control attempts to change a GPIB-controllable function.
IEEE 728	Compliance not intended.

PERFORMANCE CONDITIONS

The specifications for the GPIB Option, RS-232-C Option, and the Memory Option are listed in Table 7-4. All other specifications for the instrument (including the performance conditions) are identical to those specified in "Specification" in Section 1 of this manual.

OPTIONS SIDE PANEL

The instrument is supplied with one of three possible side panels. The standard side panel (Figure 3-8) includes one AUXILIARY connector. The Option 10 side panel (Figure 7-1A) includes one AUXILIARY connector, one GPIB (IEEE 488-1978) interface port, and one PARAMETERS switch. The side panel for Option 12 instruments (Figure 7-1B) includes one AUXILIARY connector, one RS-232-C interface port (includes one DTE and one DCE connector), and one PARAMETERS switch. The Controls, Connectors, and Indicators part of this manual contains information on the use of the AUXILIARY Connector. Refer to Figure 7-1 for location of items 46 through 51.

(46) **AUXILIARY Connector**—Provides connections for an X-Y Plotter and an External Clock input (see Controls, Connectors, and Indicators).

(47) **GPIB Connector**—Provides the ANSI/IEEE Std 488-1978 compatible electrical and mechanical connection to the GPIB. The connector is only on instruments with Option 10. The function of each pin of the connector is shown in Table 7-5.

Table 7-3
Implementation of Specific Features

Feature	Choice Made	Comments
Secondary Addressing	Not implemented.	
Indicators	ADDR (addressed), SRQ (service request), and PLOT (acquisitions locked out) indicators are included.	
Parameter Selection	10 position switch. Instrument reinitializes to power-up state with exception of issuing power-on service request.	To retain the instrument's preinitialization setup, the controller should store the response to a SET query before a change is made; then return the settings afterwards.

Table 7-4
Option Electrical Characteristics

Characteristics	Performance Requirements
EXTENDED MEMORY	
Power-Down Battery Voltage	Memory retained for battery voltages greater than 2.3 V.[a]
Data Retention	Memory maintained at least 6 months without instrument power.[a]
Battery Life	Power-down data retention specification shall be maintained for 3 years without battery change.[a]
Power-Down Detection Threshold	Fail asserted for supply drop to less than 4.75 V.[a] Reset held until supply is greater than 5.0 V.[a]
Reset Delay	Power-down interrupt to reset delay ⩾ 1 ms.[a]
GPIB OPTION	
GPIB Requirements	Complies with ANSI/IEEE Standard 488-1978.[a]
RS-232-C OPTION	
RS-232-C Requirements	Complies with EIA Standard RS-232-C.[a]
Baud Rates Available Rates	110, 300, 600, 1200, 1800, and 2400 baud.
Accuracy	< 1% error.[a]

[a] Performance Requirement not checked in manual.

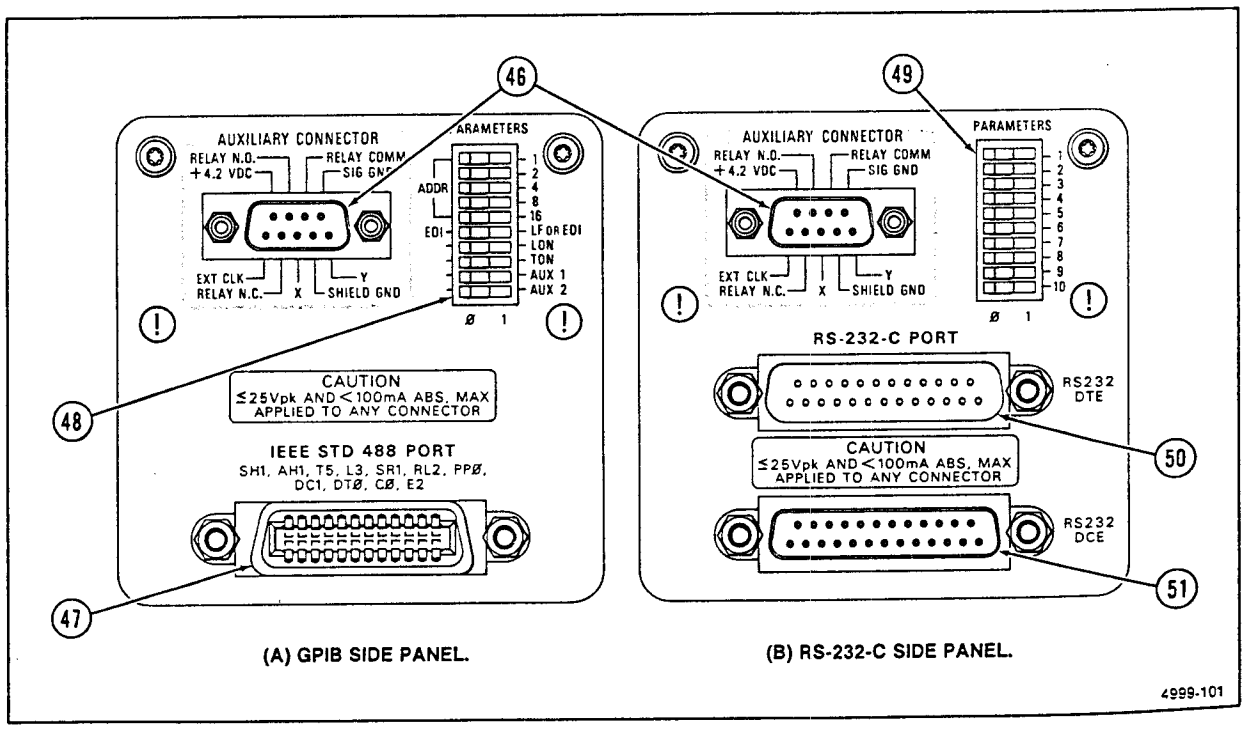


Figure 7-1. Option side panels.

Table 7-5
GPIB Connector

Pin	Line Name	Description
1	DIO1	IEEE-488 Data I/O
2	DIO2	IEEE-488 Data I/O
3	DIO3	IEEE-488 Data I/O
4	DIO4	IEEE-488 Data I/O
5	EOI	IEEE-488 END or Identify
6	DAV	IEEE-488 Handshake
7	NRFD	IEEE-488 Handshake
8	NDAC	IEEE-488 Handshake
9	IFC	IEEE-488 Input
10	SRQ	IEEE-488 Output
11	ATN	IEEE-488 Input
12	SHIELD	System Ground (Chassis)
13	DIO5	IEEE-488 Data I/O
14	DIO6	IEEE-488 Data I/O
15	DIO7	IEEE-488 Data I/O
16	DIO8	IEEE-488 Data I/O
17	REN	IEEE-488 Input
18	GND	Digital Ground (DAV)
19	GND	Digital Ground (NRFD)
20	GND	Digital Ground (NDAC)
21	GND	Digital Ground (IFC)
22	GND	Digital Ground (SRQ)
23	GND	Digital Ground (ATN)
24	GND	Digital Ground (LOGIC)

(48) **GPIB PARAMETER Switch**—Allows the selection of setup options for the GPIB interface. The switch is read at power-up and when interface clear messages are received. Five sections of the switch select the GPIB address, one selects the terminator, two select talk/listen modes, and two are used for printer/plotter selection. The function of each switch section is shown in Table 7-6.

Table 7-6
GPIB PARAMETERS Switch

Switch Section	Switch Position	Function
1		Address selection
	0	0
	1	1
2		Address selection
	0	0
	1	2
3		Address selection
	0	0
	1	4
4		Address selection
	0	0
	1	8
5		Address selection
	0	0
	1	16
6		Terminator selection
	0	EOI
	1	LF or EOI
7	0	No function
	1	LON
8	0	No function
	1	TON
9		Printer/plotter selection[a]
10		Printer/plotter selection[a]

[a]Switches 9 and 10 select printer/plotter devices at power-up. The devices may be changed after power-up using Option commands, or by using the MENU. Two EPSON(tm) formats are selectable. EPS7 uses seven print wires per head pass, and is usually slower. It is the chr$(27) "L" mode. EPS8 uses eight print wires per head pass, and is usually the faster print-head speed. It is the chr$(27) "Y" mode. In this mode most Epson and Epson-compatible printers will not strike any print wire more often than every second pixel. EPS8 is selected when parity is disabled. Devices are selected with the following switch positions:

Switch 9	Switch 10	Device Selected
0	0	HP-GL® plotter
1	0	[EPS7] or EPS8
0	1	ThinkJet® printer

® HP-GL and ThinkJet are trademarks of Hewlett - Packard Company. Epson is a trademark of Epson Corporation.

(49) **RS-232-C PARAMETER Switch**—Allows the selection of setup options for the RS-232-C interface. The switches are read at power-up and when interface clear messages are received. Four sections of the switch select the baud rate, three select parity, one selects the terminator, and two are for printer/plotter selection. The function of each switch section is shown in Table 7-7.

Table 7-7
RS-232-C PARAMETERS Switch

Switch Section	Switch Position	Function
1	--	Baud rate[a]
2	--	Baud rate[a]
3	--	Baud rate[a]
4	--	Baud rate[a]
5		Parity enable
	0	Parity error will NOT cause SRQ (also selects 8-bit character length)
	1	Parity error WILL cause SRQ (also selects 7-bit character length)
6		Parity select[b]
7		Parity select[b]
8		Line terminator selection
	0	Lines are terminated with carriage return (CR)
	1	Lines are terminated with carriage return-line feed (CR-LF)
9		Printer/plotter selection[c]
10		Printer/plotter selection[c]

[a]See Table 7-8

[b]See Table 7-9

[c]Switches 9 and 10 select printer/plotter devices at power-up. The devices may be changed after power-up using Option commands, or by using the MENU. Two EPSON® formats are selectable. EPS7 uses seven print wires per head pass, and is usually slower. It is the chr$(27) "L" mode. EPS8 uses eight print wires per head pass, and is usually the faster print-head speed. It is the chr$(27) "Y" mode. In this mode most Epson and Epson-compatible printers will not strike any print wire more often than every second pixel. EPS8 is selected when parity is disabled. Devices are selected with the following switch positions:

Switch 9	Switch 10	Device Selected
0	0	HP-GL® plotter
1	0	[EPS7] or EPS8
0	1	ThinkJet® printer

® HP-GL and ThinkJet are trademarks of Hewlett - Packard Company. Epson is a trademark of Epson Corporation.

Table 7-8
Baud Rate

Index	Switch Position 4 3 2 1	Baud Rate
0	0 0 0 0	50
1	0 0 0 1	75
2	0 0 1 0	110
3	0 0 1 1	134.5
4	0 1 0 0	150
5	0 1 0 1	300
6	0 1 1 0	600
7	0 1 1 1	1200
8	1 0 0 0	1800
9	1 0 0 1	2000
10	1 0 1 0	2400
11	1 0 1 1	3600
12	1 1 0 0	4800
13	1 1 0 1	7200
14	1 1 1 0	9600
15	1 1 1 1	Off Line

(50) **RS-232-C DTE Connector**—Provides connection meeting the EIA RS-232-C standard for data terminal equipment. The connector is shown in Figure 7-1B. Table 7-10 lists the function of each pin of the connector. The connector is only on Option 12 instruments.

NOTE

Some controllers use nonstandard connectors and pin assignments. Consult your controller operators manual for specific interfacing information.

(51) **RS-232-C DCE Connector**—Provides connection meeting the EIA RS-232-2 standard for data communications equipment. The connector is shown in Figure 7-1B. Table 7-11 lists the function of each pin of the connector. The connector is only on Option 12 instruments.

NOTE

Some controllers use nonstandard connectors and pin assignments. Consult your controller operators manual for specific information.

Table 7-9
Parity Selection[a]

Index	Switch Position 6 7	Parity Type	Comment
0	0 0	ODD	The most significant bit (MSB) is set or cleared so that the number of 1s per byte is ODD.
1	0 1	EVEN	The MSB is set or cleared so that the number of 1s per byte is even.
2	1 0	MARK	The MSB is set.
3	1 1	SPACE	The MSB is cleared.

[a]Characters are always accepted if possible. An SRQ is sent if the received parity doesn't match the parity selected. Parity must be disabled (switch position 5 set to 0) for binary transfers to take place.

Table 7-10
RS-232-C DTE Connector

Pin	Signal Name		Function
	Internal	External	
1	CHAS GND	CHAS GND	Chassis ground
2	ITXD	TXD	Transmitted data
3	IRXD	RXD	Received data
4	IRTS	RTS	Request to send
5	ICTS	CTS	Clear to send
6	IDSR	DSR	Data set ready
7	SIG GND	SIG GND	Signal ground
8	IRLSD2	RLSD	Received line signal detect
20	IDTR	DTR	Data terminal ready

Table 7-11
RS-232-C DCE Connector

Pin	Signal Name		Function
	Internal	External	
1	CHAS GND	CHAS GND	Chassis ground
2	IRXD	TXD	Transmitted data
3	ITXD	RXD	Received data
4	ICTS	RTS	Request to send
5	IRTS	CTS	Clear to send
6	IDTR	DSR	Data set ready
7	SIG GND	SIG GND	Signal ground
8	IRLSD1	RLSD	Received line signal detect
20	IDSR	DTR	Data terminal ready

INTERFACE STATUS INDICATORS

Three indicators appear in the crt readout to indicate the status of the communications options. The indicators are labeled SRQ, ADDR, and PLOT on the crt bezel, and appear as intensified lines in the crt under the labels. Refer to Figure 7-2 for the location of items 52 through 54.

(52) **SRQ Indicator**—Indicates the communications option requires service by the controller. Service requests are cleared when the instrument has been polled for its status and no further warning or error conditions are pending. The communication options assert Service Request (SRQ) when powered up.

(53) **ADDR Indicator**—Indicates the instrument is addressed to talk or listen on the GPIB option. Indicates carrier detect on the RS-232-C option.

(54) **PLOT Indicator**—Indicates the communication option is currently sending waveform data over its interface and acquisitions are inhibited.

MENU SELECTED FUNCTIONS

The following functions are available as part of the ADVANCED FUNCTIONS Menu on instruments containing the GPIB or RS-232-C options.

REFERENCE—Allows a SAVE REF memory to be Erased or Copied.

ERASE—Selects and erases a nonvolatile SAVE REF memory.

COPY—Selects and copies one nonvolatile SAVE REF memory to another SAVE REF memory.

COMM—Allows the selection of parameters for optional communications options, when they are present.

DATA—Selects the data-coding format, source or destination of the data, and channel selection for data transmissions.

STOP BITS—Selects the number of stop bits for RS-232-C data transmissions.

FLOW—Sends the waveform data to a listen only device.

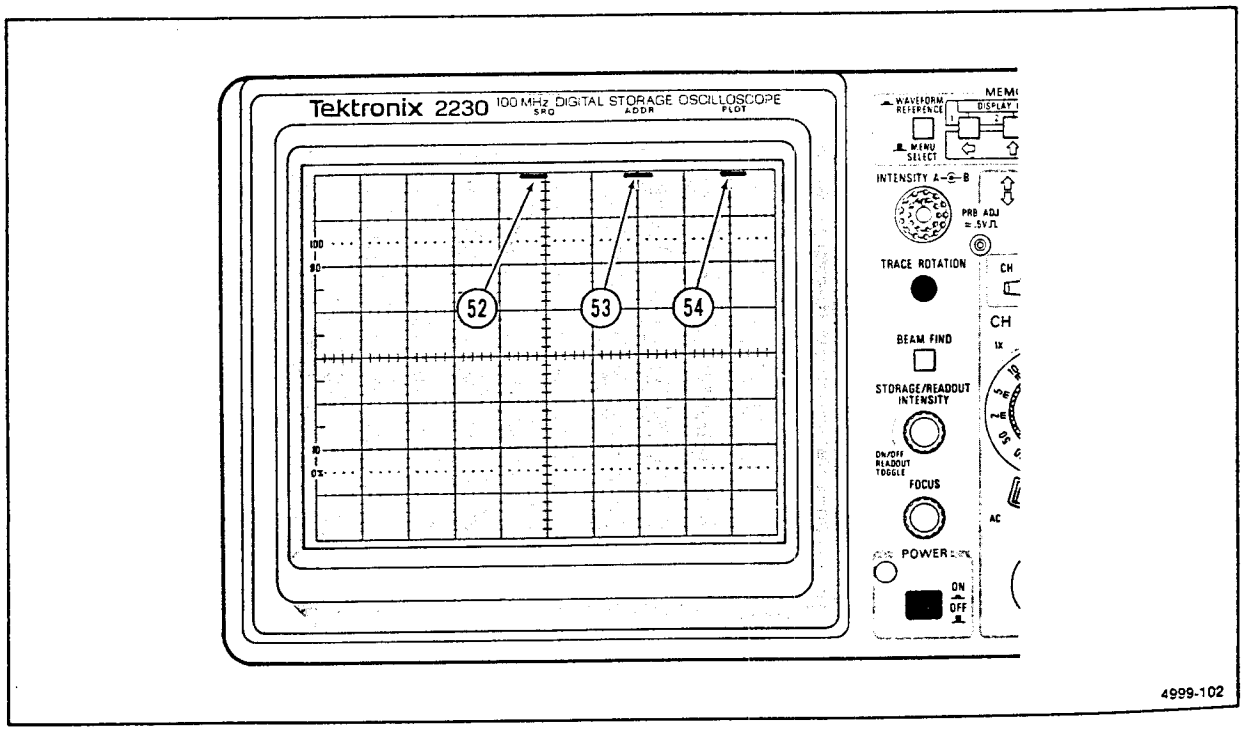


Figure 7-2. Interface status indicators.

Menus are displayed with as much of the selection path visible as possible. This method displays the current location in the menu as well as the available alternatives and messages on how to make a selection.

The COMM Menu:

The COMM menu resides under the ADVANCED FUNCTIONS menu:

```
ADVANCED FUNCTIONS
  REFERENCE
  COMM
  ACQ MODE SETUP TREE
  DIAGNOSTICS
```

Once COMM is selected, its submenus appear:

```
COMM
  DATA
  STOP BITS (Option 12 only)
  FLOW (Option 12 only)
```

If DATA is selected, its functions appear:

```
DATA
  ENCDG
  SOURCE
  TARGET
  CHANNEL
```

The ENCDG function selects waveform encoding for transmission and expected encoding for waveform reception. At power-up, the default encoding is binary. Make one of three choices from the menu:

```
ENCDG
  ASCII
  BINARY
  HEX
```

The SOURCE function selects whether one of the Reference Memories or the current acquisition is the source for waveform transfers. If REF is selected, use the Cursor knob to select the actual reference. REF4 is an explicit 4K reference:

```
SOURCE
  REF
  ACQ
```

The TARGET function is nearly identical to the SOURCE function. The only difference is that ACQ is not a valid TARGET. The TARGET reference is the destination for all waveforms sent to the instrument:

```
TARGET
  REF
```

Like SOURCE, waveform TARGET references are selected with the Cursor knob.

The CHANNEL function selects the channel whose waveform is sent. With the exception of XY waveforms, only data from one channel is sent at a time, even if both channels were acquired in ALT or CHOP Vertical Mode:

```
CHANNEL
  CH1
  CH2
```

The STOP BITS function, available ONLY on Option 12 (RS-232-C), sets the number of stop bits. Use the Cursor knob to select.

The FLOW function, available ONLY on Option 12 (RS-232-C), enables or disables Control-S/Control-Q handshaking. FLOW must be OFF during binary waveform transfers.

```
FLOW
  ON
  OFF
```

GPIB PARAMETER SELECTION

Selection of GPIB parameters (primary address, message terminator, and talk/listen mode) can be made at any time using the GPIB PARAMETERS switch and Table 7-6.

Primary Address

The selected GPIB address establishes both the primary talk and listen addresses for the oscilloscope. It can be set to any value between 0 and 31, inclusive.

NOTE

This instrument has no provisions for secondary addressing as defined by ANSI/IEEE Std 488-1978.

With an address of 31, the instrument still presents an active load but does not respond to nor interfere with any bus traffic. This is useful for changing the instrument's status without turning off the oscilloscope's power.

Input End-of-Message Terminator

The end-of-message terminator can be selected to be either the End-or-Identify (EOI) interface signal or the Line-Feed (LF) character.

When EOI (normal mode) is selected as the terminator, the instrument will:

- Accept only EOI as the end-of-message terminator.
- Assert EOI concurrently with the last byte of a message.

When LF is selected as the terminator, the instrument will:

- Accept either LF or EOI as the end-of-message terminator.
- Send Carriage Return (CR) followed by LF at the end of every message, with EOI asserted concurrently with the LF.

Talk/Listen Mode

Three talk/listen modes are selectable:

- TALK ONLY mode allows the instrument to send data over the GPIB.
- LISTEN ONLY mode permits the instrument to receive data over the GPIB.
- TALK/LISTEN mode (both TON and LON modes selected) allows the instrument to both send and receive data over the GPIB.

The default mode is TALK/LISTEN.

To select or change the talk/listen mode, select TON and/or LON using the GPIB PARAMETERS switch and Table 7-6.

RS-232-C PARAMETER SELECTION

Selection of RS-232-C parameters (baud rate, parity, and line terminator) can be made at any time using the RS-232-C PARAMETER switch and Table 7-7 through Table 7-9.

Baud Rate

The selected RS-232-C baud rate establishes the baud rate used by the instrument for both sending and receiving data. Baud rates selectable are listed in Table 7-9.

When OFF LINE is selected as the baud rate, the instrument still presents an active load but does not respond to nor interfere with any bus traffic. This is useful for changing the instrument's status without turning off the oscilloscope's power.

Use Table 7-7, Table 7-8 and the PARAMETERS switch to select the desired baud rate.

Parity

The parity parameters selected determine the instrument response to received parity errors and the parity of data sent by the instrument.

Section 5 of the PARAMETERS switch determines whether or not received parity errors will cause an SRQ (see Table 7-7).

Sections 6 and 7 of the PARAMETERS switch determine the parity used when transmitting data over the bus. ODD, EVEN, MARK, or SPACE are selectable. (see Table 7-9).

Line Terminator

The line terminator can be selected to be either the carriage return (CR) or the CR and Line-Feed (LF) characters.

When CR (normal mode) is selected as the terminator, the instrument will:

- Accept only CR as the line terminator.
- Send CR as the last byte of a message.

When CR LF is selected as the terminator, the instrument will:

- Accept either CR or LF as the line terminator.
- Send Carriage Return (CR) followed by LF at the end of every message.

Section 8 of the PARAMETERS switch determines the line terminator. Select the desired line terminator using the PARAMETERS switch and Table 7-7.

MESSAGES AND COMMUNICATION PROTOCOL

Option commands can set the instrument operating mode, query the results of measurements made, or query the state of the oscilloscope. The commands are specified

in mnemonics that are related to the functions implemented. For example, the command INIt initializes instrument settings to states that would exist if the instrument's power was cycled. To further facilitate programming, command mnemonics are similar to front-panel control names.

NOTE

All measurement results returned by the options have the same accuracy as the main instrument.

Commands

Commands for this instrument, like those for other Tektronix instruments, follow the conventions established in a Tektronix Codes and Formats Standard. The command words were chosen to be as understandable as possible, while still allowing a familiar user to shorten them as much as necessary, as long as the result is not ambiguous. Syntax is also standardized to make the commands easier to learn.

In the command lists (Tables 7-13 through 7-24), headers and arguments are listed in a combination of uppercase and lowercase characters. The instrument accepts any abbreviated header or argument containing at least the characters shown in uppercase. Any characters added to the abbreviated (uppercase) version must be those shown in lowercase. For a query, the question mark must immediately follow the header. For example, any of the following formats are acceptable:

```
VMO?
VMOd?
VMOde?
```

Headers

A command consists of at least a header. Each command has a unique header, which may be all that is needed to invoke a command; e.g.,

```
INIt
OPC
```

Arguments

Some commands require the addition of arguments to their headers to describe exactly what is to be done. If there is more to the command than just the header (including the question mark if it is a query), then the header must be followed by at least one space.

In some cases, the argument is a single word; e.g.,

```
REFF REF4
PLOt STArt
```

In other cases, the argument itself requires another argument. When a second argument is required, a colon must separate the two arguments; e.g.,

```
ACQuisition REPetitive:SAMple
WFMpre XINcr:1.0E-3
```

Where a header has multiple arguments, the arguments (or argument pairs, if the argument has its own argument) must be separated by commas; e.g.,

```
DATa ENCdg:BINary,CHAnnel:CH2
VMOde? CH1,CH2,ADD
```

Default Arguments

Arguments shown within brackets ([argument]) are defaults. In any command that has a default, omitting the default argument selects the default. Do not confuse default arguments with power-up default conditions; the power-up defaults may differ from the argument default in the same function. The default argument may be sent in any command. Do not send the brackets as part of the default argument. All commands that do not have a default must always include a argument, where one or more exists.

Command Separator

It is possible to put multiple commands into one message by separating the individual commands with a semicolon; e.g.,

```
DATa ENCdg:BINary,CHAnnel:CH2;WFMpre XINcr:1.0E-3
```

Command Formatting

Commands sent to the oscilloscope must have the proper format (syntax) to be understood; however, this format is flexible in that many variations are acceptable. The following paragraphs describe this format and the acceptable variations.

The oscilloscope expects all commands to be encoded as either uppercase or lowercase ASCII characters. All data output is in uppercase.

Spaces, Carriage Returns, and Line-Feed characters are all formatting characters that can be used to enhance the readability of command sequences. As a general rule, these characters can be placed either after commas and semicolons or after the space that follows a header.

Message Terminator

As previously explained, GPIB messages may be terminated with either EOI or LF. Some controllers assert EOI concurrently with the last data byte; others use only the LF character as a terminator. The GPIB interface can be set to accept either terminator. With EOI selected, the instrument interprets a data byte received with EOI asserted as the end of the input message; it also asserts EOI concurrently with the last byte of an output message. With the LF setting, the instrument interprets the LF character without EOI asserted (or any data byte received with EOI asserted) as the end of an input message; it transmits a Carriage Return character followed by Line Feed (LF with EOI asserted) to terminate output messages.

RS-232-C messages may be terminated with either carriage return (CR) or the CR and Line-Feed (LF) characters. The RS-232-C Option can be set to accept either terminator. With CR selected, the instrument interprets a line ending in CR as the end of the input message: it also sends CR as the last byte of an output message. With the CR and LF setting, the instrument interprets either the CR character or the LF character as the end of an input message; it transmits a Carriage return character followed by a Line Feed to terminate output messages.

Numeric Arguments

Many commands have numeric arguments. The numeric arguments are shown in either <NR1>, <NR2>, or <NR3> notation. These symbols refer to the format of the numeric argument. All values must be decimal (base 10).

Table 7-12 depicts the number formats for numeric arguments in the command set. As shown in the table, both signed and unsigned numbers are accepted; but unsigned numbers are interpreted to be positive. Any command or query that has an <NR2> argument may have that argument sent to the the instrument in either <NR2> or <NR1> format. Likewise, an <NR3> argument may be sent in <NR3>, <NR2> or <NR1> format.

Table 7-12

Numeric Argument Format for Commands

Numeric Argument Symbol	Number Format	Examples
<NR1>	Integers	+1, 2, −1, −10
<NR2>	Explicit decimal point (floating point)	−3.2, +5.1, 1.2
<NR3>	Floating point in scientific notation	+1.E-2, 1.0E+2, 1.E−2, 0.02E+3

COMMAND LISTS

Tables 7-13 through 7-24 describe all commands available in the instrument equipped with either the GPIB or RS232 Option. Query and Response examples are shown in Table 7-25. The first column lists the name (or header) of the command. The capitalized letters must be present to identify the command, while those shown in lowercase are optional. The second column lists arguments that can be associated with the command. The third column lists arguments associated with the first argument. Finally, descriptions of each command and its arguments are contained in the last column.

One or more arguments, separated by commas, may be given in a query to request only the information wanted. For example: CH1? VOLts,COUpling. However, some headers in the command tables are Query only, that is, they may only be sent as queries; never as commands. The queries are listed in the same general format as command/query headers. The arguments returned by the instrument are shown in smaller type. Do not send these arguments as part of the query; they are returnable only. For example, AC, DC, or GND are returned in response to a CH1? COU.

Instrument commands are presented in tables divided into the following functional groups:

Table	Command Group	Page
7-13	Vertical Commands	7-13
7-14	Horizontal Commands	7-14
7-15	Trigger Commands	7-15
7-16	Cursors Commands	7-16
7-17	Display Commands	7-17
7-18	Acquisition Commands	7-18
7-19	Save and Recall References Commands	7-20
7-20	Waveforms Commands	7-22
7-21	Waveform Preamble Fields	7-23
7-22	Service Request Group Commands	7-25
7-23	Miscellaneous Commands	7-26
7-24	RS-232-C Specific Commands	7-26

Table 7-13
Vertical Commands

Header	Argument	Link Argument	Description
CH1?			Query only. Returns all current CH1 settings: CH1 VOL:<NR3>, COU:string;, where <NR3> is the volts/div setting and string is either AC, DC, or GND.
	VOLts	<NR3>	Query only. Returns Channel 1 volts/div reading including probe attenuation. For example: 5.0E0 is returned when the CH1 VOLTS/DIV switch is set to 50 mV and a 100X probe is attached. A warning SRQ is generated if the CH1 Variable knob is not in the calibrated position.
	COUpling	AC DC GND	Query only. Returns the current position of the CH1 INPUT COUPLING switch: CH1 COU:string;, where string is either AC, DC, or GND.
CH2?			Query only. Like CH1?, except includes an INVert query response.
	INVert	ON OFF	Query only. Returns status of CH2 INVERT switch: CH2 INV:string;, where string is either ON or OFF.
VMOde?	CH1 CH2 ADD CHOp ALT XY		Query only. Returns current state of the vertical display: VMO string;, where string is either CH1, CH2, ADD, CHOp, ALT, or XY.
PROBe?	CH1 CH2	<NR1>	Query only. Returns the probe attenuation coding: CHn PROB:<NR1>;, where n is either 1 or 2 and <NR1> is either 1000, 100, 10, 1, −1, or −2. PROBe returns −2 for unknown encoding, −1 for identify, and positive values for proper probe encoding.

Table 7-14
Horizontal Commands

Header	Argument	Link Argument	Description
HORizontal?			Query only. Returns all current Horizontal settings in the form: HOR MOD:string, ASE:<NR3>, BSE:<NR3>, EXT:string; where the MODe string is either ASWeep, AINtb, or BSWeep. The EXTclk string is either ON or OFF.
	MODe	ASWeep AINtb BSWeep	Query only. Returns the current Horizontal Mode setting in the form: HOR MOD:string; where string is either ASWeep, AINtb, or BSWeep.
	ASEcdiv	<NR3>	Query only. Returns the current A SEC/DIV setting. The <NR3> value returned is zero when the knob is set to EXT CLK.
	BSEcdiv	<NR3>	Query only. Returns an <NR3> value representing the current B SEC/DIV setting.
	HMAg	ON OFF	Query only. Returns status of Horizontal Magnifier (X10 PULL) in the form: HOR HMA:string, where string is either ON or OFF.
	EXTclk	ON OFF	Query only. Returns status of EXTclk in the form: HOR EXT:string;, where string is either ON or OFF.
DELAy?			Query only. Returns current Horizontal delay settings in the form: DELA VAL:<NR3>, UNI:string;.
	VALue	<NR3>	Query only. Returns the current DELay VALue setting in the form DELA VAL:<NR3>;, where <NR3> is the delay value returned in units indicated by the UNIts query.
	UNIts	S DIVs	Query only. Returns the current DELAy UNIts in the form: DELA UNI:string; where string is either S (seconds) or DIVs.

Table 7-15
Trigger Commands

Header	Argument	Link Argument	Description
ATRigger?			Query only. Returns current A Trigger status: ATR MOD:string, where the MODe string is either NORmal, PPAuto, or SGLswp.
	MODe	NORmal PPAuto SGLswp	Query only. Returns current A Trigger Mode setting in the form ATR MOD:string;, where string is either NORmal, PPAuto, or SGLswp. PPAuto is returned for both P-P AUTO and TV FIELD modes.
SGLswp	ARM DONe		As a query, SGLswp returns the status of the SGLswp trigger mode: SGL string;, where string is either ARM or DONe. ARM indicates that the sweep is armed or running. DONe indicates that a sweep is complete. An execution error SRQ is generated if SGL SWP is not ON. As a command, only SGLswp ARM; is legal. ARM re-arms a completed sweep. An execution warning SRQ is generated if SGL SWP is not ON or if ARM is active.
TRIggered?	ON OFF		Query only. Returns the status of the TRIG'D indicator, either TRI ON; or TRI OFF;.

Table 7-16
Cursor Commands

Header	Argument	Link Argument	Description
CURSor	SELect	CURS1 CURS2	Selects the cursor to be positioned.
	TARget	ACQuisition REF1 REF2 REF3 REF4	Selects the waveform on which cursors appear. Although the TARget waveform can be selected with either CURS1 or CURS2, both cursors will be on the last selected TARget. REF4 is the 4k reference location.
	CHAnnel	CH1 CH2	Selects active cursor channel. CHAnnel determines which channel's DELTAV or DELTAT values are returned. Cursor positioning is independent of channel.
	POSition	<NR1>	Selects the cursor screen position in the range of 0-1023 for 1024 point waveforms and 0-4095 for 4096 point waveforms. If the value is outside the defined range, the value is limited and a warning SRQ is generated.
DELTAV?	VALue	<NR3>	Query only. Returns the voltage difference between cursors: DELTAV VAL:<NR3>;. An SRQ is sent if the voltage cannot be measured. VALue is returned in PERcent if the VAR knob is uncalibrated, otherwise Volts are returned.
	UNIts	V PERcent	Query only. Indicates whether DELTAV VALue is returned in Volts or PERcent.
DELTAT?	VALue	<NR3>	Query only. Returns the time difference between cursors: DELTAT VAL:<NR3>;. An SRQ is sent if the time cannot be measured. VALue is returned in DIVs when in EXTCLK.
	UNIts	S DIVs	Query only. Indicates whether DELTAT value is returned in S (seconds) or DIVs.

Table 7-17
Display Commands

Header	Argument	Link Argument	Description
REAdout	ON OFF		Turns CRT readout ON or OFF.
MESsage	<NR1>	"string"	Command only. Writes text strings on row <NR1> of the screen. Legal values for <NR1> are 0 through 16; 1 writes to the bottom row, 16 writes to the top row, and 0 clears all messages and restores the default displays. The "string" must always be within quote marks and is displayed left justified. Long strings are truncated to approximately 40 characters. (Characters have proportional spacing.) Displaying multiple simultaneous messages may cause display flicker and may exceed display memory capacity.
PLOt	STArt		Initiates a plot via the GPIB (Option 10) or RS-232-C (Option 12) interface port, or the XY Plotter Port. While the plot is in progress all commands or queries are ignored except for PLOt ABOrt, which terminates the plot. If enabled, an OPC SRQ is sent when the plot completes.
	ABOrt		Terminates a plot in progress and returns the instrument to its previous mode. PLOt ABOrt is the only command or query the instrument responds to during a plot.
	AUTo	[ON] OFF	Turns AUTo mode ON or OFF. If AUTo is ON, each waveform is plotted after it is acquired, however, the graticule will only be plotted once, if GRAt is ON.
	GRAt	[ON] OFF	Determines if a plot will include a graticule image.
	FORmat	[XY] HPGl EPS7 EPS8 TJEt	Defines plot format and output port. FORmat reverts to XY if port is not configured for plotting. HPGl formats for HP-GLt compatible plotters. EPS7 and EPS8 format for 7 bit (low-speed, double density) and 8 bit (high-speed, double density) Epson™ format printers, respectively. TJEt formats for the Hewlett-Packard ThinkJet™ printer.
			A GPIB Controller In Charge may issue PLOt STArt to the oscilloscope, My Listen Address (MLA) to the printer or plotter, then My Talk Address (MTA) to the oscilloscope to produce a plot.
	SPEed	<NR1>	SPEed changes the analog plotter pen speed. <NR1> must be an integer from 1 through 10. Units are roughly in divisions per second.

™Epson is a trademark of Epson Corporation.
HP-GL and ThinkJet are trademarks of Hewlett-Packard Company.

Table 7-18
Acquisition Commands

Header	Argument	Link Argument	Description
STORe?	ON OFF		Query only. Returns the operating mode of the instrument; either STOR ON; for digital storage mode, or STOR OFF; for analog mode.
ACQuisition	REPetitive	SAMple ACCpeak [AVErage]	Selects the acquisition algorithm for 0.05 us/div to 2 μs/div.
	HSRec	SAMple [ACCpeak] AVErage	Selects the acquisition algorithm for 5 μs/div and 10 μs/div.
	LSRec	SAMple ACCpeak AVErage [PEAkdet]	Selects the acquisition algorithm for 0.02 ms/div to 50 ms/div.
	SCAn	SAMple ACCpeak AVErage [PEAdet]	Selects the acquisition algorithm for 0.1 sec/div to 5 sec/div, when in SCAN Display mode.
	ROLl	SAMple [PEAkdet]	Selects the acquisition algorithm for 0.1 sec/div to 5 sec/div, when in ROLL Display mode.
	CURRent	SAMple AVErage PEAkdet ACCpeak DEFault	Without the second argument, this command selects the default algorithm for the acquisition parameters that are currently active. With an argument, the command selects the specified algorithm. An SRQ is generated if the argument is not legal for the acquisition parameters that are active.
	RESet		Sets sampling modes at all sweep speeds to their default conditions.
	SMOoth	ON OFF	Applies the smoothing algorithm, when ON.
	WEIght	<NR1>	Sets the number of weighted acquisitions included in an AVErage display. The value of <NR1> must be either 1, 2, 4, 8, 16, 32, 64, 128, or 256.
	NUMsweeps	<NR1>	Sets the number of sweeps done before halting. 0 implies continuous mode (don't halt).
	TRIGCount	<NR1>	Sets the number of points before the trigger point in an acquisition. For 1k acquisitions, TRIGCount may range between 4 and 512 when in post-trigger, and 512 through 1020 when in pre-trigger. For 4k acquisitions, TRIGCount may range between 16 and 2048 when in post-trigger, and 2048 through 4080 when in pre-trigger. Resolution of <NR1> is 4.
	VECtors	ON OFF	Turns Vector Mode ON or OFF.

Table 7-18 (cont)
Acquisition Commands (cont)

Header	Argument	Link Argument	Description
ACQuisition?	SWPcount	<NR1>	Query only. Returns the number of sweeps completed, in the form: ACQ SWP:<NR1>;.
	POInts	<NR1>	Query only. Returns the number of data points in the acquisition, either 1024 or 4096, in the form: ACQ POI:<NR1>;.
	TRIGMode	PRE POSt	Query only. Returns the current trigger mode in the form: ACQ TRIGM:string;, where string is either PRE or POSt.
	SAVE	ON OFF	Query only. Returns the current state of the acquisition system in the form: ACQ SAVE:string;, where string is ON when the acquisition system has halted or is in the process of halting, or OFF.
	DISplay	ROLl SCAn	Query only. Returns the current Acquisition Display mode in the form: ACQ DIS:string;, where string is either ROLl or SCAn.

Table 7-19
Save and Recall Reference Commands

Header	Argument	Link Argument	Description
REFFrom	[ACQ] REF1 REF2 REF3 REF4 REFA . . . REFZ		Selects the waveform memory source for SAVeref commands.
SAVeref	REF1 REF2 REF3 REF4 REFA . . . REFZ		Saves the waveform selected by REFFrom in the named reference. REF1, REF2, and REF3 are used for 1024 point reference waveform storage and REF4 is for 4096 point references. 4096 point references from ACQ or REF4 may be saved as 1024 point references in REF1 through REF3. The portion of the 4096 points reference saved is determined by the position of the active cursor. 4096 point references from REFA through REFZ may NOT be saved as 1024 point references in REF1 through REF3. 1024 point references are saved as either 1024 bytes, or 2048 bytes for AVEraged waveforms.
REFDisp	REF1 REF2 REF3 REF4	ON OFF EMPty	Controls the display of the named reference. EMPty causes the contents of the reference to be deleted and its display turned OFF. REF1, REF2, and REF3, are 1024 point references, and REF4 is the 4096 point reference.
	REFA . . . REFZ	EMPty	The non-volatile references may not be displayed, only EMPtied. To display the non-volatile references, first transfer them to a numbered reference.
REFProt	REFA . . . REFZ	LOCked PERM UNLocked	Controls the write protection of non-volatile reference memories, REFA through REFZ. LOCked and PERM disable further storage into the named reference; UNLocked enables storage. PERM cannot be overwritten via front panel controls.
REFStat?	FILl	<string>	Query only. Returns a 30 character string with each reference memory's fill status indicated by a single character. <string> is ordered REF1 through REF4 followed by REFA through REFZ. Each string character is either 0, 1, 2, 4, or 8, which represents the waveform data in kilobytes.
	PROTect	<string>	Query only. Returns a 30 character string with each reference memory's protection status indicated by a single character. The order is identical to the FILl query. The characters which may make up the string are U, L, and P, which correspond to UNLocked, LOCked, and PERManently locked.
	FREe	<NR1>	Query only. Returns number of free kilobytes in the non-volatile reference memory.

Table 7-19 (cont)
Save and Recall Reference Commands (cont)

Header	Argument	Link Argument	Description
REFOrmat	TARget	REF1 REF2 REF3 REF4	Selects the reference to REFOrmat.
	CHAnnel	[CH1] CH2	Selects channel to REFOrmat. If there is no waveform for the channel (empty reference), an SRQ error is sent. If an XY waveform is selected, either channel may be selected.
	VGAin	<NR3>	Changes the vertical gain of the waveform pointed to by REFOrmat TARget. Maximum change is ±3 detents (in a 1,2,5 sequence) from the vertical gain setting of the original waveform acquisition. Cannot be used on XY waveforms.
	BASegain	<NR3>	Query only. Returns acquired vertical gain setting.
	VPOsition	<NR3>	Adjusts vertical position, relative to the original acquisition, in divisions. Valid range is ±10 divisions. Resolution is one displayed bit.
	HMAg	ON OFF	When ON, increases the horizontal gain of the waveform pointed to by REFOrmat TARget. Affects both vertical channels. Cannot be used on XY waveforms.
	MODe	CH1 CH2 ADD CHOP ALT XY	Query only. Returns originally acquired vertical mode.

Table 7-20
Waveform Commands

Header	Argument	Link Argument	Description
WAVfrm?	<string>		Query only. Response is a waveform from the oscilloscope, in the form: WFMpre <ascii string>; CURVe <string>;, which is a concatenation of the WFMpre and CURVe queries. The waveform pointed to by the DATa SOUrce and DATa CHAnnel pointers are sent in the current DATa ENCdg format.
CURVe	<Wfm Data>		The CURVe command or query is used to send or receive waveform data from the oscilloscope. The DATa SOUrce or DATa TARget pointers show where to get or put data, respectively. The DATa ENCdg pointer shows which format, HEX, BINary, or ASCii data is sent or expected. The DATa CHAnnel pointer selects either CH1 or CH2. <Wfm Data> is in the form: CURVE <Data>; where <Data> is either %<Byte Count><Binary Data><Checksum> for BINary, #H<Byte Count><Hexadecimal Data><Checksum> for HEX, or <ASCII Data> for ASCii ENCdg. For ASCii ENCdg, each data value is seperated by a comma.
DATa			Sets data parameters for data transmission and reception.
	SOUrce	REF1 REF2 REF3 REF4 [ACQ]	Selects which reference memory is source for the next WFMpre? or CURVe? query sent to the instrument. The default at power-up is ACQuisition.
	TARget	REF1 REF2 REF3 REF4	Selects which reference memory receives the next WFMpre or CURVe command sent to the instrument. The default at power-up is REF1.
	CHAnnel	[CH1] CH2	Points to the waveform that a CURVe? or WAVfrm? query will return. If there is no waveform for the CHAnnel and SOUrce selected (empty reference), an SRQ error is sent when the waveform is requested. Power-up default is CH1.
	ENCdg	ASCii [BINary] HEX	Sets the data encoding/decoding format. The default at power-up is BINary. All ENCdg formats represent an unsigned integer.

Table 7-21
Waveform Preamble Fields

<table>
<tr><th>Header</th><th>Argument</th><th>Link Argument</th><th>Description</th></tr>
<tr><td>WFMpre</td><td>WFId</td><td>"ascii str"</td><td>The WFId field includes labeling information to help you remember key features about the waveform. The information includes Vertical Mode, Coupling, Volts/Div, Time/Div, and Acquisition Mode. The scaling information is the same as in the corresponding preamble fields, but is labeled in the appropriate units. There is no command form of this argument. If received as a command, it is ignored.

The fields and their possible values for the WFId section of the preamble are:

<table>
<tr><th>Source</th><th>Chan</th><th>Cplng</th><th>Vert</th><th>Horiz</th><th>Acq-Mode</th></tr>
<tr><td>ACQ</td><td>CH1</td><td>DC</td><td>0.2MV</td><td>50ns</td><td>SMPL</td></tr>
<tr><td>REF1</td><td>CH2</td><td>AC</td><td>.</td><td>.</td><td>AVG</td></tr>
<tr><td>.</td><td>XY</td><td>GND</td><td>.</td><td>.</td><td>PKDET</td></tr>
<tr><td>.</td><td></td><td>Unknown</td><td>.</td><td>.</td><td>PKDET-SMOOTH</td></tr>
<tr><td>.</td><td></td><td></td><td>5V</td><td>5s</td><td>ACCPK</td></tr>
<tr><td>REF4</td><td></td><td></td><td>DIVS</td><td>CLKS</td><td>ACCPK-SMOOTH</td></tr>
</table></td></tr>
<tr><td></td><td>ENCdg</td><td>ASCii
[BINary]
HEX</td><td>Determines waveform encoding for waveform transmission or reception. WFMpre ENCdg and DATa ENCdg operate identically. Power-up default is BINary. All ENCdg formats represent unsigned integers.</td></tr>
<tr><td></td><td>NR.Pts</td><td><NR1></td><td>Number of points in waveform. Each point can be a single Y value (T implied), an X-Y pair, or an Max-Min pair. Although digitized record length is either 1024 or 4096 points, NR.Pts may be 256, 512, 1024, 2048, or 4096, depending on number of acquired channels, acquisition mode, whether or not smoothing is enabled.

<table>
<tr><th>Num Chn</th><th>Acquire Mode</th><th>SMOOTH ON/OFF</th><th>NR.pts to RECLEN Ratio</th></tr>
<tr><td>1</td><td>SMPL</td><td>N/A</td><td>RECLEN/1</td></tr>
<tr><td>1</td><td>AVG</td><td>N/A</td><td>RECLEN/1</td></tr>
<tr><td>1</td><td>PKDET</td><td>ON</td><td>RECLEN/1</td></tr>
<tr><td>1</td><td>ACCPK</td><td>ON</td><td>RECLEN/1</td></tr>
<tr><td>2</td><td>SMPL</td><td>N/A</td><td>RECLEN/2</td></tr>
<tr><td>2</td><td>AVG</td><td>N/A</td><td>RECLEN/2</td></tr>
<tr><td>2</td><td>PKDET</td><td>ON</td><td>RECLEN/2</td></tr>
<tr><td>2</td><td>ACCPK</td><td>ON</td><td>RECLEN/2</td></tr>
<tr><td>1</td><td>PKDET</td><td>OFF</td><td>RECLEN/2</td></tr>
<tr><td>1</td><td>ACCPK</td><td>OFF</td><td>RECLEN/2</td></tr>
<tr><td>2</td><td>PKDET</td><td>OFF</td><td>RECLEN/4</td></tr>
<tr><td>2</td><td>ACCPK</td><td>OFF</td><td>RECLEN/4</td></tr>
</table></td></tr>
</table>

Table 7-21 (cont)
Waveform Preamble Fields (cont)

Header	Argument	Link Argument	Description
WFMpre (cont)	PT.Off	<NR1>	Point offset identifies the trigger position relative to the first point of the waveform. For a 1024 point record PT.Off normally varies between 4 and 1024 in increments of 4. Normal range with 4096 point records is between 4 and 4096. NOTE: PT.Off returns a negative value if the trigger occurred before the first point of the waveform. Since a 1024 record portion of a 4096 point record can be transferred, legal values for PT.Off range from −3076 to +4096. If the value is unknown, −10000 is returned.
	PT.Fmt		Point format defines how to interpret the curve data.
		Y	Y format means that X information is implicit and that data points are Y values.
		XY	XY format means that data points are XY pairs, with X first.
		ENV	Format used for envelope waveforms. The data is sent in the form: ..., y1max, y1min, y2max, y2min,... ENV is valid for PEAkdet and ACCpeak when SMOoth is OFF.
	XUNits	S CLKs	If the argument is S, the XINcr value is in seconds. If it is CLKs, the scaling is unknown (EXTCLK).
	XINcr	<NR3>	Value gives the time interval between points (sampling rate). If <NR3> does not correspond to a legitimate time/div setting, the nearest legitimate setting is substituted and a warning SRQ is issued if EXW is ON. For a query response with an unknown time/div (i.e. EXTCLK), <NR3> is set to 1.
	YUNits	V DIV	Indicates the units associated with YMUlt.
	YMUlt	<NR3>	This value gives the vertical "step" size of the digitizer (volts between points). If <NR3> does not correspond to a legitimate volts/div setting it is treated as a "variable" setting and a warning SRQ is sent. On a query response, an unknown vertical scaling (i.e. variable) sets <NR3> to 0.04 (25 pts/div).
	YOFf	<NR1>	YOFf is the Y coordinate of ground. If ground is unknown, −10000 is returned.

Table 7-21 (cont)
Waveform Preamble Fields (cont)

Header	Argument	Link Argument	Description
WFMpre (cont)	XMUlt XOFf		XMUlt and XOFf are analogous to YMUlt and YOFf. They are used when an XY waveform is indicated. For all XY waveforms, the YUNits indicator is valid for both X and Y data. The XUNits value references sampling rate.
	BN.Fmt	RP	Binary format is always a right-justified, positive binary integer, also known as an unsigned binary integer.
	BYT/nr	<NR1>	Each data value is contained in 2 bytes for ACQuisition AVEerage or 1 byte otherwise. If 2 bytes are sent, the most sigificant byte is sent first. In HEX format, each data byte is represented by 2 ASCII encoded hex characters.
	BIT/nr	<NR1>	The data consists of 8 or 16 bits. NOTE: The least sigificant bits of a 16 bit waveform may not be valid, depending on the number of waveforms averaged.
	CRVchk	CHKsm0	CHKsm0 indicates that the last byte of a binary curve is a checksum. It is the 2's complement of the modulo 256 sum of the binary count and curve data bytes. It does not include the "CURVE %" that precedes the binary count.

Table 7-22
Service Request Group Commands

Header	Argument	Link Argument	Description
RQS	[ON] OFF		When enabled, the instrument asserts SRQ when it has an event to report. When disabled, the events are still accumulated and can be retrieved with an EVEnt? query. Default is ON with no argument and at power-up.
OPC	[ON] OFF		When enabled, the instrument asserts SRQ upon completion of certain commands. Commands that assert OPC service requests include REFTo, PLOt complete, and Self-test complete. Power-up default is OFF.
EVEnt?	<NR1>		Query only. Returns: EVE <NR1>;, where <NR1> is the oldest SRQ event held by the instrument, when multiple SRQs exist. If no error is pending, 0 is returned.

Table 7-23
Miscellaneous Commands

Header	Argument	Link Argument	Description
ID?	<string>		Query only. Returns: ID <string>; where <string> is TEK/2230, V81.1, VERS:xx. "xx" is the firmware revision number of the instrument.
HELp?	<string>		Query only. Returns a list of all valid command headers available in the instrument.
INIt			Command only. Causes the instrument to go to an initialized state equivalent to power-on.
LONg	[ON] OFF		When LONg is ON, all queries respond with the full length versions of commands. When LONg is OFF, the shortest acceptable version of commands are used in query responses. Default argument is ON. At power-up, LONg is OFF.
SET?	<string>		Query only. Returns an ASCII string that reflects the current instrument state. The returned string can be sent to the instrument to recreate that state. In order to comply with Codes and Formats, SET? does not respond with its header. NOTE: This query has very limited capability because only settable values are returned in response to the SET? query. The status of LONg affects the length of the response to the SET? query.

Table 7-24
RS-232-C Specific Commands

Header	Argument	Link Argument	Description
REMote	[ON] OFF		REMote must be ON in order to change the state of the instrument. REMote is similar to the GPIB Remote Enable (REN) and Go To Local (GTL) messages.
STOp	1 2		Selects the number of stop bits.
FLOw	[ON] OFF		Enables and disables DC1/DC3 flow control. When FLOw is ON, BINary data transfers cannot be made. Omitting the argument turns FLOw ON. Power-on default is OFF.
STAtus?	<NR1>		Query only. Returns the current status byte in the same manner as a GPIB Serial Poll.

Table 7-25
Query and Response Examples

QUERY	RESPONSE
Vertical Query Examples	
CH1? VOL	CH1 VOL:0.5E0;
CH2?	CH2 VOL:10.0E−3,COU:AC,INV:OFF;
VMO?	VMO ADD;
CH1? VOL	CH1 VOL:5.0E-3;
PROB?	PROB CH1:10,CH2:1;
Horizontal Query Examples	
HOR?	HOR MOD:ASW,ASE:2.0E-6, BSE:5.0E−9,HMA:OFF,EXT:OFF;
DELA?	DELA VAL:2.45E-3,UNI:S;
Trigger Query Examples	
ATR?	ATR MOD:PPA;
ATR? MOD	ATR MOD:NOR;
SGL?	SGL DON;
TRI?	TRI ON;
Cursor Query Examples	
CURS? TAR	CURS TAR:REF2;
CURS?	CURS SEL:CURS1,TAR:REF2, CHA:CH1,POS:765;
DELTAT?	DELTAT VAL:11.5E-6,UNI:S;
Acquisition Query Examples	
ACQ? HSR	ACQ HSR:AVE;
ACQ?	ACQ REP:AVE,HSR:SAM,LSR:PEA, SCA:SAM,ROL:PEA,SMO:ON,WEI:8, SWP:6,NUM:0,POI:4096,TRIGM:PRE, TRIGC:320,SAVE:OFF,DIS:SCA,VEC:ON;
Save and Recall Reference Query Examples	
REFO? VGA	REFO VGA:10.0E-3;
REFO?	REFO TAR:REF1,CHA:CH2,VGA:10.0E-3, VPO:0.0,HMA:ON,MODE:CHOP;

Table 7-25 (cont)
Query and Response Examples

QUERY	RESPONSE
Waveform Query Examples	
WFM? WFI	WFM WFI:"REF1,CH1,10.0MV,DC, 50.0MS,SAMPLE-SMOOTH,CRV# 4";
WFM? PT.F	WFM PT.F:ENV;
WFM? ENC	WFM ENC:ASC;

WAVEFORM TRANSFERS

The instrument can transmit and receive waveforms. It can transfer these waveforms, in binary, hexadecimal, or ASCII format. When sending waveforms to the instrument, the target is a reference memory. Waveforms transferred from the oscilloscope to the controller are selected from the same reference memories or the current acquisition. The data source and data target are selected independently.

Waveform Preamble

The waveform preamble indicates the waveform attributes, such as number of points per waveform, scale factors, offset, horizontal increment, scaling units, and data encoding. The preamble information is sent as an ASCII string. The length of the string depends on the characteristics of the waveform.

A typical response to the preamble query WFMpre? for a Y (time implied) acquisition is:

Query	Response
WFMpre?	WFM WFI:"ACQ, CH1, 0.5V, DC, 0.2MS, SAMPLE - SMOOTH, CRV# 2", NR.P:4096, PT.O:122, PT.F:Y, XMU:0.0E0, XOF:0, XUN:S, XIN:2.0E-6, YMU:20.0E-3, YOF:-20, YUN:V, ENC:HEX, BN.F:RP, BYT:1, BIT:8, CRV:CHK;

A typical response to the preamble query WFMpre? for an XY acquisition is:

Query	Response
WFMpre?	WFM WFI:"ACQ, XY, 0.2V, DC, 50.0MV, DC, 1.0US, SAMPLE, CRV# 19", NR.P:2048, PT.O:216, PT.F:XY, XMU:8.0E-3, XOF:0, XUN:S, XIN:20.0E-9, YMU:2.0E-3, YOF:0, YUN:V, ENC:BIN, BN.F:RP, BIT:8, BYT:1, CRV:CHK;

In these examples, the instrument response is shown on multiple lines. WFMpre? responses, as well as all other query responses, are sent as a single line of data ending with a carriage return line feed. With the GPIB interface, EOI is also sent if that message terminator mode is selected.

Transferring Waveforms

The oscilloscope can respond with either the Preamble only, Curve only, or both Preamble and Curve together:

Query	Response
CURVe?	Curve Data Only
WFMpre?	Preamble Only
WAVfrm?	Preamble and Curve data

When responding to the WAVfrm? query, the preamble is separated from the curve data with a ";".

The instrument digitizes data internally as an 8-bit, unsigned integer. Before data is sent over the GPIB or RS-232-C Option, it is changed into one of three formats,

BINary, HEXADECIMAL, or ASCii. The resolution of data points sent over the bus may be either 8 or 16 bits. Waveform record length is 1024 or 4096, but the number of data points per record depends on several variables. See the description of NR.Pts in the Command Tables for more information.

Binary Encoding

BINary data is transferred as an unsigned binary integer. Each record is 8 bits, or 16 bits when averaged.

In BINary format, the waveform curve data is in the form of: CURVE <space> % <Binary Count MSB> <Binary Count LSB> <Data> <Checksum> <Terminator>

Where:

%	is used as a header character to show the start of a binary block.
<Binary Count MSB>	is the most significant byte of the two-byte Binary Count. Binary Count is the length of the waveform, in bytes, plus the one byte Checksum.
<Binary Count LSB>	is the least significant byte of the Binary Count.
<Data>	is made up of 256, 512, 1024, 2048 or 4096 data points. Each data point is either a 1 byte (8-bit) or 2 byte (16-bit) representation of each digitized value.
<Checksum>	is the two's-complement of the modulo 256 sum of the preceding data bytes and the binary count. The Checksum is used by the controller to verify that all data values have been received correctly.

Table 7-26 shows an example of data sent over the interface during a 4096 point, 8-bit BINary waveform transfer. The actual waveform point (Pt.) values will vary depending upon the signal acquired.

Table 7-27 shows an example of data sent over the interface during a 4096 point, 16-bit BINary waveform transfer.

Table 7-26
Typical 8-Bit Binary Waveform Data

Byte	Contents	Decimal	GPIB EOI (1=Asserted)
1	C	67	0
2	U	85	0
3	R	82	0
4	V	86	0
5	E	69	0
6	<SP>	32	0
7	%	37	0
8	<Bin Count MSB>	16[a]	0
9	<Bin Count LSB>	01[a]	0
10	1st Pt	d_1	0
11	2nd Pt	d_2	0
.	.	.	0
.	.	.	0
.	.	.	0
4105	4096th Pt	d_{4096}	0
4106	<Checksum>	chk	1 When TERM=EOI
4107[b]	<CR>	13	0
4108[c]	<LF>	10	1

[a] (1001_{16} or 4097_{10})

[b] All RS-232-C or GPIB with TERM = LF/EOI.

[c] RS-232-C with TERM = CR-LF.

Hexadecimal Encoding

In HEXadecimal waveform encoding, characters representing an 8-bit or 16-bit data point are sent in a fixed ASCII hexadecimal format. There are no delimiters between data points. Data format is very similar to BINary format, with the following exceptions:

1. The curve header is "CURVE #H" instead of "CURVE %".

2. Each data point is 2 ASCII hexadecimal characters for 8-bit and 4 ASCII hexadecimal characters for 16-bit transfers.

Table 7-27
Typical 16-Bit Binary Waveform Data

Byte	Contents	Decimal	GPIB EOI (1=Asserted)
1	C	67	0
2	U	85	0
3	R	82	0
4	V	86	0
5	E	69	0
6	<SP>	32	0
7	%	37	0
8	<Bin Count MSB>	32[a]	0
9	<Bin Count LSB>	01[a]	0
10	1st Pt MSB	d_{1H}	0
11	1st Pt LSB	d_{1L}	0
12	2nd Pt MSB	d_{2H}	0
13	2nd Pt LSB	d_{2L}	0
.	.	.	0
.	.	.	0
.	.	.	0
8200	4096th Pt MSB	d_{4096H}	0
8201	4096th Pt LSB	d_{4096L}	0
8202	<Checksum>	chk	1 When TERM=EOI
8203[b]	<CR>	13	0
8204[c]	<LF>	10	1

[a] (1001_{16} or 4097_{10})

[b] All RS-232-C or GPIB with TERM = LF/EOI.

[c] RS-232-C with TERM = CR-LF.

3. The byte count is sent as four successive ASCII hexadecimal characters, but the value of the byte count is identical to a comparable BINary transfer.

4. The checksum is sent as two successive ASCII hexadecimal characters.

Table 7-28 and Table 7-29 show 8-bit and 16-bit HEXadecimal waveform CURVe structures.

Table 7-28
Typical 8-Bit Hexadecimal Waveform Data

Byte	Contents	Decimal	GPIB EOI (1=Asserted)
1	C	67	0
2	U	85	0
3	R	82	0
4	V	86	0
5	E	69	0
6	<SP>	32	0
7	#	35	0
8	H	72	0
9	<Bin Count MS 4 bits>	49	0
10	.	48	0
11	.	48	0
12	<Bin Count LS 4 bits>	49	0
13	1st Pt MS 4 bits	d_{1H}	0
14	1st Pt LS 4 bits	d_{1L}	0
15	2nd Pt MS 4 bits	d_{2H}	0
16	2nd Pt LS 4 bits	d_{2L}	0
.	.	.	0
.	.	.	0
.	.	.	0
203	4096th Pt MS 4 bits	d_{4096H}	0
204	4096th Pt LS 4 bits	d_{4096L}	0
205	<Checksum MS 4 bits>	chk_H	0
206	<Checksum LS 4 bits>	chk_L	1 When TERM=EOI
207[a]	<CR>	13 (If term =LF/EOI)	0
208[b]	<LF>	10 (If term =CR-LF)	1

[a] All RS-232-C or GPIB with TERM = LF/EOI.

[b] RS-232-C with TERM = CR-LF.

ASCII Encoding

In ASCii encoding, ASCII characters representing the binary value of each data point are sent in variable length format, separated by commas.

Table 7-29
Typical 16-Bit Hexadecimal Waveform Data

Byte	Contents	Decimal	GPIB EOI (1=Asserted)
1	C	67	0
2	U	85	0
3	R	82	0
4	V	86	0
5	E	69	0
6	<SP>	32	0
7	#	35	0
8	H	72	0
9	<Bin Count MS 4 bits>	50	0
10	.	48	0
11	.	48	0
12	<Bin Count LS 4 bits>	49	0
13	1st Pt MS 4 bits	d_{1H}	0
14	.	.	0
15	.	.	0
16	1st Pt LS 4 bits	d_{1L}	0
17	2nd Pt MS 4 bits	d_{2H}	0
18	.	.	0
19	.	.	0
20	2nd Pt LS 4 bits	d_{2L}	0
.	.	.	0
.	.	.	0
.	.	.	0
6393	4096th Pt MS 4 bits	d_{4096H}	0
6394	.	.	0
6395	.	.	0
6396	4096th Pt LS 4 bits	d_{4096L}	0
6397	<Checksum MS 4 bits>	chk_H	0
6398	<Checksum LS 4 bits>	chk_L	1 When TERM=EOI
6399[a]	<CR>	13 (If term =LF/EOI)	0
6400[b]	<LF>	10 (If term =LF/EOI)	1

[a]All RS-232-C or GPIB with TERM = LF/EOI.

[b]RS-232-C with TERM = CR-LF.

In ASCII format, the curve data transfer is represented as:

CURVE<space>data,data,data,...,data<terminator>

Table 7-30 shows an example of an 8-bit ASCii waveform CURVe transfer. Transmission length depends on specific data values, record length, acquisition mode and smoothing, and whether the acquisition was 1 or 2 channels.

REMOTE-LOCAL OPERATING STATES

The following paragraphs describe the two operating states of the instrument: Local and Remote.

Table 7-30
Typical ASCII Waveform Data

Byte	Contents	Decimal	GPIB EOI (1=Asserted)
1	C	67	0
2	U	85	0
3	R	82	0
4	V	86	0
5	E	69	0
6	<SP>	32	0
7	$Pt^{100}{}_1$*	$d^{100}{}_1$	0
8	$Pt^{10}{}_1$*	$d^{10}{}_1$	0
9	$Pt^{1}{}_1$*	$d^{1}{}_1$	0
10	.	44	0
.	.	.	0
.	.	.	0
.	.	.	0
XXX	$Pt^{100}{}_{4096}$*	$d^{100}{}_{4096}$	0
XXX	$Pt^{10}{}_{4096}$	$d^{10}{}_{4096}$	0
XXX	$Pt^{1}{}_{4096}$*	$d^{1}{}_{4096}$	0
XXX[a]	<CR>	13	0
XXX[b]	<LF>	10	1

* Pt^{100} and Pt^{10} values are NOT sent when 0, so each Pt may be 1, 2, or 3 digits.

[a]All RS-232-C or GPIB with TERM = LF/EOI.

[b]RS-232-C with TERM = CR-LF.

Local State (LOCS)

In LOCS, instrument parameters are both set and changed manually by operator manipulation of the front- and side-panel controls. Only option interface messages can be received and executed. Device-dependent commands (without REN asserted) will cause SRQ errors since their functions are under front-panel control while in LOCS.

Remote State (REMS)

In this state, the oscilloscope executes all commands addressed to it over the communication options bus. Front-panel indicators and crt readouts are updated as applicable when commands are executed. Manually changing any option-controllable front-panel control causes the instrument to return to the Local State. If a waveform is being transmitted over the bus, the PLOT indicator is lit and acquisitions are prevented until the transmission is complete.

INSTRUMENT RESPONSE TO INTERFACE MESSAGES

The following explains effects on the oscilloscope of standard interface messages received from a remote controller. Message abbreviations used are from ANSI/IEEE Std 488-1978.

Local Lockout (LLO)

Local Lockout is not supported by the instrument. In response to a LLO message via the GPIB, the option generates an SRQ error.

NOTE

The RS-232-C Option uses Option Interface Commands to implement the following GPIB (hardware) messages.

Remote Enable (REN)

When Remote Enable is asserted and the instrument receives its listen address, the oscilloscope is placed in the Remote State (REMS). When in the Remote State, the oscilloscope's Addressed (ADDR) indicator is lit.

Disasserting REN causes a transition to LOCS; the instrument remains in LOCS as long as REN is false. The transition may occur after processing of a different message has begun. In this case, execution of the message being processed is not interrupted by the transition.

Go To Local (GTL)

Instruments that are already listen-addressed respond to GTL by assuming a local state. Remote-to-local transitions caused by GTL do not affect the execution of any message being processed when GTL was received.

My Listen and My Talk Addresses (MLA and MTA)

The primary Talk/Listen address is established as previously explained in this section.

Unlisten (UNL) and Untalk (UNT)

When the UNL message is received, the oscilloscope's listen function is placed in an idle (unaddressed state). In the idle state, the instrument will not accept commands over the bus.

The talk function is placed in an idle state when the oscilloscope receives the UNT message. In this state, the instrument cannot transmit data via the interface bus.

Interface Clear (IFC)

When IFC is asserted, both the Talk and Listen functions are placed in an idle state and the crt ADDR indicator is turned off. This produces the same effect as receiving both the UNL and the UNT messages.

Device Clear (DCL)

The DCL message reinitializes communication between the instrument and the controller. In response to DCL, the instrument clears any input and output messages as well as any unexecuted control settings. Also cleared are any errors and events waiting to be reported (except the power-on event). If the SRQ line is asserted for any reason (other than power-on), it becomes unasserted when the DCL message is received.

Selected Device Clear (SDC)

This message performs the same function as DCL; however, only instruments that have been listen-addressed respond to SDC.

Serial Poll Enable and Disable (SPE and SPD)

The Serial Poll Enable (SPE) message causes the instrument to transmit its serial-poll status byte when it is talk-addressed. The Serial Poll Disable (SPD) message switches the instrument back to its normal operation.

GPIB PROGRAMMING

Programming considerations are provided in this part to assist in developing programs for interfacing to the oscilloscope via the GPIB. For additional information see the "Instrument Interfacing Guide". Before a program can be used for controlling the oscilloscope, the GPIB parameters (primary address, message terminator, and talk/listen mode) must be set. These parameters are selected and set at the oscilloscope using the GPIB PARAMETERS switch.

Programs are usually composed of two main parts (or routines), which can be generally categorized as a command handler and a service-request handler.

Command Handler

Basically, a command handler should establish communication between the controller and oscilloscope, send commands and queries to the oscilloscope, receive responses from the oscilloscope, and display responses as required. The following outline indicates the general sequence of functions that the command-handling routine should perform to accommodate communications between the controller and oscilloscope over the GPIB.

1. Initialize the controller.

2. Disable the service-request handler until the program is ready to handle them.

3. Get the GPIB address of the oscilloscope.

4. Enable the service-request handler.

5. Get the command to send to the oscilloscope.

6. Send the command to the oscilloscope.

7. Check for a response from the oscilloscope.

8. If there is a response, perform the desired function.

9. You are ready for a new command. Repeat the functions in statements 5 through 9 as many time as desired.

Service-Request Handler

The typical service-request handler routine contains the necessary instructions to permit proper processing of interrupts. For example, whenever power-on occurs, the oscilloscope asserts an SRQ interrupt. If a GPIB program is operating on the controller when a power-on SRQ is received, the program should be able to determine that the oscilloscope's power was interrupted at some time during program operation. This event could cause improper program execution, unless the program was written to adequately handle the possibility of a power-on SRQ occurring.

Other interrupts (or events) for which the oscilloscope asserts SRQ are identified in Table 7-32.

While some controllers have the capability of ignoring service requests, others require that all SRQs be managed. The programmer should understand the controller being used. If service requests are to be handled in the program, the interrupts must first be enabled.

A service-request handler routine can be developed to service interrupts when they occur during program operation. It basically should consist of an interrupt-enabling statement (ON SRQ) near the beginning of the program and a serial-poll subroutine somewhere in the program. The ON SRQ statement directs program control to the serial-poll subroutine whenever an SRQ interrupt occurs. For each interrupt received by the controller, the program should perform a serial-poll subroutine.

The following general steps are required to handle service requests from the oscilloscope:

1. Perform a serial poll.

2. Send an EVENT? query to the oscilloscope requesting service.

3. If the EVENT? query response is not zero, then perform the desired response to the event.

4. Return to the main program.

RS-232-C PROGRAMMING

Programming considerations are provided in this part to assist in developing programs for interfacing to the oscilloscope via the RS-232-C. For additional information see the

"Instrument Interfacing Guide". Before a program can be used for controlling the oscilloscope, the RS-232-C parameters (baud rate, line terminator, and parity) must be set. These parameters are selected and set at the oscilloscope using the RS-232-C PARAMETERS switch.

Programs are usually composed of two main parts (or routines), which can be generally categorized as a command handler and a service-request handler.

Command Handler

Basically, a command handler should establish communication between the controller and oscilloscope, send commands and queries to the oscilloscope, receive responses from the oscilloscope, and display responses as required. The following outline indicates the general sequence of functions that the command-handling routine should perform to accommodate communications between the controller and oscilloscope.

1. Initialize the controller.

2. Check for a service request from the oscilloscope (by sending an EVEnt query); if not zero, service the request.

3. Get the command to send to the oscilloscope.

4. Send the command to the oscilloscope.

5. Check for a response from the oscilloscope.

6. If there is a response, perform the desired function. If there is also an error response, perform step 2.

7. You are ready for a new command. Repeat the functions in statements 2 through 7 as many time as desired.

Service-Request Handler

The typical service-request handler routine contains the necessary instructions to permit proper processing of service requests. For example, whenever power-on occurs, the oscilloscope sends an SRQ. If a GPIB program is operating on the controller when a power-on SRQ is generated, the program should be able to determine that the oscilloscope's power was interrupted at some time during program operation. This event could cause improper program execution, unless the program was written to adequately handle the possibility of a power-on SRQ occurring. Other events for which the oscilloscope generates SRQ are identified in Table 7-32.

The following general steps are required to handle service requests from the oscilloscope:

1. Send an EVENT? query to the oscilloscope requesting service.

2. If the EVENT? query response is not zero, then perform the desired response to the event.

3. Return to the main program.

RESET UNDER COMMUNICATION OPTIONS CONTROL

The oscilloscope may be set to its power-up state by sending the INIt command via the communication option. This command always initiates the power-up self tests. On completion of power-up tests, SRQ code 65 (operation complete) is generated, and the oscilloscope enters the normal operating state. If there is a self-test error, the option also generates SRQ code 65 and does not shift the instrument to the normal operating state. Invoking the INIt command can simplify a program. When using INIt, fewer commands will usually be needed to set the instrument state, since all front-panel settings may not need to be individually specified.

STATUS AND ERROR REPORTING

The status and error reporting system used by the Communication Options interrupts the bus controller. On the GPIB Option, the bus controller is interrupted by asserting the Service Request (SRQ) line on the bus. This SRQ provides the means of indicating that an event (either a change in status or an error) has occurred. To service a request, the GPIB controller performs a Serial Poll; in response, the instrument returns a Status Byte (STB), which indicates the type of event that occurred. On the RS-232-C Option, as soon as a change of status or an error occurs, the instrument returns a Status Byte (STB), which indicates the type of event that occurred. Bit 4 of the Status Byte is used to indicate that the command processor is active. This bit is set when the command processor is executing a command, and reset when it is not. The Status Byte, therefore, provides a limited amount of information about the specific cause of the SRQ. The various status events and errors that can occur are divided into several categories as defined in Table 7-31.

Each time the GPIB controller performs a serial poll, it can cause a second SRQ if more than one error exists. The most serious error at the time of the serial poll is the error reported. An EVEnt? query returns a number indicating the specific type of error that occurred. Table 7-32 lists the EVEnt? codes generated by the communication options.

Table 7-32

Event Codes

EVEnt? Code	Instrument Status
000	No status to report
	Command Errors
101	Command header error.
102	Header delimiter error.
103	Command argument error.
104	Argument delimiter error.
105	Non-numeric argument, numeric expected.
106	Missing argument.
107	Invalid message-unit delimiter.
108	Checksum error.
109	Byte-count error.
151	The argument is too large.
152	Illegal hex character.
153	Non-binary argument; binary or hex expected.
154	Invalid numeric input.
155	Unrecognized argument type.
	Execution Errors
201	Command cannot be executed when in LOCAL.
203	I/O buffers full, output dumped.
205	Argument out of range, command ignored.
206	Group execute trigger ignored.
251	Illegal command.
252	Integer overflow.
253	Input buffer overflow.
254	Invalid waveform preamble.
255	Invalid instrument state.
256	GPIB (Option 10) Command not allowed.
258	Command not allowed on a 2220.
259	Command not allowed on a 2230.
260	Cannot execute command with RQS OFF.
261	Reference memory busy with local (front-panel) command.
262	Reference memory non-existent or specified as different size than selected waveform.
263	Plot active; only PLOT ABORT allowed while plotting.
	Internal Errors
351	Firmware failure. Contact your nearest Tektronix Service Center for assistance.

Table 7-32 (cont)

EVEnt? Code	Instrument Status
	System Events
401	Power on.
451	Parity error.
452	Framing error.
453	Carrier lost.
454	End of acquisition OPC.
455	End of plot OPC.
456	Diagnostics test complete OPC.
	Execution Warnings
551	Single sweep is already armed.
552	No ground-dot measurement available.
553	Invalid probe code or identify.
554	Query not valid for current instrument state.
555	Requested setting is out of detent (uncalibrated).
556	MESsage display buffer is full.
557	Waveform preamble incorrect, has been corrected.
558	Waveform transfer ended abnormally.

Table 7-33
Readout/MESage Command Character Set

BITS B7 B6 B5 / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		SYMBOLS		UPPERCASE		LOWERCASE	
0 0 0 0	0 0	10 T 16	20 SP 32	30 0 48	40 @ 64	50 P 80	60 ` 96	70 p 112
0 0 0 1	1 1	11 17	21 ! 33	31 1 49	41 A 65	51 Q 81	61 a 97	71 q 113
0 0 1 0	2 BWL 2	12 18	22 " 34	32 2 50	42 B 66	52 R 82	62 b 98	72 r 114
0 0 1 1	3 ⊠ 3	13 19	23 # 35	33 3 51	43 C 67	53 S 83	63 c 99	73 s 115
0 1 0 0	4 Δ 4	14 20	24 $ 36	34 4 52	44 D 68	54 T 84	64 d 100	74 t 116
0 1 0 1	5 — 5	15 μ 21	25 % 37	35 5 53	45 E 69	55 U 85	65 e 101	75 u 117
0 1 1 0	6 = 6	16 Ṽ 22	26 & 38	36 6 54	46 F 70	56 V 86	66 f 102	76 v 118
0 1 1 1	7 ⏚ 7	17 ↓ 23	27 ' 39	37 7 55	47 G 71	57 W 87	67 g 103	77 w 119
1 0 0 0	8 8	18 24	28 (40	38 8 56	48 H 72	58 X 88	68 h 104	78 x 120
1 0 0 1	9 9	19 25	29) 41	39 9 57	49 I 73	59 Y 89	69 i 105	79 y 121
1 0 1 0	A 10	1A 26	2A * 42	3A : 58	4A J 74	5A Z 90	6A j 106	7A z 122
1 0 1 1	B 11	1B 27	2B + 43	3B ; 59	4B K 75	5B [91	6B k 107	7B { 123
1 1 0 0	C 12	1C 28	2C , 44	3C < 60	4C L 76	5C \ 92	6C l 108	7C ¦ 124
1 1 0 1	D 13	1D 29	2D - 45	3D = 61	4D M 77	5D] 93	6D m 109	7D } 125
1 1 1 0	E Hz 14	1E 30	2E . 46	3E > 62	4E N 78	5E ^ 94	6E n 110	7E ~ 126
1 1 1 1	F ⅛ 15	1F 31	2F / 47	3F ? 63	4F O 79	5F — 95	6F o 111	7F 127

Table 7-34
ASCII Code Chart

B7 B6 B5 / BITS / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0 0	20 DLE 10 16	40 SP 20 32	0 60 30 48	100 @ 40 64	0 120 P 50 80	140 ` 60 96	0 160 p 70 112
0 0 0 1	1 GTL SOH 1 1	21 LLO DC1 11 17	41 ! 21 33	1 61 1 31 49	101 A 41 65	1 121 Q 51 81	141 a 61 97	1 161 q 71 113
0 0 1 0	2 STX 2 2	22 DC2 12 18	42 " 22 34	2 62 2 32 50	102 B 42 66	2 122 R 52 82	142 b 62 98	2 162 r 72 114
0 0 1 1	3 ETX 3 3	23 DC3 13 19	43 # 23 35	3 63 3 33 51	103 C 43 67	3 123 S 53 83	143 c 63 99	3 163 s 73 115
0 1 0 0	4 SDC EOT 4 4	24 DCL DC4 14 20	44 $ 24 36	4 64 4 34 52	104 D 44 68	4 124 T 54 84	144 d 64 100	4 164 t 74 116
0 1 0 1	5 PPC ENQ 5 5	25 PPU NAK 15 21	45 % 25 37	5 65 5 35 53	105 E 45 69	5 125 U 55 85	145 e 65 101	5 165 u 75 117
0 1 1 0	6 ACK 6 6	26 SYN 16 22	46 & 26 38	6 66 6 36 54	106 F 46 70	6 126 V 56 86	146 f 66 102	6 166 v 76 118
0 1 1 1	7 BEL 7 7	27 ETB 17 23	47 ' 27 39	7 67 7 37 55	107 G 47 71	7 127 W 57 87	147 g 67 103	7 167 w 77 119
1 0 0 0	10 GET BS 8 8	30 SPE CAN 18 24	50 (28 40	8 70 8 38 56	110 H 48 72	8 130 X 58 88	150 h 68 104	8 170 x 78 120
1 0 0 1	11 TCT HT 9 9	31 SPD EM 19 25	51) 29 41	9 71 9 39 57	111 I 49 73	9 131 Y 59 89	151 i 69 105	9 171 y 79 121
1 0 1 0	12 LF A 10	32 SUB 1A 26	52 * 2A 42	10 72 : 3A 58	112 J 4A 74	10 132 Z 5A 90	152 j 6A 106	10 172 z 7A 122
1 0 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	11 73 ; 3B 59	113 K 4B 75	11 133 [5B 91	153 k 6B 107	11 173 { 7B 123
1 1 0 0	14 FF C 12	34 FS 1C 28	54 , 2C 44	12 74 < 3C 60	114 L 4C 76	12 134 \ 5C 92	154 l 6C 108	12 174 | * 7C 124
1 1 0 1	15 CR D 13	35 GS 1D 29	55 - 2D 45	13 75 = 3D 61	115 M 4D 77	13 135] 5D 93	155 m 6D 109	13 175 } 7D 125
1 1 1 0	16 SO E 14	36 RS 1E 30	56 . 2E 46	14 76 > 3E 62	116 N 4E 78	14 136 ^ 5E 94	156 n 6E 110	14 176 ~ 7E 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 2F 47	15 77 UNL ? 3F 63	117 O 4F 79	15 137 UNT — 5F 95	157 o 6F 111	15 177 DEL (RUBOUT) 7F 127
	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS (PPE)	(PPD)

KEY

octal / hex: 25 PPU / NAK / 15 21 — GPIB code / ASCII character / decimal

*| on some keyboards or systems

4999-103

OPTION 10
THEORY OF OPERATION

The General Purpose Interface Bus (GPIB) option (see Diagram 24) provides a general purpose interface for the exchange of waveform data and instrument-state information. It retains the XY Plotter function of the base instrument, and provides a means of adding non-volatile waveform memory.

The XY Plotter circuitry is unchanged from the standard instrument. The circuit descriptions covering the standard XY Plotter still apply, and are not repeated here. The following discussion refers only to the GPIB portion of the board.

The board contains 64K bytes of ROM, 2K bytes of RAM, and an interface to the GPIB port. Supporting the GPIB port are two 8-bit input ports for status signals and parameter switches, and a 1-bit output port used for diagnostics. The remainder of the circuitry provides signal buffering and address decoding.

The microprocessor bus extends to this option through W8101. The address bus, the data bus, the bus control signals, and several address decode lines which are generated on the storage board are included. Power supplies are also brought in through this connector, and J9301 in the XY Plotter portion of the board is not used.

Bus Buffers

The address lines are buffered by U1341 and U1333. The buffers are always enabled. Bidirectional data bus buffer U1331 isolates the circuitry from the storage board and provides improved signal drive capability. Also buffered are the $\overline{RD}$, $\overline{WR}$, 6.7MHZCLK, and RESET signals.

Address Decoding

The GPIB occupies all of the addresses in the COM-SEG range (80000H to BFFFFH). Its I/O occupies several addresses in the I/O-SEG range (40000H to 7FFFFH). Table 3-1 lists the actual addresses used.

Primary address decoding is accomplished by U1345. It provides a one-of-eight, active-LO signal when BA12, BA13, $\overline{IO\ SEG}$, and $\overline{BLK0}$, are all LO. Three address lines, BA3, BA6, and BA7, are decoded to produce the eight strobes. Four of the strobes enable the GPIB controller U1351, Parameter buffer U1322, Status buffer U1323, and Diagnostic latch U1335. Also generated by U1345 is a signal that is LO whenever one of the strobes is enabled and BA8 is LO. This signal is gated with $\overline{COM\ SEG}$ and $\overline{DEN}$ in U1332 to produce an enable for data buffer U1331 via U1344C.

Half of U1332 generates the ROM enable signal. The ROM is enabled whenever $\overline{COM\ SEG}$ is LO and either $\overline{BLK0}$ or $\overline{BLK1}$ is LO. This enable drives the output enable (pin 22) of U1343 and not its chip enable (pin 20) which is driven by $\overline{A18}$.

The other half of U1332 generates the $\overline{DATEN}$ enable for the data bus buffer. When $\overline{DEN}$ is LO and either $\overline{I/O\ 2OPT}$ or $\overline{COM\ SEG}$ is LO, pin 8 of U1332 goes HI. U1344 inverts this signal, producing $\overline{DATEN}$. The data bus buffer is enabled only for references in COM SEG or to I/O ports used by this option.

The RAM enable signal $\overline{RAMEN}$ (U1334A pin 3) is produced by U1334A and U1334C. RAM enable $\overline{RAMEN}$ is LO only if RAM DIS, $\overline{BLK3}$, and $\overline{COM\ SEG}$ are all LO. RAM DIS disables U1342 if the non-volatile RAM is present.

RAM and ROM

Temporary storage for the option is provided by RAM U1342. Option operating system firmware is contained in ROM U1343.

GPIB Controller

The GPIB controller, U1351, is a TMS9914A which handles much of the protocol required to interface to the IEEE STANDARD 488 bus. The controller has eight internal registers decoded by RS0, RS1, and RS2. Under certain conditions it generates an interrupt to the microprocessor which appears as a LO $\overline{INT}$ (U1351 pin 9). This pin is an open drain output connected to the microprocessor's maskable interrupt.

Data bus lines are reversed, BD0 for BD7, to accommodate the internal convention of the GPIB controller.

Trigger signal TR, U1351 pin 39, is used only for diagnostics and is read by the microprocessor via U1322 pin 2.

Line Drivers

Bus buffers U1324 and U1325 provide the drive characteristics required by IEEE 488 bus standards. They also control characteristics of the drive circuitry during bus operation.

All of the signal lines that are at GPIB levels are protected by diode arrays CR1321, CR1322, and zener diode VR1321. These networks clip voltage transients greater than +6.8 volts or less than −0.6 volts.

Connector J1314 is a standard GPIB interface connector.

Clock Divider and Diagnostic Latch

U1335 is a dual J-K flip-flop that performs two independent functions. U1335A divides the 6.7 MHz clock by two for GPIB controller U1351. U1335B provides a one-bit latch for diagnostic use. When its enable (clock), U1335B pin 12, is strobed LO, the data on BD0 is latched.

Parameter Buffer

Parameter buffer U1322 provides an eight-bit input port for selecting parameters associated with the GPIB option such as address and terminator. It consists of U1322, S1321, and part of resistor pack R1322. The switch is sensed by enabling buffer U1322 which gates its inputs onto the data bus. Bit 7 is used to sense TR, U1351 pin 39, for diagnostic use.

Status Buffer

Status buffer U1323 is used to sense three of the GPIB PARAMETER switch positions as well as miscellaneous other signals. Buffer circuitry consists of U1323, S1321, R1321, and part of resistor pack R1322. Status buffer functions are shown in Table 7-35.

Table 7-35

GPIB Status Buffer Functions

BIT	Signal Name	Function
Bit 0	$\overline{\text{PWR INT}}$	Power going down interrupt
Bit 1	$+5V_P$	Logic HI
Bit 2	TRIG	GPIB chip diagnostic
Bit 3		PARAMETER SWITCH position 8
Bit 4		PARAMETER SWITCH position 10
Bit 5		PARAMETER SWITCH position 9
Bit 6	$+5V_P$	Logic HI
Bit 7	DIAG	Diagnostic latch

OPTION 12
THEORY OF OPERATION

The RS-232-C communication option (see Diagram 23) provides a general-purpose interface for the exchange of waveforms and instrument-state information. It replaces the XY Plotter board of the standard instrument but includes the XY Plotter circuitry. The following discussion refers only to the RS-232-C portion of the board.

The option includes 64K bytes of ROM, 2K bytes of RAM, and an RS-232-C interface. Supporting the RS232 port are two 8-bit input ports for status signals and parameter switches, and a 4-bit output port used mainly for interrupt masking. The remaining circuitry either decodes addresses or buffers signals.

Microprocessor bus signals are extended to this board through W8101. The address bus, data bus, bus control signals, several address decode lines, and power supplies all pass through this connector.

Bus Buffers

The address lines are buffered by U1241 and U1233. These buffers are always enabled. Data bus buffer U1231 is bidirectional. It isolates the option from the storage board and improves signal driving capabilities. Also buffered are the $\overline{\text{RD}}$ (U1233), $\overline{\text{WR}}$ (U1234D), and RESET (U1244E) signals.

Address Decoding

All addresses in the COM-SEG range (80000H to BFFFFH) are used by the option. Several addresses in the I/O-SEG range (40000H to 7FFFFH) are used by option I/O circuitry. Table 3-1 lists the actual addresses used.

Primary address decoding is accomplished by U1245. It provides a one-of-eight, low-asserting signal when BA12, BA13, $\overline{\text{IO SEG}}$, and $\overline{\text{BLK0}}$, are all LO. Address lines BA3, BA6, and BA7 are decoded to produce eight strobes. Three of the strobes are used to enable UART U1251, parameter buffer U1222, and Status buffer U1223. A fourth strobe is gated with $\overline{\text{BWR}}$ at U1234A to produce a write strobe for the interrupt mask latch (U1236). Also generated by U1245 is a signal that is LO whenever one of the strobes is enabled and BA8 is LO. This signal is gated with $\overline{\text{COM SEG}}$ and $\overline{\text{DEN}}$ in U1232A to produce an enable for the data bus buffer (U1231).

The ROM and RAM enable signals are generated by U1235. One half of U1235 is enabled by $\overline{\text{COM SEG}}$. It decodes $\overline{\text{BLK0}}$ and $\overline{\text{BLK1}}$ into four strobes, two are wire-ANDed together to produce the $\overline{\text{ROMEN}}$ enable for the

ROM chip (U1243). The resultant function is to enable the ROM whenever $\overline{\text{COM SEG}}$ is LO and either $\overline{\text{BLK0}}$ or $\overline{\text{BLK1}}$ is LO. This enable drives the output enable pin of U1243 and not its chip enable pin which is driven by $\overline{\text{A18}}$.

The other half of U1235 provides a similar function for U1242, the RAM chip. It generates a LO-going strobe when $\overline{\text{COM SEG}}$, RAM DIS, and $\overline{\text{BLK3}}$ are LO and $\overline{\text{BLK0}}$ and $\overline{\text{BLK1}}$ are HI. RAM DIS disables U1242 if the non-volatile RAM is present. Although the RAM has images throughout the 88000 to 8FFFF address range, only the highest image is used.

Half of U1232 and inverter U1244C generate the $\overline{\text{DATEN}}$ signal for the bidirectional data bus buffer U1231. $\overline{\text{DATEN}}$ is LO for any reference in COM-SEG and for references to the option I/O ports. It is LO when $\overline{\text{DEN}}$, the data enable from the processor, is LO and either $\overline{\text{COM SEG}}$ or $\overline{\text{I/O 2OPT}}$ (U1245 pin 3) is LO.

RAM and ROM

Temporary storage for the option is provided by RAM U1242. Option operating system firmware is contained in ROM U1243.

UART

The UART U1251 communicates with the Microprocessor, providing serial-to-parallel conversion and handling some of the RS232 protocol. Also included is an internal baud rate generator. Crystal Y1251 provides a time base which is divided by software selectable ratios to provide the required bit transfer speeds. Three interrupt lines, INTR, TBRE, and DR, inform the Microprocessor that intervention is required.

Line Drivers

Driver U1225 translates from TTL logic levels to the levels required by the EIA RS-232-C standard. It requires positive and negative supplies which are derived by diodes isolation (CR1224 and CR1223) on the +8.6 V and −8.6 V supplies. Diode isolation protects the instrument from transients or faults coupled through the RS-232-C connectors. The RLSD signal is generated by Interrupt Mask Latch U1236.

The RS-232-C receiver is U1224. It translates from RS-232-C levels to TTL logic levels and also has a protected supply. Its +5 V supply is generated by dropping the +8.6 V supply through zener diode VR1232. The IRSLD2 signal goes to Status Buffer U1223.

All of the RS-232-C signals are protected by diode arrays CR1221 and CR1222, and zener diodes VR1221 through VR1224. Any transients that exceed a ±25 V range are clipped by the networks.

Two connectors, J1212 and J1214, are provided to make interfacing easier. The male DB-25 connector conforms to the DTE (data terminal equipment) specifications of RS-232-C, and the female DB-25 connector conforms to the DCE (data communications equipment) specification. Only one of the connectors may be used at one time.

Interrupt Circuitry

Two interrupt lines from the UART, INTR and DR, are combined via OR gate U1234B, generating the DR+INTR interrupt line. That signal is then routed to U1232A, an AND-OR-INVERT gate, where it is gated with DR+INTR MASK, which comes from the Interrupt Mask Latch (U1236). When DR+INTR MASK is LO, DR+INTR can not propagate through to the output. TBRE is similarly masked by TBRE MASK, then they are ORed together and inverted within the AND-OR-INVERT gate. Inverter U1244D inverts the signal and applies it to the base of Q1221. Transistor Q1221 inverts the signal to $\overline{\text{INTR}}$, driving the Microprocessor maskable interrupt.

Interrupt Mask Latch

Interrupt Mask Latch U1236 provides four signals that are directly controlled by the Microprocessor. It is enabled when the Microprocessor writes to the addresses decoded as $\overline{\text{LATCH}}$. This latch uses BA0 and BA1 to select either 0D, 1D, 2D, or 3D, and latches the data present on U1236 pin 13 into the selected output when enabled. Two of the outputs are used for interrupt masking, one for the RS-232-C port, and one for diagnostics. The outputs are forced LO by the $\overline{\text{BRST}}$ line to insure that interrupts are masked when the Microprocessor powers up.

Parameter Buffer

This circuit is an eight-bit input port for selecting parameters associated with the option such as baud rate and parity. It consists of buffer U1222, switch S1221, and resistor pack R1222. The switch is sensed by enabling the buffer which gates the buffer inputs onto the data bus. Bit 7 is used to sense serial data out (SDO) from U1251 for diagnostic use.

Status Buffer

Status buffer U1223 is used to sense three positions of Parameter switch S1221 as well as miscellaneous other signals. Functions of the Status buffer are shown in Table 7-36.

Table 7-36

RS-232-C Status Buffer Functions

Bit	Signal Name	Function
Bit 0	$\overline{\text{PWR INT}}$	Power-going-down interrupt
Bit 1	$\overline{\text{DR+INTR}}$	UART interrupt request
Bit 2	TBRE	UART interrupt request
Bit 3		Parameter switch position 8
Bit 4		Parameter switch position 10
Bit 5		Parameter switch position 9
Bit 6	DIAG	Interrupt mask latch D3
Bit 7	$\overline{\text{DCD2}}$	Data carrier detect

OPTION MEMORY

Option Memory (see Diagram 25) contains 32K-bytes of non-volatile memory, a lithium battery, and power failure sensing and control circuitry. When the board is installed, the option RAM is disabled.

Address Decoding

Addresses are decoded by U1162. All addresses in the COM-SEG range (88000-8FFFF) are used. Four active LO strobes, one for each RAM, are generated, $\overline{\text{DECODE 0}}$ (U1162 pin 4), $\overline{\text{DECODE 1}}$ (U1162 pin 5), $\overline{\text{DECODE 2}}$ (U1162 pin 12), and $\overline{\text{DECODE 3}}$ (U1162 pin 11).

RAM

Four 8K-byte RAMs make up the 32K-byte non-volatile memory. When instrument power is turned off, $\overline{\text{STANDBY}}$ goes LO, placing the memories in a low current standby state. In the standby state the lithium battery (BT1101) supplies the memories standby current needs.

Each RAM is selected by its Decode signal (pin 20) when the memories are not in standby. Data is read onto the data bus, BD1-BD7, from the memory location selected by BA0-BA12 when $\overline{\text{BRD}}$ goes LO. Data on the data bus, BD0-BD7, is written to the memory location selected by BA0-BA12 when $\overline{\text{BWR}}$ goes LO.

Power Sense

Power to the RAM array is supplied by the Power Sense circuitry. The Power Sense circuit supplies power to the RAM either from the instrument power supply or from the lithium battery.

WARNING

The battery used in this device may present a fire or chemical burn hazard if mistreated. Do not recharge, rapidly discharge, disassemble, heat, or short terminals. See service information for complete instructions.

Lithium Battery

If instrument power is available, 5 V from the instrument forward biases CR1102 and reverse biases CR1104, disconnecting lithium battery BT1101 from the circuit. Because CR1102 is forward biased, the instrument suplies power ($+V_S$) to the RAM through CR1102.

If instrument power is not available, the lithium battery forward biases CR1104 and reverse biases CR1102, supplying power ($+V_S$) to the RAM through CR1104. If there is a circuit failure, lithium battery current is limited to safe levels by ceramic current limiter RT1102.

Voltage Comparator

U1122 compares the instrument voltage to an internal reference to determine if the power is going down. If power is going down, an interrupt is generated to tell the Microprocessor that the power is failing. Also, the RAM is put in standby.

Comparator U1122 compares its internal reference to the voltage on pin 3. The voltage at U1122 pin 3 is set by the instrument power supply and the voltage divider made up of R1112, R1114, and R1116.

If power is up, the voltage at pin 3 is about 1.2 V, and FAIL at U1122 pin 4 is LO. FAIL is inverted and delayed by U1132B, C, D, and associated circuitry, making $\overline{\text{STANDBY}}$ normal operating mode. Also, FAIL is inverted and delayed by U1132B and associated circuitry, generating $\overline{\text{FAIL}}$ HI. Comparators U1142A and U1142B look at both the instrument supply voltage and $\overline{\text{FAIL}}$. If $\overline{\text{FAIL}}$ goes HI (power is coming up), interrupts are not generated, but U1132D pulses the IRST signal HI to reset the microprocessor systems.

If power is going down or is down, the voltage at U1122 pin 3 drops below the internal reference voltage, causing FAIL, U1122 pin 4 to go HI. FAIL is inverted and delayed by U1132B and associated circuitry, generating $\overline{\text{FAIL}}$ LO. Comparators U1142A and U1142B look at both the instrument supply voltage and $\overline{\text{FAIL}}$. Since $\overline{\text{FAIL}}$ is LO

(power failing), interrupts are generated to tell the Microprocessor that instrument power is going down. A LO $\overline{\text{FAIL}}$ is also delayed by U1132C, D, and associated circuitry, making $\overline{\text{STANDBY}}$ LO. This places the RAM in the low current standby operating mode.

PERFORMANCE CHECK PROCEDURE

Introduction

This part of Section 7 contains the GPIB Option and RS-232-C portion of the instrument's performance check procedures. The "Performance Check Procedure" is used to check the GPIB Option performance against the requirements listed in Table 7-4. It is not necessary to remove the instrument cover to accomplish any of the performance checks.

The Option performance check intervals are identical to the basic instrument as indicated in "Performance Check Interval" in the "Performance Check Procedure" Section 4 of this manual.

Limits and Tolerances

The limits and tolerances stated in this procedure are GPIB and RS-232-C specifications only if they are listed in the "Performance Requirements" column of Table 7-4. The tolerances given in this procedure are valid for an instrument that is operating in and has been previously calibrated in an ambient temperature between +20°C and +30°C. The instrument also must have had at least a 20-minute warm-up period. Refer to Table 7-4 for tolerances applicable to an instrument that is operating outside this temperature range. All tolerances specified are for the instrument only and do not include test-equipment error. When performing either the GPIB or the RS-232 checks, it is assumed that the standard instrument meets all of its "Performance Requirements" as stated in the "Specification" (Section 1) of the Service manual.

Test Equipment Required

Test equipment listed in Table 7-37 is required to perform this procedure. Test equipment specifications described in Table 7-37 are the minimum necessary to provide accurate results. Therefore, equipment used must meet or exceed the listed specifications. Detail operating instructions for test equipment are not given in this procedure.

When equipment other than that recommended is used, control settings of the test setup may need to be altered. If the exact item of equipment given as an example in Table 7-37 is not available, check the "Minimum Specification" column to determine if any other available test equipment might suffice for the performance check procedure.

1. GPIB Performance Check

a. Set the RS-232-C Parameter switch to match the requirements of your controller, GPIB Address 1.

b. Set the oscilloscope's front panel controls to obtain a baseline trace.

c. Set the oscilloscope's POWER button to OFF and then to ON.

d. CHECK—The SRQ indicator is on when the power-up sequence is finished.

e. Connect the Controller via GPIB cable to the IEEE STD 488 PORT connector.

Table 7-37

Test Equipment Required

Item and Description	Minimum Specification	Purpose	Example of Suitable Test Equipment
1. Controller	IEEE-488-1978 compatible.	Signal source.	TEKTRONIX 4041 System Controller.
2. GPIB Cable	IEEE-488-1978 compatible.	Signal interconnection.	Tektronix Part Nmber 012-0630-00.
3. RS-232 Cable	Connectors, Male-to-female, 2 meter, 25 wires, general purpose.	Signal interconnection.	Tektronix Part Number 012-0815-00.

f. Enter the following program to the Controller.

```
100  Init
110  ! Initialize gpib
120  Gpib_adr = 1
130  Open #1:"gpib0(pri="&str$(gpib_adr)&",
     EOM=<0>):"
140  ! Poll the instrument
150  Poll srq_stat, srq_addr; gpib_adr
160  ! Get its EVENT code
170  Print #1: "EVENT?"
180  Input #1: eve_code
190  ! Print responses
200  Print "SRQ : ";srq_stat
210  Print " EVENT  : ";eve_code
220  Close all
230  end
```

g. Run the program entered in Part f.

h. CHECK—The SRQ indicator is turned off.

i. CHECK—The controller for SRQ: 65.0 and EVEN: 401.0.

j. Disconnect the test equipment from the instrument.

2. RS-232-C Performance Check

a. Set the RS-232-C Parameter switch to match the requirements of your controller.

b. Set the oscilloscope's front panel controls to obtain a baseline trace.

c. Set the oscilloscope's POWER button to OFF and then to ON.

d. CHECK—The SRQ indicator is on when the power-up sequence is finished.

e. Connect the Controller via RS-232 cable to the RS232 DCE connector.

f. Enter the message "ID?;" from the controller to the RS-232.

g. CHECK—The response to the controller from the RS-232 is "TEK/2230,V81.1.VERS:XX", where"XX" is the ROM's firmware version number in the instrument.

h. CHECK—The SRQ indicator is turned off.

i. Disconnect the test equipment from the instrument.

ADJUSTMENT PROCEDURE

There are no adjustment procedures for the GPIB and RS-232-C Options.

OPTION MAINTENANCE INFORMATION

WARNING

The battery used in this device may present a fire or chemical burn hazard if mistreated. Do not recharge, rapidly discharge, disassemble, heat above 100°C (212°F), or incinerate.

Replace battery with part number listed in replaceable parts section only. Use of another battery may present a risk of fire or explosion.

Dispose of used battery promptly. Small quantities of used batteries may be disposed of in normal refuse. Keep away from children. Do not disassemble and do not dispose of in fire.

Maintenance information contained in the Maintenance Section of the manual also applies to these options. Additional information for the Options is contained in this part of the manual.

Diagnostics

Additional diagnostics are added to the instrument when Option 10 or Option 12 are added to the instrument. This discussion describes each diagnostic separately.

COMM_RAM. This test checks the Option RAM and its microprocessor interface. This test is performed during Power-Up. The RAM is filled with a checkerboard pattern of AA55 and 55AA and checked to see if the values are correct.

NOTE

The displayed address is offset from 0x80000 and is a 4 digit hexadecimal number between F800 and FFFF.

If an error is found, the address of the error, the actual data found at the address, and the data expected at the address are displayed on the crt:

COMM_RAM : @ <address> <actual data> <> <expected data>

CMOS_RAM. This test checks the nonvolatile CMOS memory. It is performed during Power-Up. Each stored waveform is analyzed to determine if they contain errors. If errors are found, the diagnostic either repairs or removes the waveform. If seven or more errors are found, the entire CMOS memory is reformated, erasing all stored waveforms. If errors are found, the result of the recovery attempt displayed on the crt:

CMOS : reformated
or
CMOS : recovered

If errors are reported, the instrument should be turned off and then powered up again. An error should be ignored unless it is repeatable.

ROM_MATCH. This test checks to see that all ROMs are the correct version number ROMs. Each ROM is checked during Power-Up. If an error is found, the version numbers found are displayed on the crt:

ROMS:mismatch,nn,mm,oo

where nn, mm, and oo are the version numbers of the ROMs in the instrument.

COMM_READBACK. Bit paths within the Option are checked by COMM_READBACK. GPIB circuitry checked includes U1335B and U1323. RS-232-C circuitry checked includes U1236 and U1223. Data is first written to the Option. Registers are then read and checked for the correct data. If the data read back is in error, the actual data read back is displayed on the crt:

COMM_RB : rb(1) = x_2x_1 & rb(0) = y_2y_1

where:

rb is the data written to the Option (U1236 pin 7 or U1335 pin 10).

x_1 = y_1 = data read back from the Option (U1223 pin 3 or U1323 pin 3).

x_2 = y_2 = data read back from the Option (U1223 pin 2 or U1323 pin 2).

COMM_LOOPBACK. This test checks the GPIB controller U1321 and associated circuitry by commanding the controller to change its TR output and then checking the TR output. If an error is found it is displayed on the crt:

COMM_LB : FGET NOT SET
or
COMM_LB : FGET NOT CLEAR

INPUT_PORTS. Two additional ports are added to the INPUT_PORTS diagnostic. Option 10 adds U1322 and U1323. Option 12 adds U1222 and U1223. They are labeled on the crt display as COMM_STAT U1x23 and COMM_PARAM U1x22.

OUT_PORTS. Two output ports are added the the OUT_PORTS diagnostic by the Options. OUT_PORTS is run at power-up only. Option 10 adds U1335B. The pattern seen on U1315B pin 10 is about an eight second square wave. Option 12 adds U1236. The pattern seen on U1236 is the same type of shift pattern as for the PRC test.

Removal and Replacement Instructions

The exploded view drawings in the "Replaceable Mechanical Parts" list (Section 9) may be helpful during the removal and reinstallation of the GPIB and RS-232-C assembly and its circuit boards from the instrument. Circuit board and component locations are shown in the "Diagrams" section.

CABINET. To remove either the GPIB or the RS-232-C Assembly from the instrument, perform the "Cabinet" removal procedure in the "Removal and Replacement Instructions" of Section 6. In step 4 of the procedure, remove two screws and two post spacers and washers from the GPIB side panel or two screws and four post spacers and washers from the RS-232-C side panel.

MEMORY CIRCUIT BOARD. The Memory circuit board can be removed and reinstalled as follows:

1. Remove the four flat-head screws that secures the insulation and the Memory circuit board to the Option Assembly. Remove the insulation from the Memory circuit board.

2. Remove the Memory circuit board from GPIB Assembly by carefully pulling the connectors P1251 and P1222 on the Memory circuit board from the pins of J1251 and J1222 on either the GPIB or the RS-232-C circuit board. The connectors are located on the inside and at each end of the Memory circuit board. Disconnect P1152 from the rear of the Memory circuit board as it being removed from the GPIB Assembly.

To reinstall the Memory circuit board, perform the reverse of the preceding steps.

GPIB AND RS-232-C ASSEMBLIES. The Option assembly can be removed and reinstalled as follows:

NOTE

The field-installed GPIB Option and RS-232-C Option have one more connector to be removed than the factory installed Options.

1. Disconnect the following connectors from the Option Assembly and the instrument.

a. P4110, a two-wire connector located at the rear of the Option Assembly.

b. P6423, a four-wire connector located at the rear of the Option Assembly.

c. P9301, a five-wire connector located at the rear of the Option Assembly.

d. P8100, a ribbon cable from the Storage circuit board.

NOTE

Instruments with factory-installed GPIB and RS-232-C, proceed to step 3. For field-installed GPIB and RS-232-C, proceed with step 2.

2. Disconnect either P1316 (GPIB) or P1216 (RS-232-C) from the front of the Option assembly circuit board.

3. Stand the instrument on its side (Option Assembly up) and remove two screws from the extreme edge of the bottom chassis frame underneath the delay line cable.

4. Lay the instrument down and remove the two screws from the top of the chassis frame (located inside the two cutouts on the Storage circuit board). Note the position of the ground clip when removing the screw from the chassis frame.

5. Remove the Option Assembly out from between the top and bottom chassis frames.

6. Slide the Option Assembly forward until the ribbon cable clears the Storage circuit board.

7. Remove the Option Assembly from the instrument by tilting the bottom of the assembly out first.

To reinstall the Option Assembly, perform the reverse of the preceding steps.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

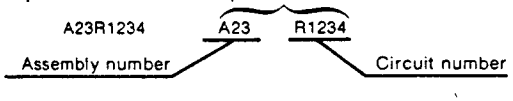
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

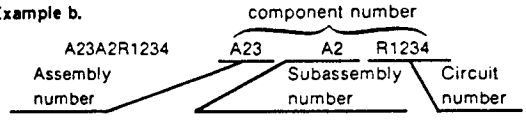
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00213	NYTRONICS COMPONENTS GROUP INC SUBSIDIARY OF NYTRONICS INC	ORANGE ST	DARLINGTON SC 29532
00779	AMP INC	P O BOX 3608	HARRISBURG PA 17105
00853	SANGAMO WESTON INC SANGAMO CAPACITOR DIV	SANGAMO RD P O BOX 128	PICKENS SC 29671
01121	ALLEN-BRADLEY CO	1201 SOUTH 2ND ST	MILWAUKEE WI 53204
01281	TRW INC TRW SEMICONDUCTOR DIV	14520 AVIATION BLVD	LAWNDALE CA 90260
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPRESSWAY P O BOX 225012 M/S 49	DALLAS TX 75265
01537	MOTOROLA COMMUNICATIONS AND ELECTRONICS INC	2553 N EDGINGTON ST	FRANKLIN PARK IL 60131
01807	PETERSEN RADIO CO INC	2800 WEST BROADWAY	COUNCIL BLUFFS IA 51501
02113	COILCRAFT INC	1102 SILVER LAKE RD	CARY IL 60013
02114	AMPEREX ELECTRONIC CORP FERROXCUBE DIV	5083 KINGS HWY	SAUGERTIES NY 12477
02735	RCA CORP SOLID STATE DIVISION	ROUTE 202	SOMERVILLE NJ 08876
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	W GENESEE ST	AUBURN NY 13021
04099	CAPCO INC	FORESIGHT INDUSTRIAL PARK P O BOX 2164	GRAND JUNCTION CO 81501
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR GROUP	5005 E MCDOWELL RD	PHOENIX AZ 85008
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
06665	PRECISION MONOLITHICS INC SUB OF BOURNS INC	1500 SPACE PARK DR	SANTA CLARA CA 95050
07263	FAIRCHILD CAMERA AND INSTRUMENT CORP SEMICONDUCTOR DIV	464 ELLIS ST	MOUNTAIN VIEW CA 94042
07716	TRW INC TRW ELECTRONICS COMPONENTS TRW IRC FIXED RESISTORS/BURLINGTON	2850 MT PLEASANT AVE	BURLINGTON IA 52601
11236	CTS OF BERNE INC	406 PARR ROAD	BERNE IN 46711
12697	CLAROSTAT MFG CO INC	LOWER WASHINGTON ST	DOVER NH 03820
12954	MICROSEMI CORP	8700 E THOMAS RD P O BOX 1390	SCOTTSDALE AZ 85252
12969	UNITRODE CORP	580 PLEASANT ST	WATERTOWN MA 02172 LOS GATOS CA
13511	AMPHENOL CADRE DIV BUNKER RAMO CORP		
13556	TRW CINCH CONNECTORS NULINE FACILITY	8821 SCIENCE CENTER DRIVE	NEWHOPE MN 55428
14193	CAL-R INC	1601 OLYMPIC BLVD	SANTA MONICA CA 90404
14552	MICRO/SEMICONDUCTOR CORP	2830 S FAIRVIEW ST	SANTA ANA CA 92704
14752	ELECTRO CUBE INC	1710 S DEL MAR AVE	SAN GABRIEL CA 91776
15238	ITT SEMICONDUCTORS A DIVISION OF INTERNATIONAL TELEPHONE AND TELEGRAPH CORP	500 BROADWAY P O BOX 168	LAWRENCE MA 01841
15454	AMETEK INC RODAN DIV	2905 BLUE STAR ST	ANAHEIM CA 92806
15636	ELEC-TROL INC	26477 N GOLDEN VALLEY RD	SAUGUS CA 91350
17856	SILICONIX INC	2201 LAURELWOOD RD	SANTA CLARA CA 95054
18324	SIGNETICS CORP	811 E ARQUES	SUNNYVALE CA 94086
19396	ILLINOIS TOOL WORKS INC PAKTRON DIVISION	900 FOLLIN LANE S E	VIENNA VA 22180
19701	MEPCO/ELECTRA INC A NORTH AMERICAN PHILIPS CO	P O BOX 760	MINERAL WELLS TX 76067
20932	KYOCERA INC	11620 SORRENTO VALLEY RD	SAN DIEGO CA 92121
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS	30 HUNTER LANE	CAMP HILL PA 17011
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701
24931	SPECIALTY CONNECTOR CO INC	2620 ENDRESS PLACE P O BOX D	GREENWOOD IN 46142
25403	AMPEREX ELECTRONIC CORP SEMICONDUCTOR AND MICROCIRCUITS DIV	PROVIDENCE PIKE	SLATERSVILLE RI 02876

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051
31433	UNION CARBIDE CORP ELECTRONICS DIV	PO BOX 5928	GREENVILLE SC 29606
31918	ITT SCHADOW INC	8081 WALLACE RD	EDEN PRAIRIE MN 55343
32293	INTERSIL INC	10900 N TANTAU AVE	CUPERTINO CA 95014
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507
34371	HARRIS SEMICONDUCTOR DIV OF HARRIS CORP	P O BOX 883	MELBOURNE FL 32901
34649	INTEL CORP	3065 BOWERS AVE	SANTA CLARA CA 95051
34899	FAIR-RITE PRODUCTS CORP	1 COMMERCIAL ROW	WALLKILL NY 12589
50157	MIDWEST COMPONENTS INC	1981 PORT CITY BLVD P O BOX 787	MUSKEGON MI 49443
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	640 PAGE MILL RD	PALO ALTO CA 94304
51406	MURATA ERIE NORTH AMERICA INC GEORGIA OPERATIONS	1148 FRANKLIN RD SE	MARIETTA GA 30067
51642	CENTRE ENGINEERING INC	2820 E COLLEGE AVE	STATE COLLEGE PA 16801
51984	NEC AMERICA INC	2741 PROSPERITY AVE	FAIRFAX VA 22031
52763	STETTNER ELECTRONICS INC	6135 AIRWAYS BLVD PO BOX 21947	CHATTANOOGA TN 37421
52769	SPRAGUE-GOODMAN ELECTRONICS INC	134 FULTON AVE	GARDEN CITY PARK NY 11040
54473	MATSUSHITA ELECTRIC CORP OF AMERICA	ONE PANASONIC WAY	SECAUCUS NJ 07094
54583	TDK ELECTRONICS CORP	755 EASTGATE BLVD	GARDEN CITY NY 11530
54937	DE YOUNG MANUFACTURING INC	12920 NE 125TH WAY	KIRKLAND, WA 98034-7716
55112	WESTLAKE CAPACITORS INC	5334 STERLING CENTER DRIVE	WESTLAKE VILLAGE CA 91361
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195
56289	SPRAGUE ELECTRIC CO	87 MARSHALL ST	NORTH ADAMS MA 01247
56866	QUALITY THERMISTOR INC	2096 SOUTH COLE RD SUITE 7	BOISE ID 83705
57668	ROHM CORP	16931 MILLIKEN AVE	IRVINE CA 92713
58361	GENERAL INSTRUMENT CORP OPTOELECTRONICS DIV	3400 HILLVIEW AVE	PALO ALTO CA 94304
59660	TUSONIX INC	2155 N FORBES BLVD	TUCSON, ARIZONA 85705
59821	CENTRALAB INC SUB NORTH AMERICAN PHILIPS CORP	7158 MERCHANT AVE	EL PASO TX 79915
71400	BUSSMANN MFG CO MCGRAW EDISION CO	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
71468	ITT CANNON ELECTRIC	10550 TALBERT PO BOX 8040	FOUNTAIN VALLEY CA 92728-8040
71590	GLOBE-UNION INC CENTRALAB ELECTRONICS DIV	HWY 20 W P O BOX 858	FORT DODGE IA 50501
74868	AMPHENOL R F OPERATIONS AN ALLIED CO	33 E FRANKLIN ST	DANBURY CT 06810
75042	TRW INC TRW ELECTRONIC COMPONENTS IRC FIXED RESISTORS PHILADELPHIA DIV	401 N BROAD ST	PHILADELPHIA PA 19108
75915	LITTELFUSE INC	800 E NORTHWEST HWY	DES PLAINES IL 60016
76493	BELL INDUSTRIES INC MILLER J W DIV	19070 REYES AVE P O BOX 5825	COMPTON CA 90224
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
82389	SWITCHCRAFT INC SUB OF RAYTHEON CO	5555 N ELSTRON AVE	CHICAGO IL 60630
84411	TRW INC TRW ELECTRONICS COMPONENTS DIV TRW CAPACITORS	301 WEST O ST	OGALLALA NE 69153
91637	DALE ELECTRONICS INC	P O BOX 609	COLUMBUS NE 68601
96341	M/A-COM SEMICONDUCTOR PRODUCTS INC	NORTHWEST INDUSTRIAL PARK SOUTH AVE	BURLINGTON MA 01803
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO CA 91341
97525	ELECTRONIC ENGINEERING COMPANY OF CALIFORNIA/EECO	1441 E CHESTNUT AVENUE	SANTA ANA, CA 92702
D5243	ROEDERSTEIN E SPEZIALFABRIK FUER KONDENSATOREN GMBN	LUDMILLASTRASSE 23-25	8300 LANDSHUT GERMANY
TK0146	BUEHLER PRODUCTS INC	PO BOX A, HIGHWAY 70	EAST KINSTON NC 28501

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
TK0196	ALMAC-STROUM ELECTRONICS	1885 NW 169TH PLACE	BEAVERTON OR 97006
TK0213	TOPTRON CORP	TOKYO	JAPAN
TK0510	PANASONIC COMPANY DIV OF MATSUSHITA ELECTRIC CORP	ONE PANASONIC WAY	SECAUCUS NJ 07094
TK0515	RIFA WORLD PRODUCTS INC	19678 8TH STREET EAST P O BOX 517	SONOMA CA 95476
TK0946	SAN-O INDUSTRIAL CORP	170 WILBUR PL	BAHEMIA, LONG ISLAND NY 11716
TK0961	NEC ELECTRONICS USA INC	401 ELLIS ST	MOUNTAIN VIEW CA 94043
TK1016	TOSHIBA AMERICA INC ELECTRONIC COMPONENTS DIV BUSINESS SECTOR	2692 DOW AVE	TUSTIN CA 92680
TK1339	PREM MAGNETICS INC	3521 N CHAPEL SPACE HILL RD	MCHENRY IL 60050
TK1345	ZMAN AND ASSOCIATES	7633 S 180TH	KENT WA 98032
TK1395	ROEDERSTEIN ELECTRONICS INC	2100 WEST FRONT ST P O BOX 5588	STATESVILLE NC 28677
TK1421	COILTRON	PO BOX 904	BEAVERTON OR 97075
TK1450	TOKYO COSMOS ELECTRIC CO LTD	2-268 SOBUDAI ZAWA	KANAGAWA 228 JAPAN
TK1483	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
TK1573	WILHELM WESTERMAN	PO BOX 2345 AUGUSTA-ANLAGE 56	6800 MANNHEIM 1 WEST GERMANY
TK1856	VLSI TECHNOLOGY INC	1101 MCKAY DRIVE	SAN JOSE CA 95131
TK1884	ROGERS CORPORATION Q PAC DIVISION	5750 EAST MCKELLIPS RD	MESA ARIZONA 85205
TK2042	ZMAN & ASSOCIATES	7633 SO. 180TH	KENT, WA 98032
TK2048	UNION CARBIDE INC	401 PARK PLACE SUITE 219	KIRKLAND, WASHINGTON 98033

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	670-8708-00	B010100	B022101	CIRCUIT BD ASSY:MAIN	80009	670-8708-00
A1	670-8708-01	B022102		CIRCUIT BD ASSY:MAIN	80009	670-8708-01
A2	670-8699-00			CIRCUIT BD ASSY:ATTENUATOR	80009	670-8699-00
A3	670-8710-00	B010100	B019999	CIRCUIT BD ASSY:FR PNL	80009	670-8710-00
A3	670-8710-01	B020000		CIRCUIT BD ASSY:FRONT PNL	80009	670-8710-01
A4	670-8709-00	B010100	B012199	CIRCUIT BD ASSY:TIMING	80009	670-8709-00
A4	670-8709-02	B012200	B022101	CIRCUIT BD ASSY:TIMING	80009	670-8709-02
A4	670-8709-02	B022102		CIRCUIT BD ASSY:TIMING	80009	670-8709-02
A5	670-8711-00	B010100	B022042	CIRCUIT BD ASSY:ALT SW	80009	670-8711-00
A5	670-8711-01	B022043		CIRCUIT BD ASSY:ALTERNATE SWEEP	80009	670-8711-01
A6	670-7615-00			CIRCUIT BD ASSY:EMI FILTER	80009	670-7615-00
A7	----- -----			CIRCUIT BD ASSY:INTENS POT (SEE R9802 REPL)		
A10	670-8702-00	B010100	B019999	CIRCUIT BD ASSY:STORAGE	80009	670-8702-00
A10	670-8702-01	B020000	B021984	CIRCUIT BD ASSY:STORAGE	80009	670-8702-01
A10	670-8702-02	B021985		CIRCUIT BD ASSY:STORAGE	80009	670-8702-02
A11	672-1194-00	B010100	B022101	CIRCUIT BD ASSY:INPUT/OUTPUT & VECTOR GEN	80009	672-1194-00
A11	672-1194-01	B022102		CIRCUIT BD ASSY:INPUT/OUTPUT & VECTOR GEN	80009	672-1194-01
A11A1	----- -----			CKT BOARD ASSY:INPUT/OUTPUT (NOT AVAILABLE, USE A11)		
A11A2	----- -----			CKT BOARD ASSY:VECTOR GENERATOR (NOT AVAILABLE, USE A11)		
A13	670-8705-00			CIRCUIT BD ASSY:SWEEP INTFC	80009	670-8705-00
A14	670-8698-00			CIRCUIT BD ASSY:LOGIC CH1 & CH2 (CH 1 LOGIC BOARD)	80009	670-8698-00
A15	670-8698-00			CIRCUIT BD ASSY:LOGIC CH1 & CH2 (CH 2 LOGIC BOARD)	80009	670-8698-00
A16	670-8706-00			CIRCUIT BD ASSY:SWEEP REF	80009	670-8706-00
A17	670-8780-00			CIRCUIT BD ASSY:POSITION INTERFACE	80009	670-8780-00
A18	670-8998-00			CIRCUIT BD ASSY:THERMAL SHUTDOWN	80009	670-8998-00
A20	670-8898-00	B010100	B021412	CIRCUIT BD ASSY:X-Y PLOTTER	80009	670-8898-00
A20	670-8898-01	B021413		CIRCUIT BD ASSY:X-Y PLOTTER	80009	670-8898-01
A21	670-8899-00	B010100	B021935	CIRCUIT BD ASSY:RS232	80009	670-8899-00
A21	670-8899-01	B021936		CIRCUIT BD ASSY:RS232 (OPTION 12 ONLY)	80009	670-8899-01
A22	670-8900-00	B010100	B021759	CIRCUIT BD ASSY:GPIB	80009	670-8900-00
A22	670-8900-01	B021760		CIRCUIT BD ASSY:GPIB (OPTION 10 ONLY)	80009	670-8900-01
A23	670-8952-00	B010100	B021935	CIRCUIT BD ASSY:OPT MEMORY	80009	670-8952-00
A23	670-8952-01	B021936		CIRCUIT BD ASSY:A23 OPTION MEMORY (OPTION 12,10 ONLY)	80009	670-8952-01
A24	670-9701-00	B020000		CIRCUIT BD ASSY:CURSOR CONTROL	80009	670-9701-00
A1	670-8708-00	B010100	B022101	CIRCUIT BD ASSY:MAIN	80009	670-8708-00
A1	670-8708-01	B022102		CIRCUIT BD ASSY:MAIN	80009	670-8708-01
A1C100	283-0853-00	B022630		CAP,FXD,CER DI:2.2PF,200V	TK2048	C322C22902G5CA
A1C114	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A1C115	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A1C116	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C125	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A1C126	285-1346-00			CAP,FXD,PLASTIC:1500PF,100V,5%	55112	185(1500PF)
A1C130	283-0159-00			CAP,FXD,CER DI:18PF,5%,50V	04222	SR155A180JAA
A1C133	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A1C150	283-0853-00	B022630		CAP,FXD,CER DI:2.2PF,200V	TK2048	C322C22902G5CA
A1C164	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A1C165	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1C175	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A1C176	285-1346-00			CAP,FXD,PLASTIC:1500PF,100V,5%	55112	185(1500PF)
A1C180	283-0159-00			CAP,FXD,CER DI:18PF,5%,50V	04222	SR155A180JAA
A1C200	290-0136-00			CAP,FXD,ELCTLT:2.2UF,20%,20V	05397	T322B225M020AS
A1C201	290-0136-00			CAP,FXD,ELCTLT:2.2UF,20%,20V	05397	T322B225M020AS
A1C202	281-0811-00	B010980		CAP,FXD,CER DI:10PF,10%,100V	04222	MA101A100KAA
A1C210	281-0500-00	B010100	B022386	CAP,FXD,CER DI:2.2PF,+/-0.5PF,500V	52763	2RDPLZ007 2P200C
A1C210	283-0853-00	B022387		CAP,FXD,CER DI:2.2FF,200V	TK2048	C322C229G2G5CA
A1C215	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C220	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A1C225	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V	04222	MA101A100MAA
A1C226	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C228	283-0665-00			CAP,FXD,MICA DI:190PF,1%,100V	00853	D155F191F0
A1C229	283-0665-00			CAP,FXD,MICA DI:190PF,1%,100V	00853	D155F191F0
A1C237	281-0140-00			CAP,VAR,CER DI:5-25PF,100V	59660	518-023A 5-25
A1C239	281-0776-00			CAP,FXD,CER DI:120PF,5%,100V	20932	401E0100AD121J
A1C240	281-0511-00			CAP,FXD,CER DI:22PF,+/-2.2PF,500V	52763	2RDPLZ007 22P0KC
A1C241	281-0777-00			CAP,FXD,CER DI:51PF,5%,100V	04222	MA101A510JAA
A1C242	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A1C250	281-0768-00			CAP,FXD,CER DI:470PF,20%,100V	04222	MA101A471MAA
A1C251	281-0768-00			CAP,FXD,CER DI:470PF,20%,100V	04222	MA101A471MAA
A1C255	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C262	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C274	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C281	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C282	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A1C292	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A1C312	281-0893-00			CAP,FXD,CER DI:4.7PF,+/-0.5PF,100V	04222	MA101A4R7DAA
A1C337	281-0893-00			CAP,FXD,CER DI:4.7PF,+/-0.5PF,100V	04222	MA101A4R7DAA
A1C350	281-0898-00			CAP,FXD,CER DI:7.5PF,+/-0.5PF,500V	96733	XR3446
A1C351	281-0756-00	B010270		CAP,FXD,CER DI:2.2PF,+/-0.5PF,200V	04222	MA105A2R2DAA
A1C363	281-0862-00	B010100	B022101	CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C369	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C381	283-0663-00			CAP,FXD,MICA DI:16.8PF,+/0.5PF,500V	00853	D155C16R8D0
A1C389	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C390	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C392	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C396	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A1C397	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C400	283-0094-00			CAP,FXD,CER DI:27PF,10%,200V	59821	2DDT73K270K
A1C414	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A1C415	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A1C418	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C419	281-0851-00			CAP,FXD,CER DI:180PF,5%,100VDC	04222	MA101A181JAA
A1C420	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C421	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C440	283-0665-00			CAP,FXD,MICA DI:190PF,1%,100V	00853	D155F191F0
A1C453	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C454	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C459	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C460	281-0826-00			CAP,FXD,CER DI:2200PF,5%,100V	20932	401EM100AD222K
A1C467	281-0772-00	B010100	B022076	CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A1C467	281-0826-00	B022077		CAP,FXD,CER DI:2200PF,5%,100V	20932	401EM100AD222K
A1C469	281-0772-00	B010100	B022076	CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A1C469	281-0826-00	B022077		CAP,FXD,CER DI:2200PF,5%,100V	20932	401EM100AD222K
A1C473	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C480	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A1C487	281-0785-00	B022077		CAP,FXD,CER DI:68PF,10%,100V	04222	MA101A680KAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1C494	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C499	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C500	281-0903-00			CAP,FXD,CER DI:3.9PF,100V	04222	MA101A3R9DAA
A1C501	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A1C502	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C503	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C504	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A1C505	290-0183-00			CAP,FXD,ELCTLT:1UF,10%,35V	05397	T3228105K035AS
A1C506	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A1C507	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A1C518	281-0852-00			CAP,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A1C519	290-0814-00			CAP,FXD,ELCTLT:0.33MF,10%,20V	05397	T110A334K020AS
A1C520	290-0301-00			CAP,FXD,ELCTLT:10UF,10%,20V	05397	T110B106K020AS
A1C521	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C525	281-0895-00			CAP,FXD,CER DI:6.8PF,100WVDC	04222	MA101A6R8DAA
A1C527	281-0797-00			CAP,FXD,CER DI:15PF,10%,100V	04222	MA106A150KAA
A1C528	281-0750-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A1C531	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C537	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C538	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C539	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C540	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A1C544	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C545	285-1345-00			CAP,FXD,PLASTIC:2200PF,100V,5%	55112	185(2200PF)
A1C547	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A1C553	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C561	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C562	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C562	281-0775-01	B010552		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C563	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C563	281-0775-01	B010552		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C565	281-0768-00			CAP,FXD,CER DI:470PF,20%,100V	04222	MA101A471MAA
A1C590	290-0136-00			CAP,FXD,ELCTLT:2.2UF,20%,20V	05397	T322B225M020AS
A1C603	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C635	281-0826-00			CAP,FXD,CER DI:2200PF,5%,100V	20932	401EM100AD222K
A1C646	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A1C647	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C648	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C649	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C764	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C770	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C775	281-0214-00			CAP,VAR,CER DI:0.6-3PF,400V	52763	313613-140
A1C777	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	MA106E222MAA
A1C779	285-1101-00			CAP,FXD,PLASTIC:0.022UF,10%,200V	19396	223K02PT485
A1C780	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C782	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C785	281-0661-00	B010100	B010245	CAP,FXD,CER DI:0.8PF,+/-0.1PF,500V	52763	2RDPLZ007 0P80BC
A1C785	281-0214-00	B010246		CAP,VAR,CER DI:0.6-3PF,400V	52763	313613-140
A1C787	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	MA106E222MAA
A1C789	285-1101-00			CAP,FXD,PLASTIC:0.022UF,10%,200V	19396	223K02PT485
A1C796	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C797	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C799	283-0057-00	B010100	B022356	CAP,FXD,CER DI:0.1UF,+80-20%,200V	04222	SR306E104ZAA
A1C799	285-1341-00	B022357		CAP,FXD,PLASTIC:0.1UF,20%,100V	TK1573	MKS2 0.1/100/20
A1C824	281-0785-00			CAP,FXD,CER DI:68PF,10%,100V	04222	MA101A680KAA
A1C825	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A1C828	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C832	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1C835	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C845	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	MA106E222MAA
A1C847	283-0057-00	B010100	B022356	CAP,FXD,CER DI:0.1UF,+80-20%,200V	04222	SR306E104ZAA
A1C847	285-1341-00	B022357		CAP,FXD,PLASTIC:0.1UF,20%,100V	TK1573	MKS2 0.1/100/20
A1C849	283-0057-00	B010100	B022356	CAP,FXD,CER DI:0.1UF,+80-20%,200V	04222	SR306E104ZAA
A1C849	285-1341-00	B022357		CAP,FXD,PLASTIC:0.1UF,20%,100V	TK1573	MKS2 0.1/100/20
A1C851	283-0057-00	B010100	B022356	CAP,FXD,CER DI:0.1UF,+80-20%,200V	04222	SR306E104ZAA
A1C851	285-1341-00	B022357		CAP,FXD,PLASTIC:0.1UF,20%,100V	TK1573	MKS2 0.1/100/20
A1C853	281-0791-00			CAP,FXD,CER DI:270PF,10%,100V	04222	MA101C271KAA
A1C854	283-0279-00			CAP,FXD,CER DI:0.001UF,20%,3000V	51406	DHR12Y5S102M3KV
A1C855	285-1255-00			CAP,FXD,PLASTIC:0.01UF,20%,3KV	56289	430P582
A1C871	283-0057-00	B010100	B022356	CAP,FXD,CER DI:0.1UF,+80-20%,200V	04222	SR306E104ZAA
A1C871	285-1341-00	B022357		CAP,FXD,PLASTIC:0.1UF,20%,100V	TK1573	MKS2 0.1/100/20
A1C873	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C875	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C877	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C893	283-0279-00			CAP,FXD,CER DI:0.001UF,20%,3000V	51406	DHR12Y5S102M3KV
A1C904	285-1222-00			CAP,FXD,PLASTIC:0.068UF,20%,250V	55112	158/.068/M/250/H
A1C906	290-0978-00			CAP,FXD,ELCTLT:75UF,+50-10%,450V	56289	17D1149
A1C907	285-0932-00	B010100	B011390	CAP,FXD,PLASTIC:1UF,10%,400V	04099	C705D105K
A1C907	285-1177-01	B011391		CAP,FXD,PLASTIC:1UF,10%,400V	80009	285-1177-01
A1C908	283-0481-00			CAP,FXD,CER DI:220PF,10%,250VAC	TK1395	RK0611
A1C917	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A1C919	281-0852-00			CAP,FXD,CER DI:1800PF,10%,100VDC	04222	MA101C182KAA
A1C922	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C925	290-0973-00			CAP,FXD,ELCTLT:100UF,20%,25VDC	55680	ULB1E101MPA
A1C940	290-0922-00			CAP,FXD,ELCTLT:1000UF,20%,50V	55680	ULB1E102TFAANA
A1C941	283-0057-00	B010100	B022456	CAP,FXD,CER DI:0.1UF,+80-20%,200V	04222	SR306E104ZAA
A1C941	285-1341-00	B022357		CAP,FXD,PLASTIC:0.1UF,20%,100V	TK1573	MKS2 0.1/100/20
A1C942	290-0768-00			CAP,FXD,ELCTLT:10UF,+50-10%,100VDC	54473	ECE-A100V10L
A1C943	290-0768-00			CAP,FXD,ELCTLT:10UF,+50-10%,100VDC	54473	ECE-A100V10L
A1C944	290-0163-00			CAP,FXD,ELCTLT:1UF,10%,35V	05397	T3228105K035AS
A1C945	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C951	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C954	290-0947-00			CAP,FXD,ELCTLT:33UF,+50-10%,160V W/SLEEVE (NOMINAL VALUE)	55680	UHC2C330TFA
A1C954	290-1130-00	B022634		CAP,FXD,ELCTLT:39UF,+100%-10%,150V (SELECTABLE VALUE)	56289	ORDER BY DESCR
A1C956	290-0946-00			CAP,FXD,ELCTLT:270UF,+100-10%,40V	00853	301EN271W040B2
A1C958	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C959	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C960	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C961	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C962	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C963	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C964	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C965	290-0989-00			CAP,FXD,ELCTLT:4700UF,20%,10V	TK0510	ECEA1AS472
A1C968	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C970	290-0945-00			CAP,FXD,ELCTLT:840UF 10 + 100 %,12V	00853	301EN841U012B2
A1C975	285-1255-00			CAP,FXD,PLASTIC:0.01UF,20%,3KV	56289	430P582
A1C976	285-1255-00			CAP,FXD,PLASTIC:0.01UF,20%,3KV	56289	430P582
A1C979	285-1255-00			CAP,FXD,PLASTIC:0.01UF,20%,3KV	56289	430P582
A1C6121	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C6122	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C6123	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C6131	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A1C7101	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C7201	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1C7203	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C7260	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C7320	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C7361	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A1C7362	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1CR133	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR183	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR200	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR201	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR202	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR203	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR224	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR225	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR226	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR227	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR228	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR229	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR372	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR381	152-0245-00			SEMICOND DVC,DI:SW,SI,40V,DO-7	03508	DA2740
A1CR393	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR399	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR414	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR415	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR467	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR476	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR477	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR501	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR504	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR505	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR508	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR509	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR514	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR527	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR531	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR532	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR541	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR551	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR556	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR590	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR712	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR764	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR765	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR768	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR770	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR780	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR805	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR818	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR820	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR823	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR824	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR825	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR829	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR840	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR845	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR851	152-0413-00			SEMICOND DVC,DI:RECT,SI,400V,1.0A,A59	04713	SR2046KRL
A1CR853	152-0413-00			SEMICOND DVC,DI:RECT,SI,400V,1.0A,A59	04713	SR2046KRL
A1CR854	152-0413-00			SEMICOND DVC,DI:RECT,SI,400V,1.0A,A59	04713	SR2046KRL
A1CR855	152-0413-00			SEMICOND DVC,DI:RECT,SI,400V,1.0A,A59	04713	SR2046KRL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1CR901	152-0040-00			SEMICOND DVC,DI:RECT,SI,600V,1A,DO-41	80009	152-0040-00
A1CR902	152-0040-00			SEMICOND DVC,DI:RECT,SI,600V,1A,DO-41	80009	152-0040-00
A1CR903	152-0040-00			SEMICOND DVC,DI:RECT,SI,600V,1A,DO-41	80009	152-0040-00
A1CR904	152-0040-00			SEMICOND DVC,DI:RECT,SI,600V,1A,DO-41	80009	152-0040-00
A1CR907	152-0808-00			SEMICOND DVC,DI:RECT,SI,400V,1.5 A,50 NS	01281	DSR3400X
A1CR908	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR920	152-0061-00			SEMICOND DVC,DI:SW,SI,175V,0.1A,DO-35	07263	FDH2161
A1CR946	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR947	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR948	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR954	152-0413-00			SEMICOND DVC,DI:RECT,SI,400V,1.0A,A59	04713	SR2046KRL
A1CR955	152-0413-00			SEMICOND DVC,DI:RECT,SI,400V,1.0A,A59	04713	SR2046KRL
A1CR956	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR957	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR960	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR961	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR962	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR963	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR965	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR967	152-0414-00			SEMICOND DVC,DI:RECT,SI,200V,1.0A,TEK A59	04713	SR2069RL
A1CR980	152-0601-00			SEMICOND DVC,DI:RECTIFIER,PLSTC,150V,25NS	04713	MUR115
A1CR981	152-0601-00			SEMICOND DVC,DI:RECTIFIER,PLSTC,150V,25NS	04713	MUR115
A1CR7201	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7202	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7203	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7301	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7302	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7303	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7304	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7305	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7306	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7307	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1CR7308	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A1DS856	150-0035-00			LAMP,GLOW:90V MAX,0.3MA,AID-T,WIRE LD	TK0213	JH005/3011JA
A1DS858	150-0035-00			LAMP,GLOW:90V MAX,0.3MA,AID-T,WIRE LD	TK0213	JH005/3011JA
A1DS870	150-0035-00			LAMP,GLOW:90V MAX,0.3MA,AID-T,WIRE LD	TK0213	JH005/3011JA
A1E200	276-0752-00			CORE,EM:FERRITE	34899	2743001111
A1E201	276-0752-00			CORE,EM:FERRITE	34899	2743001111
A1E272	276-0752-00			CORE,EM:FERRITE	34899	2743001111
A1E590	276-0752-00			CORE,EM:FERRITE	34899	2743001111
A1E907	276-0635-00			CORE,EM:TOROID,FERRITE	02114	768 T188/3E2A
A1J4210	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 4)	22526	48283-029
A1J9010	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 9)	22526	48283-036
A1J9050	131-2427-00			TERM,QIK DISC.:CKT BD,BRASS	00779	62409-1
A1J9060	131-2427-00			TERM,QIK DISC.:CKT BD,BRASS	00779	62409-1
A1J9210	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 7)	22526	48283-036
A1J9300	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 5)	22526	48283-036
A1J9320	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A1J9644	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A1J9802	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 5)	22526	48283-029
A1L142	108-0420-00			COIL,RF:FIXED,35NH,15%	TK2042	ORDER BY DESCR
A1L143	108-0420-00			COIL,RF:FIXED,35NH,15%	TK2042	ORDER BY DESCR

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1L192	108-0420-00			COIL,RF:FIXED,35NH,15%	TK2042	ORDER BY DESCR
A1L193	108-0420-00			COIL,RF:FIXED,35NH,15%	TK2042	ORDER BY DESCR
A1L960	108-1058-00			COIL,RF:FIXED,10UH	02113	B8724
A1L961	108-1058-00			COIL,RF:FIXED,10UH	02113	B8724
A1L962	108-1058-00			COIL,RF:FIXED,10UH	02113	B8724
A1L968	108-0554-00			COIL,RF:FIXED,5UH,+/-20%	TK1345	108-0554-00
A1P7390	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A1P7391	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A1P7392	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A1P7393	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A1Q102	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A1Q103	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A1Q114	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q115	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q152	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A1Q153	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A1Q164	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q165	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q202	151-0212-00			TRANSISTOR:NPN,SI,TO-72	04713	SRF 518
A1Q203	151-0212-00			TRANSISTOR:NPN,SI,TO-72	04713	SRF 518
A1Q206	151-0369-00			TRANSISTOR:PNP,SI,X-55	04713	SPS8273
A1Q207	151-0369-00			TRANSISTOR:PNP,SI,X-55	04713	SPS8273
A1Q230	151-0271-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8236
A1Q231	151-0271-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8236
A1Q254	151-0752-00			TRANSISTOR:NPN,SI,MARCO T	25403	BFR96
A1Q255	151-0752-00			TRANSISTOR:NPN,SI,MARCO T	25403	BFR96
A1Q256	151-0752-00			TRANSISTOR:NPN,SI,MARCO T	25403	BFR96
A1Q257	151-0752-00			TRANSISTOR:NPN,SI,MARCO T	25403	BFR96
A1Q282	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q283	151-0736-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0736-00
A1Q284	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A1Q285	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A1Q302	151-0711-01			TRANSISTOR:NPN,SI,TO-92	04713	SPS8608M
A1Q303	151-0711-01			TRANSISTOR:NPN,SI,TO-92	04713	SPS8608M
A1Q327	151-0711-01			TRANSISTOR:NPN,SI,TO-92	04713	SPS8608M
A1Q328	151-0711-01			TRANSISTOR:NPN,SI,TO-92	04713	SPS8608M
A1Q382	151-1042-00			SEMICOND DVC SE:FET,SI,TO-92	04713	SPF627M2
A1Q384	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A1Q397	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q413	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q419	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A1Q420	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A1Q421	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A1Q422	151-0199-00			TRANSISTOR:PNP,SI,TO-92	27014	ST65057
A1Q423	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1Q428	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A1Q429	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A1Q473	151-0276-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8025
A1Q474	151-0276-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8025
A1Q487	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1Q509	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q511	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q521	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q522	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q523	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q524	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q525	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q527	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1Q541	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q542	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q543	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q544	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q576	151-0199-00			TRANSISTOR:PNP,SI,TO-92	27014	ST65057
A1Q578	151-0199-00			TRANSISTOR:PNP,SI,TO-92	27014	ST65057
A1Q583	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A1Q586	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A1Q756	151-0432-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS8512
A1Q770	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q775	151-0347-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7951
A1Q779	151-0350-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6700
A1Q780	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q785	151-0347-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7951
A1Q789	151-0350-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6700
A1Q804	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q814	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q825	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A1Q829	151-0199-00			TRANSISTOR:PNP,SI,TO-92	27014	ST65057
A1Q835	151-0199-00			TRANSISTOR:PNP,SI,TO-92	27014	ST65057
A1Q840	151-0347-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7951
A1Q845	151-0350-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6700
A1Q908	151-0164-00			TRANSISTOR:PNP,SI,TO-92	04713	2N2907A
A1Q928	151-0432-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS8512
A1Q930	151-0164-00			TRANSISTOR:PNP,SI,TO-92	04713	2N2907A
A1Q935	151-0506-00			SCR:SI,RD-44	80009	151-0506-00
A1Q938	151-0276-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8025
A1Q939	151-0276-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8025
A1Q944	151-0432-00	B010100	B010269	TRANSISTOR:NPN,SI,TO-106	04713	SPS8512
A1Q944	151-0311-01	B010270		TRANSISTOR:NPN,SI,TO-126	04713	SJE908
A1Q946	151-0476-02	B010100	B011144	TRANSISTOR:SELECTED	04713	SJE389
A1Q946	151-0852-00	B011145		TRANSISTOR:	80009	151-0852-00
A1Q947	151-0476-02	B010100	B011144	TRANSISTOR:SELECTED	04713	SJE389
A1Q947	151-0852-00	B011145		TRANSISTOR: (Q946 AND Q947 MUST BE REPLACED AS A PAIR)	80009	151-0852-00
A1Q7201	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q7202	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q7203	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q7204	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A1Q7362	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A1Q7420	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q7440	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q7470	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q7471	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1Q7472	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A1R100	315-0430-00	B010100	B022629	RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A1R100	315-0620-00	B022630		RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1R101	315-0430-00	B010100	B022629	RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A1R101	315-0620-00	B022630		RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1R102	321-0155-00			RES,FXD,FILM:402 OHM,1%,0.125W,TC=T0	07716	CEAD402R0F
A1R103	321-0155-00			RES,FXD,FILM:402 OHM,1%,0.125W,TC=T0	07716	CEAD402R0F
A1R104	321-0101-00			RES,FXD,FILM:110 OHM,1%,0.125W,TC=T0	07716	CEAD110R0F
A1R105	321-0101-00			RES,FXD,FILM:110 OHM,1%,0.125W,TC=T0	07716	CEAD110R0F
A1R106	321-0161-00			RES,FXD,FILM:464 OHM,1%,0.125W,TC=T0	07716	CEAD464R0F
A1R108	321-0223-00			RES,FXD,FILM:2.05K OHM,1%,0.125W,TC=T0	19701	5033ED2K05F
A1R109	321-0221-00			RES,FXD,FILM:1.96K OHM,1%,0.125W,TC=T0	19701	5043ED1K960F
A1R114	321-0225-00			RES,FXD,FILM:2.15K OHM,1%,0.125W,TC=T0	19701	5033ED2K15F
A1R115	321-0225-00			RES,FXD,FILM:2.15K OHM,1%,0.125W,TC=T0	19701	5033ED2K15F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R122	321-0085-00			RES,FXD,FILM:75 OHM,1%,0.125W,TC=T0	57668	CRB14FXE 75 OHM
A1R125	315-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A1R126	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R130	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A1R131	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A1R132	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R133	315-0111-00			RES,FXD,FILM:110 OHM,5%,0.25W	57668	NTR25J-E110E
A1R135	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R136	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A1R138	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R139	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R142	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R143	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R144	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R145	311-1238-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3386X-DY6-502
A1R150	315-0430-00	B010100	B022629	RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A1R150	315-0620-00	B022630		RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1R151	315-0430-00	B010100	B022629	RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
A1R151	315-0620-00	B022630		RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1R152	321-0155-00			RES,FXD,FILM:402 OHM,1%,0.125W,TC=T0	07716	CEAD402R0F
A1R153	321-0155-00			RES,FXD,FILM:402 OHM,1%,0.125W,TC=T0	07716	CEAD402R0F
A1R154	321-0101-00			RES,FXD,FILM:110 OHM,1%,0.125W,TC=T0	07716	CEAD110R0F
A1R155	321-0101-00			RES,FXD,FILM:110 OHM,1%,0.125W,TC=T0	07716	CEAD110R0F
A1R156	321-0161-00			RES,FXD,FILM:464 OHM,1%,0.125W,TC=T0	07716	CEAD464R0F
A1R158	321-0223-00			RES,FXD,FILM:2.05K OHM,1%,0.125W,TC=T0	19701	5033ED2K05F
A1R159	321-0221-00			RES,FXD,FILM:1.96K OHM,1%,0.125W,TC=T0	19701	5043ED1K960F
A1R164	321-0225-00			RES,FXD,FILM:2.15K OHM,1%,0.125W,TC=T0	19701	5033ED2K15F
A1R165	321-0225-00			RES,FXD,FILM:2.15K OHM,1%,0.125W,TC=T0	19701	5033ED2K15F
A1R172	321-0085-00			RES,FXD,FILM:75 OHM,1%,0.125W,TC=T0	57668	CRB14FXE 75 OHM
A1R175	315-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A1R176	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R180	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A1R181	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A1R182	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R183	315-0111-00			RES,FXD,FILM:110 OHM,5%,0.25W	57668	NTR25J-E110E
A1R185	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R186	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A1R188	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R189	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R192	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R193	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R194	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R195	311-1238-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3386X-DY6-502
A1R200	315-0391-00	B010100	B010245	RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A1R200	315-0331-00	B010246		RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A1R202	321-0178-00			RES,FXD,FILM:698 OHM,1%,0.125W,TC=T0	07716	CEAD698R0F
A1R203	321-0178-00			RES,FXD,FILM:698 OHM,1%,0.125W,TC=T0	07716	CEAD698R0F
A1R204	321-0089-00			RES,FXD,FILM:82.5 OHM,1%,0.125W,TC=T0	91637	CMF55116G82R50F
A1R206	321-0139-00			RES,FXD,FILM:274 OHM,1%,0.125W,TC=T0	07716	CEAD274R0F
A1R207	321-0139-00			RES,FXD,FILM:274 OHM,1%,0.125W,TC=T0	07716	CEAD274R0F
A1R210	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W (NOMINAL VALUE)	57668	NTR25J-E220E
A1R210	315-0431-00	B020250		RES,FXD,FILM:430 OHM,5%,0.25W (SELECTED VALUE)	19701	5043CX430R0J
A1R212	321-0086-00			RES,FXD,FILM:76.8 OHM,1%,0.125W,TC=T0	91637	CMF55116G76R80F
A1R213	321-0086-00			RES,FXD,FILM:76.8 OHM,1%,0.125W,TC=T0	91637	CMF55116G76R80F
A1R215	321-0135-00			RES,FXD,FILM:249 OHM,1%,0.125W,TC=T0	07716	CEAD249R0F
A1R216	321-0163-00			RES,FXD,FILM:487 OHM,1%,0.125W,TC=T0	07716	CEAD487R0F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R217	321-0163-00			RES,FXD,FILM:487 OHM,1%,0.125W,TC=T0	07716	CEAD487R0F
A1R218	321-0102-00			RES,FXD,FILM:113 OHM,1%,0.125W,TC=T0	07716	CEAD113R0F
A1R219	321-0102-00			RES,FXD,FILM:113 OHM,1%,0.125W,TC=T0	07716	CEAD113R0F
A1R220	307-0104-00			RES,FXD,CMPSN:3.3 OHM,5%,0.25W	01121	CB33G5
A1R222	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A1R223	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A1R225	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R226	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R227	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R230	321-0086-00			RES,FXD,FILM:76.8 OHM,1%,0.125W,TC=T0	91637	CMF55116G76R80F
A1R231	321-0086-00			RES,FXD,FILM:76.8 OHM,1%,0.125W,TC=T0	91637	CMF55116G76R80F
A1R233	321-0086-00			RES,FXD,FILM:76.8 OHM,1%,0.125W,TC=T0	91637	CMF55116G76R80F
A1R234	315-0360-00			RES,FXD,FILM:36 OHM,5%,0.25W	19701	5043CX36R00J
A1R235	315-0360-00			RES,FXD,FILM:36 OHM,5%,0.25W	19701	5043CX36R00J
A1R236	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A1R239	315-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A1R240	311-1248-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3386X-T07-501
A1R241	311-1237-00			RES,VAR,NONWW:1K OHM,10%,0.50W	32997	3386X-DY6-102
A1R242	315-0273-00			RES,FXD,FILM:27K OHM,5%,0.25W	57668	NTR25J-E27K0
A1R244	321-0172-00			RES,FXD,FILM:604 OHM,1%,0.125W,TC=T0	19701	5033ED604R0F
A1R245	321-0172-00			RES,FXD,FILM:604 OHM,1%,0.125W,TC=T0	19701	5033ED604R0F
A1R250	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R251	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R254	321-0110-00			RES,FXD,FILM:137 OHM,1%,0.125W,TC=T0	07716	CEAD137R0F
A1R255	321-0110-00			RES,FXD,FILM:137 OHM,1%,0.125W,TC=T0	07716	CEAD137R0F
A1R256	322-0175-00			RES,FXD,FILM:649 OHM,1%,0.25W,TC=T0	75042	CEBT0-6490F
A1R257	322-0175-00			RES,FXD,FILM:649 OHM,1%,0.25W,TC=T0	75042	CEBT0-6490F
A1R258	322-0180-00			RES,FXD,FILM:732 OHM,1%,0.25W,TC=T0	75042	CEBT0-7320F
A1R259	322-0180-00			RES,FXD,FILM:732 OHM,1%,0.25W,TC=T0	75042	CEBT0-7320F
A1R261	323-0058-00			RES,FXD,FILM:39.2 OHM,1%,0.5W,TC=T0	57668	CRB11FX39R2E
A1R262	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1R266	323-0114-00			RES,FXD,FILM:150 OHM,1%,0.5W,TC=T0	75042	CECT0-1500F
A1R267	323-0114-00			RES,FXD,FILM:150 OHM,1%,0.5W,TC=T0	75042	CECT0-1500F
A1R268	323-0114-00			RES,FXD,FILM:150 OHM,1%,0.5W,TC=T0	75042	CECT0-1500F
A1R269	323-0114-00			RES,FXD,FILM:150 OHM,1%,0.5W,TC=T0	75042	CECT0-1500F
A1R270	323-0114-00			RES,FXD,FILM:150 OHM,1%,0.5W,TC=T0	75042	CECT0-1500F
A1R271	323-0114-00			RES,FXD,FILM:150 OHM,1%,0.5W,TC=T0	75042	CECT0-1500F
A1R278	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A1R279	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A1R281	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A1R282	315-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A1R283	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R284	315-0621-00			RES,FXD,FILM:620 OHM,5%,0.25W	57668	NTR25J-E620E
A1R285	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A1R286	321-0068-00			RES,FXD,FILM:49.9 OHM,0.5%,0.125W,TC=T0	91637	CMF55116G49R90F
A1R287	321-0068-00			RES,FXD,FILM:49.9 OHM,0.5%,0.125W,TC=T0	91637	CMF55116G49R90F
A1R288	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A1R289	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A1R292	321-0179-00			RES,FXD,FILM:715 OHM,1%,0.125W,TC=T0	07716	CEAD715R0F
A1R293	315-0620-00			RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1R301	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R302	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R303	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R304	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A1R305	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A1R306	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R307	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R309	311-2230-00			RES,VAR,NONWW:TRMR,500 OHM,20%,0.50 LINEAR	TK1450	GF06UT 500
A1R310	321-0194-00			RES,FXD,FILM:1.02K OHM,1%,0.125W,TC=T0	07716	CEAD10200F
A1R311	321-0194-00			RES,FXD,FILM:1.02K OHM,1%,0.125W,TC=T0	07716	CEAD10200F
A1R312	321-0098-00			RES,FXD,FILM:102 OHM,1%,0.125W,TC=T0	07716	CEAD102R0F
A1R314	321-0170-00			RES,FXD,FILM:576 OHM,1%,0.125W,TC=T0	07716	CEAD576R0F
A1R315	321-0170-00			RES,FXD,FILM:576 OHM,1%,0.125W,TC=T0	07716	CEAD576R0F
A1R317	321-0209-00			RES,FXD,FILM:1.47K OHM,1%,0.125W,TC=T0	19701	5033ED1K47F
A1R318	321-0198-00			RES,FXD,FILM:1.13K OHM,1%,0.125W,TC=T0	07716	CEAD11300F
A1R319	321-0213-00			RES,FXD,FILM:1.62K OHM,1%,0.125W,TC=T0	07716	CEAD16200F
A1R321	321-0208-00			RES,FXD,FILM:1.43K OHM,1%,0.125W,TC=T0	19701	5033ED1K43F
A1R322	321-0238-00			RES,FXD,FILM:2.94K OHM,1%,0.125W,TC=T0	07716	CEAD29400F
A1R324	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R326	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R327	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R328	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R329	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A1R330	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A1R331	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R332	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R335	321-0203-00			RES,FXD,FILM:1.27K OHM,1%,0.125W,TC=T0	07716	CEAD12700F
A1R336	321-0203-00			RES,FXD,FILM:1.27K OHM,1%,0.125W,TC=T0	07716	CEAD12700F
A1R337	321-0098-00			RES,FXD,FILM:102 OHM,1%,0.125W,TC=T0	07716	CEAD102R0F
A1R339	321-0170-00			RES,FXD,FILM:576 OHM,1%,0.125W,TC=T0	07716	CEAD576R0F
A1R340	321-0170-00			RES,FXD,FILM:576 OHM,1%,0.125W,TC=T0	07716	CEAD576R0F
A1R342	321-0209-00			RES,FXD,FILM:1.47K OHM,1%,0.125W,TC=T0	19701	5033ED1K47F
A1R343	321-0198-00			RES,FXD,FILM:1.13K OHM,1%,0.125W,TC=T0	07716	CEAD11300F
A1R344	321-0213-00			RES,FXD,FILM:1.62K OHM,1%,0.125W,TC=T0	07716	CEAD16200F
A1R346	321-0208-00			RES,FXD,FILM:1.43K OHM,1%,0.125W,TC=T0	19701	5033ED1K43F
A1R347	321-0238-00			RES,FXD,FILM:2.94K OHM,1%,0.125W,TC=T0	07716	CEAD29400F
A1R349	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R350	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R351	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R352	321-0275-00			RES,FXD,FILM:7.15K OHM,1%,0.125W,TC=T0	07716	CEAD71500F
A1R353	321-0275-00			RES,FXD,FILM:7.15K OHM,1%,0.125W,TC=T0	07716	CEAD71500F
A1R354	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R355	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R356	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25W	19701	5043CX6K200J
A1R357	321-0149-00			RES,FXD,FILM:348 OHM,1%,0.125W,TC=T0	07716	CEAD348R0F
A1R358	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R359	321-0148-00			RES,FXD,FILM:340 OHM,1%,0.125W,TC=T0	07716	CEAD340R0F
A1R360	321-0156-00			RES,FXD,FILM:412 OHM,1%,0.125W,TC=T0	07716	CEAD412R0F
A1R361	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R363	315-0331-00	B010100	B022101	RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A1R363	315-0470-00	B022102		RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R365	315-0620-00			RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A1R366	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A1R367	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1R369	315-0751-00			RES,FXD,FILM:750 OHM,5%,0.25W	57668	NTR25J-E750E
A1R372	315-0220-00			RES,FXD,FILM:22 OHM,5%,0.25W	19701	5043CX22R00J
A1R374	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A1R381	321-0444-00			RES,FXD,FILM:412K OHM,1%,0.125W,TC=T0	07716	CEAD41202F
A1R382	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R384	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A1R385	315-0130-00			RES,FXD,FILM:13 OHM,5%,0.25W	01121	CB1305
A1R386	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1R389	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R390	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R392	315-0751-00			RES,FXD,FILM:750 OHM,5%,0.25W	57668	NTR25J-E750E

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R393	315-0240-00			RES,FXD,FILM:24 OHM,5%,0.25W	57668	NTR25J-E24E0
A1R395	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1R397	315-0200-00			RES,FXD,FILM:20 OHM,5%,0.25W	19701	5043CX20R00J
A1R398	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A1R399	315-0751-00			RES,FXD,FILM:750 OHM,5%,0.25W	57668	NTR25J-E750E
A1R411	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R412	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R413	315-0113-00			RES,FXD,FILM:11K OHM,5%,0.25W	19701	5043CX11K00J
A1R414	315-0244-00			RES,FXD,FILM:240K OHM,5%,0.25W	19701	5043CX240K0J
A1R415	315-0244-00			RES,FXD,FILM:240K OHM,5%,0.25W	19701	5043CX240K0J
A1R416	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A1R417	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A1R419	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R420	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R421	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A1R422	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R423	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R424	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A1R426	315-0434-00			RES,FXD,FILM:430K OHM,5%,0.25W	57668	NTR25J-E430K
A1R427	315-0434-00			RES,FXD,FILM:430K OHM,5%,0.25W	57668	NTR25J-E430K
A1R428	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R429	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R432	315-0823-00			RES,FXD,FILM:82K OHM,5%,0.25W	57668	NTR25J-E82K
A1R433	315-0823-00			RES,FXD,FILM:82K OHM,5%,0.25W	57668	NTR25J-E82K
A1R434	311-1646-00			RES,VAR,NONWW:TRMR,2M OHM,0.5W	32997	3386X-T07-205
A1R435	311-1646-00			RES,VAR,NONWW:TRMR,2M OHM,0.5W	32997	3386X-T07-205
A1R446	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1R448	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A1R449	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A1R452	321-0130-00			RES,FXD,FILM:221 OHM,1%,0.125W,TC=T0	19701	5043ED221ROF
A1R453	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R454	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R455	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R457	321-0145-00			RES,FXD,FILM:316 OHM,1%,0.125W,TC=T0	07716	CEAD316R0F
A1R458	321-0182-00			RES,FXD,FILM:768 OHM,1%,0.125W,TC=T0	07716	CEAD768R0F
A1R459	321-0180-00			RES,FXD,FILM:732 OHM,1%,0.125W,TC=T0	07716	CEAD732R0F
A1R460	321-0141-00			RES,FXD,FILM:287 OHM,1%,0.125W,TC=T0	19701	5033ED287ROF
A1R461	321-0141-00			RES,FXD,FILM:287 OHM,1%,0.125W,TC=T0	19701	5033ED287ROF
A1R462	321-0194-00			RES,FXD,FILM:1.02K OHM,1%,0.125W,TC=T0	07716	CEAD10200F
A1R463	321-0215-00			RES,FXD,FILM:1.69K OHM,1%,0.125W,TC=T0	07716	CEAD16900F
A1R464	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A1R465	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A1R467	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A1R468	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A1R469	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A1R470	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A1R471	311-1237-00	B010100	B022633	RES,VAR,NONWW:1K OHM,10%,0.50W	32997	3386X-DY6-102
A1R471	311-1239-00	B022634		RES,VAR,NONWW:TRMR,2.5K OHM,0.5W	32997	3386X-T07-252
A1R473	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R474	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R476	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A1R477	315-0132-00			RES,FXD,FILM:1.3K OHM,5%,0.25W	57668	NTR25J-E01K3
A1R478	321-0215-00			RES,FXD,FILM:1.69K OHM,1%,0.125W,TC=T0	07716	CEAD16900F
A1R486	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R487	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R494	307-0104-00			RES,FXD,CMPSN:3.3 OHM,5%,0.25W	01121	CB33G5
A1R499	307-0104-00			RES,FXD,CMPSN:3.3 OHM,5%,0.25W	01121	CB33G5
A1R500	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R501	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R502	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1R503	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A1R504	315-0124-00			RES,FXD,FILM:120K OHM,5%,0.25W	19701	5043CX120K0J
A1R505	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A1R507	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A1R509	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A1R510	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R511	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A1R512	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W	57668	NTR25J-E04K3
A1R513	315-0391-00			RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A1R514	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R515	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R516	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A1R517	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W	57668	NTR25J-E04K3
A1R518	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R521	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R522	315-0363-00			RES,FXD,FILM:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A1R523	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A1R524	321-0318-00			RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A1R525	321-0322-00			RES,FXD,FILM:22.1K OHM,0.1%,0.125W,TC=T0	19701	5033ED22K10F
A1R526	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A1R527	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R528	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A1R529	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A1R530	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R531	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R532	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R533	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R534	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R535	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25W	19701	5043CX200K0J
A1R536	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W	57668	NTR25J-E390K
A1R537	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R538	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R539	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R540	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R541	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R542	315-0274-00			RES,FXD,FILM:270K OHM,5%,0.25W	57668	NTR25J-E270K
A1R543	315-0364-00			RES,FXD,FILM:360K OHM,5%,0.25W	57668	NTR25J-E360K
A1R544	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A1R545	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R546	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A1R547	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R548	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R549	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A1R550	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R551	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R552	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R553	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R554	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R555	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A1R556	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R558	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R560	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R561	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R562	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R564	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A1R565	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R565	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R568	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A1R569	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W	57668	NTR25J-E04K3
A1R571	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A1R572	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R573	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A1R574	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R576	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A1R577	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R578	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A1R580	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A1R581	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R582	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1R583	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R584	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R585	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R586	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R590	315-0183-00			RES,FXD,FILM:18K OHM,5%,0.25W	19701	5043CX18K00J
A1R595	315-0682-00	B010100	B010245	RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A1R595	315-0163-00	B010246		RES,FXD,FILM:16K OHM,5%,0.25W	57668	NTR25J-E 16K
A1R645	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A1R646	311-2231-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A1R648	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R649	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R675	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R676	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R756	315-0912-00			RES,FXD,FILM:9.1K OHM,5%,0.25W	57668	NTR25J-E09K1
A1R757	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A1R758	321-0336-00			RES,FXD,FILM:30.9K OHM,1%,0.125W,TC=T0	19701	5043ED30K90F
A1R759	321-0267-00			RES,FXD,FILM:5.90K OHM,1%,0.125_,TC=T0	19701	5033ED5K900F
A1R760	311-2229-00			RES,VAR,NONWW:TRMR,250 OHM,20%,0.5W LINEAR	TK1450	GF06UT 250
A1R761	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A1R764	315-0221-00	B010100	B011299	RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A1R764	315-0151-00	B011300		RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A1R766	321-0093-00			RES,FXD,FILM:90.9 OHM,1%,0.125W,TC=T0	19701	5043ED90R90F
A1R768	321-0162-00			RES,FXD,FILM:475 OHM,1%,0.125W,TC=T0	19701	5033ED475R0F
A1R770	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R773	321-0182-00			RES,FXD,FILM:768 OHM,1%,0.125W,TC=T0	07716	CEAD768R0F
A1R775	323-0310-00			RES,FXD,FILM:16.5K OHM,1%,0.5W,TC=T0	75042	CECT0-1652F
A1R776	321-0205-00			RES,FXD,FILM:1.33K OHM,1%,0.125W,TC=T0	19701	5033ED1K330F
A1R777	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R778	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R779	315-0243-00			RES,FXD,FILM:24K OHM,5%,0.25W	57668	NTR25J-E24K0
A1R780	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R782	321-0209-00			RES,FXD,FILM:1.47K OHM,1%,0.125W,TC=T0	19701	5033ED1K47F
A1R783	321-0201-00			RES,FXD,FILM:1.21K OHM,1%,0.125W,TC=T0	19701	5043ED1K210F
A1R785	323-0310-00			RES,FXD,FILM:16.5K OHM,1%,0.5W,TC=T0	75042	CECT0-1652F
A1R786	321-0205-00			RES,FXD,FILM:1.33K OHM,1%,0.125W,TC=T0	19701	5033ED1K330F
A1R787	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A1R788	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R789	315-0243-00			RES,FXD,FILM:24K OHM,5%,0.25W	57668	NTR25J-E24K0
A1R792	321-0263-00			RES,FXD,FILM:5.36K OHM,1%,0.125W,TC=T0	07716	CEAD53600F
A1R793	321-0361-00			RES,FXD,FILM:56.2K OHM,1%,0.125W,TC=T0	07716	CEAD56201F
A1R796	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R797	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R799	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R800	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A1R804	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R805	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A1R810	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A1R814	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R818	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R820	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A1R822	301-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.5W	19701	5053CX5K100J
A1R823	301-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.5W	19701	5053CX5K100J
A1R825	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A1R826	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1R828	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
A1R830	321-0212-00			RES,FXD,FILM:1.58K OHM,1%,0.125W,TC=70	19701	5033ED1K58F
A1R832	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A1R834	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R835	321-0228-00			RES,FXD,FILM:2.32K OHM,1%,0.125W,TC=T0	19701	5043ED2K32F
A1R836	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R840	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A1R841	322-0322-00			RES,FXD,FILM:22.1K OHM,1%,0.25W,TC=T0	19701	5034RD22K1
A1R842	315-0241-00			RES,FXD,FILM:240 OHM,5%,0.25W	19701	5043CX240R0J
A1R844	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1R845	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R849	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R851	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A1R852	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A1R853	315-0244-00			RES,FXD,FILM:240K OHM,5%,0.25W	19701	5043CX240K0J
A1R854	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R858	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A1R860	315-0625-00			RES,FXD,FILM:6.2M OHM,5%,0.25W	01121	CB6255
A1R870	311-2239-00			RES,VAR,NONWW:TRMR,100K OHM,20%,0.5W LINEAR	TK1450	GF06UT 100K
A1R871	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R872	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A1R873	315-0513-00			RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A1R874	311-2239-00			RES,VAR,NONWW:TRMR,100K OHM,20%,0.5W LINEAR	TK1450	GF06UT 100K
A1R875	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R877	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R886	315-0184-00			RES,FXD,FILM:180K OHM,5%,0.25W	19701	5043CX180K0J
A1R888	301-0514-00			RES,FXD,FILM:510K OHM,5%,0.5W	19701	5053CX510K0J
A1R889	301-0514-00			RES,FXD,FILM:510K OHM,5%,0.5W	19701	5053CX510K0J
A1R890	301-0514-00			RES,FXD,FILM:510K OHM,5%,0.5W	19701	5053CX510K0J
A1R891	301-0514-00			RES,FXD,FILM:510K OHM,5%,0.5W	19701	5053CX510K0J
A1R892	301-0514-00			RES,FXD,FILM:510K OHM,5%,0.5W	19701	5053CX510K0J
A1R893	311-1933-00			RES,VAR,NONWW:PNL,5M OHM,10%,0.5W	01121	23M909
A1R894	301-0514-00			RES,FXD,FILM:510K OHM,5%,0.5W	19701	5053CX510K0J
A1R905	301-0823-00			RES,FXD,FILM:82K OHM,5%,0.5W	19701	5053CX82K00J
A1R906	301-0823-00			RES,FXD,FILM:82K OHM,5%,0.5W	19701	5053CX82K00J
A1R907	308-0843-00			RES,FXD,WW:0.2 OHM,5%,1/0W	91637	RS1A-90-R2J
A1R908	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R909	315-0390-00			RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A1R910	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A1R912	321-0168-00			RES,FXD,FILM:549 OHM,1%,0.125W,TC=T0	07716	CEAD549R0F
A1R913	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A1R914	321-0378-00			RES,FXD,FILM:84.5K OHM,1%,0.125W,TC=T0	07716	CEAD84501F
A1R915	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A1R916	315-0514-00			RES,FXD,FILM:510K OHM,5%,0.25W	19701	5043CX510K0J
A1R917	315-0303-00			RES,FXD,FILM:30K OHM,5%,0.25W	19701	5043CX30K00J
A1R919	315-0113-00			RES,FXD,FILM:11K OHM,5%,0.25W	19701	5043CX11K00J
A1R921	315-0303-00			RES,FXD,FILM:30K OHM,5%,0.25W	19701	5043CX30K00J
A1R922	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A1R925	315-0124-00			RES,FXD,FILM:120K OHM,5%,0.25W	19701	5043CX120K0J

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R926	303-0154-00			RES,FXD,CMPSN:150K OHM,5%,1W	24546	FP1 150K OHM 5%
A1R927	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1R928	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A1R929	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A1R930	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A1R934	308-0441-00			RES,FXD,WW:3 OHM,5%,3W	14193	SA31-3R00J
A1R935	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A1R937	321-0234-00			RES,FXD,FILM:2.67K OHM,1%,0.125W,TC=T0	19701	5033ED2K67F
A1R938	311-1248-00			RES,VAR,NONWW:TRMR,500 OHM,0.5W	32997	3386X-T07-501
A1R939	321-0304-00			RES,FXD,FILM:14.3K OHM,1%,0.125W,TC=T0	19701	5033ED14K30F
A1R940	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25W	57668	NTR25J-E 20K
A1R941	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R942	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R943	301-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.5W	19701	5053CX4K700J
A1R944	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R945	301-0102-00	B010100	B010269	RES,FXD,FILM:1K OHM,5%,0.50W	19701	5053CX1K000J
A1R945	308-0298-00	B010270		RES,FXD,WW:560 OHM,5%,3W	00213	1240S-560-5
A1R946	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A1R947	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A1R948	315-0100-00	B010100	B020450	RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R948	315-0330-00	B020451		RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A1R949	308-0679-00			RES,FXD,WW:0.51 OHM,5%,2W	75042	BWH 0.51 OHM 5%
A1R953	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R954	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R964	307-0106-00			RES,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB 47G5
A1R965	307-0103-00			RES,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A1R966	307-0106-00			RES,FXD,CMPSN:4.7 OHM,5%,0.25W	01121	CB 47G5
A1R976	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R978	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A1R7111	321-0354-00			RES,FXD,FILM:47.5K OHM,1%,0.125W,TC=T0	19701	5043ED47K50F
A1R7117	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7203	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7204	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A1R7205	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7206	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A1R7207	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7208	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R7209	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7210	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7211	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7212	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7213	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W	19701	5043CX1K100J
A1R7214	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R7215	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R7216	315-0100-00	B010246		RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R7260	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R7261	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A1R7262	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A1R7263	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A1R7301	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R7360	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R7361	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A1R7420	315-0751-00			RES,FXD,FILM:750 OHM,5%,0.25W	57668	NTR25J-E750E
A1R7421	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A1R7430	315-0393-00			RES,FXD,FILM:39K OHM,5%,0.25W	57668	NTR25J-E39K0
A1R7431	315-0513-00			RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A1R7440	315-0823-00			RES,FXD,FILM:82K OHM,5%,0.25W	57668	NTR25J-E82K
A1R7441	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R7442	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A1R7470	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R7471	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1RT236	307-0125-00			RES,THERMAL:500 OHM,10%,NTC	15454	1DB501K-220-EC
A1S901	260-1849-00			SWITCH,PUSH:DPDT,4A,250VAC	31918	NE15/F2U103EE
A1T350	120-1680-00			TRANSFORMER,RF:5 TURN,BIBILAR	80009	120-1680-00
A1T390	120-1401-00			XFMR,TRIGGER:LINE,1:1 TURNS RATIO	54937	DMI 500-2044
A1T906	120-1439-00	B010100	B011390	TRANSFORMER,RF:ENERGY STORAGE	54937	5002573
A1T906	120-1439-01	B011391		TRANSFORMER,RF:ENERGY STORAGE	TK1339	120-1439-01
A1T944	120-1347-00			TRANSFORMER,RF:DRIVER SATURATING	54583	BDT-001
A1T948	120-1601-00	B010100	B020371	XFMR,PWR SDN&UP:HIGH VOLTAGE	80009	120-1601-00
A1T948	120-1601-01	B020372		XFMR,PWR SDN&UP:HIGH VOLTAGE	80009	120-1601-01
A1TP397	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1TP460	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1TP504	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1TP537	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1TP842	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1TP940	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1TP950	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1U130	155-0274-00			MICROCKT,LINEAR:VERTICAL PREAMP	80009	155-0274-00
A1U180	155-0274-00			MICROCKT,LINEAR:VERTICAL PREAMP	80009	155-0274-00
A1U225	156-0742-00			MICROCKT,LINEAR:OPNL AMPL	01295	LM318P
A1U310	156-0534-00			MICROCKT,LINEAR:DUAL DIFF AMPL	02735	CA3102E-98
A1U335	156-0534-00			MICROCKT,LINEAR:DUAL DIFF AMPL	02735	CA3102E-98
A1U350	156-1294-00			MICROCKT,LINEAR:NPN,5 TRANSISTOR ARRAY	02735	CA3127E
A1U426	156-0158-00			MICROCKT,LINEAR:DUAL OPNL AMPL	04713	MC1458P1/MC1458U
A1U460	234-0107-20			INTEGRATED CKT:SCHMITT TRIGGER	80009	234-0107-20
A1U501	156-1225-00			MICROCKT,LINEAR:DUAL COMPARATOR	01295	LM393P
A1U502	156-1713-00			MICROCKT,DGTL:ECL,RETRIG MONOSTABLE MV	04713	MC10198(P OR L)
A1U504	156-1335-00			MICROCKT,DGTL:LSTTL,DUAL RETRIGGERABLE	07263	96LS02PCQR
A1U506	156-1639-00			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	04713	MC10H131(P OR L)
A1U532	156-1641-00			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	04713	MC10H102(L OR P)
A1U537	156-0721-02	B010100	B022299	MICROCKT,DGTL:QUAD ST 2-INP NAND GATES	18324	N74LS132(NBORFB)
A1U537	156-0721-00	B022300		MICROCKT,DGTL:QUAD 2-INP ST NAND GATE	27014	DM74LS132N
A1U540	156-0388-03	B010100	B022299	MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A1U540	156-0388-00	B022300		MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74 N OR J
A1U555	156-0728-02	B010100	B022299	MICROCKT,DGTL:QUAD 2 INPUT GATE W/OC OUT	01295	SN74LS09NP3
A1U555	156-0728-00	B022300		MICROCKT,DGTL:QUAD 2-INP AND GATE W/OC OUT	01295	SN74LS09(N OR J)
A1U565	156-0384-02	B010100	B022299	MICROCKT,DGTL:QUAD 2-INP NAND GATE	07263	74LS03PCQR
A1U565	156-0384-00	B022300		MICROCKT,DGTL:QUAD 2-INP NAND GATE	01295	SN74LS03 N OR J
A1U758	156-1149-00			MICROCKT,LINEAR:OPERATIONAL AMP,JFET INPUT	27014	LF351N/GLEA134
A1U930	156-1627-00			MICROCKT,LINEAR:PULSE WIDTH MOD CONT CKT	12969	UC494ACN
A1U975	152-0806-00			SEMICOND DVC,DI:HV MULTR,4KVAC/12KVDC	12969	CMX647
A1U7201	156-0530-02	B010100	B022299	MICROCKT,DGTL:QUAD 2-INP MUX	01295	SN74LS157NP3
A1U7201	156-0530-00	B022300		MICROCKT,DGTL:QUAD 2-INP MUX	01295	SN74LS157N
A1U7202	156-0328-00			MICROCKT,DGTL:DUAL MOS CLOCK DRIVER	04713	MMH0026CP1D
A1VR645	152-0317-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.25W,DO-7	04713	SZG20012
A1VR712	152-0508-00			SEMICOND DVC,DI:ZEN,SI,12.6V,5%,0.4W,DO-7	04713	SZ13294RL
A1VR764	152-0508-00	B010100	B010831	SEMICOND DVC,DI:ZEN,SI,12.6V,5%,0.4W,DO-7	04713	SZ13294RL
A1VR764	152-0702-00	B010832		SEMICOND DVC,DI:ZEN,SI,13V,2%,500MW,DO-7	04713	SZG30214RL
A1VR782	152-0243-00			SEMICOND DVC,DI:ZEN,SI,15V,5%,0.4W,DO-7	04713	SZ13203 (1N965B)
A1VR828	152-0514-00			SEMICOND DVC,DI:ZEN,SI,10V,1%,0.4W,DO-7	04713	SZG15RL
A1VR925	152-0166-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.4W,DO-7	04713	SZ11738RL
A1VR935	152-0255-00			SEMICOND DVC,DI:ZEN,SI,51V,5%,0.4W,DO-7	04713	SZG35009K7
A1VR943	152-0317-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.25W,DO-7	04713	SZG20012
A1VR953	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A1VR954	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A1W282	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1W283	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W284	131-0566-00	B012600		BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W335	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W400	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W408	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W410	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W419	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W428	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W429	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W453	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W459	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W494	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W501	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W502	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W503	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W531	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W532	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W535	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W537	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W538	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W541	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W542	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W543	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W544	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W555	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W556	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W558	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W560	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W565	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W570	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W575	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W591	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W592	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W602	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W603	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W635	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W649	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W732	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W770	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W780	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W885	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W954	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W955	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W956	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W959	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W960	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W961	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W964	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W965	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W968	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W971	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W972	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W974	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W975	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W976	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W977	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W979	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W991	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1W992	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W993	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W995	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W997	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W998	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W999	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W2111	174-0032-00			CA ASSY,SP,ELEC:4,26 AWG,8.75 L,RIBBON	80009	174-0032-00
A1W2112	174-0032-00			CA ASSY,SP,ELEC:4,26 AWG,8.75 L,RIBBON	80009	174-0032-00
A1W7120	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7121	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7122	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7143	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7202	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7220	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7231	131-0566-00	B010100	B010245	BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7250	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7310	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1W7314	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1W7315	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1W7320	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7360	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1W7364	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1W7365	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A1W7420	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W7440	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W9000	179-2949-00			WIRING HARNESS:I/O	80009	179-2949-00
A1W9020	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W9035	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W9068	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A1W9070	198-4819-00			WIRE SET,ELEC:POWER FET	80009	198-4819-00
A1W9080	175-9852-00			CA ASSY,SP,ELEC:3,18 AWG,6.0 L,RIBBON	80009	175-9852-00
A1W9103	175-6138-00			CA ASSY,SP,ELEC:4,26 AWG,6.0 L,RIBBON	80009	175-6138-00
A1W9108	175-6138-00			CA ASSY,SP,ELEC:4,26 AWG,6.0 L,RIBBON	80009	175-6138-00
A1W9191	195-7747-00			LEAD,ELECTRICAL:18 AWG,3.5 L,8-19	80009	195-7747-00
A1W9300	175-9850-00			CA ASSY,SP,ELEC:5,22 AWG,7.0 L,RIBBON	80009	175-9850-00
A1W9700	175-9252-00			CABLE ASSY,RF:8,26 AWG/1,50 OHM COAX,8.0 L	80009	175-9252-00
A1W9705	175-6137-00			CA ASSY,SP,ELEC:8,26 AWG,6.0 L,RIBBON	80009	175-6137-00
A1W9778	195-7065-00	B010100	B021074	LEAD,ELECTRICAL:22 AWG,1.5 L,9-2	80009	195-7065-00
A1W9778	195-7064-00	B021075		LEAD,ELECTRICAL:22 AWG,2.25 L,9-N	80009	195-7064-00
A1W9788	195-7064-00			LEAD,ELECTRICAL:22 AWG,2.25 L,9-N	80009	195-7064-00
A1W9870	136-0830-00			SKT,PL-IN ELEK:CRT SOCKET ASSY	80009	136-0830-00
A1W9991	175-6139-00			CA ASSY,SP,ELEC:3,26 AWG,4.0 L,RIBBON	80009	175-6139-00
A2	670-8699-00			CIRCUIT BD ASSY:ATTENUATOR	80009	670-8699-00
A2AT1	307-1014-06			ATTENUATOR,FXD:100X	80009	307-1014-06
A2AT2	307-1013-00			ATTENUATOR,FXD:10X	80009	307-1013-00
A2AT51	307-1014-06			ATTENUATOR,FXD:100X	80009	307-1014-06
A2AT52	307-1013-00			ATTENUATOR,FXD:10X	80009	307-1013-00
A2C2	285-1106-00			CAP,FXD,PLASTIC:0.022UF,20%,600V	14752	230B1F223
A2C3	281-0158-00			CAP,VAR,CER DI:7-45PF,25V	59660	518-006 G 7-45
A2C6	283-0000-00			CAP,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-610-Y5U0102P
A2C7	283-0185-00	B010100	B022259	CAP,FXD,CER DI:2.5PF,0.5%,5CV	51642	100-050-NP0-259B
A2C7	283-0898-00	B022260		CAP,FXD,CER DI:2.7PF,50V,0.25%	51406	RPE110C062R7C50V
A2C9	281-0826-00			CAP,FXD,CER DI:2200PF,5%,100V	20932	401EM100AD222K
A2C10	283-0100-00			CAP,FXD,CER DI:0.0047UF,10%,200V	04222	SR306A472KAA
A2C13	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2C17	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2C21	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A2C26	281-0158-00			CAP,VAR,CER DI:7-45PF,25V	59660	518-006 G 7-45
A2C27	281-0893-00			CAP,FXD,CER DI:4.7PF,+/-0.5PF,100V	04222	MA101A4R7DAA
A2C30	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C35	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2C38	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2C52	285-1106-00			CAP,FXD,PLASTIC:0.022UF,20%,600V	14752	230B1F223
A2C53	281-0158-00			CAP,VAR,CER DI:7-45PF,25V	59660	518-006 G 7-45
A2C56	283-0000-00			CAP,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-610-Y5U0102P
A2C57	283-0185-00	B010100	B022259	CAP,FXD,CER DI:2.5PF,0.5%,50V	51642	100-050-NPO-259B
A2C57	283-0898-00	B022260		CAP,FXD,CER DI:2.7PF,50V,0.25%	51406	RPE110C062R7C50V
A2C59	281-0826-00			CAP,FXD,CER DI:2200PF,5%,100V	20932	401EM100AD222K
A2C60	283-0100-00			CAP,FXD,CER DI:0.0047UF,10%,200V	04222	SR306A472KAA
A2C63	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2C67	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2C71	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A2C76	281-0158-00			CAP,VAR,CER DI:7-45PF,25V	59660	518-006 G 7-45
A2C77	281-0893-00			CAP,FXD,CER DI:4.7PF,+/-0.5PF,100V	04222	MA101A4R7DAA
A2C80	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C85	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2C88	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2C90	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A2C91	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A2C93	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A2C94	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2C96	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A2C97	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C10ZMAA
A2CR7	152-0324-00			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-7	14552	MT5128
A2CR18	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR57	152-0324-00			SEMICOND DVC,DI:SW,SI,35V,0.1A,DO-7	14552	MT5128
A2CR68	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2L90	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A2L91	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A2L93	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A2L96	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A2P9091	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A2P9103	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A2P9108	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A2P9200	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	47359-000
A2Q13	151-1124-00			TRANSISTOR:JFE,N-CHAN,SI,SEL,TO-92	17856	J-2400
A2Q15	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A2Q18	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A2Q63	151-1124-00			TRANSISTOR:JFE,N-CHAN,SI,SEL,TO-92	17856	J-2400
A2Q65	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A2Q68	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A2R1	315-0620-02			RES,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A2R2	317-0105-00			RES,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A2R3	322-0614-00			RES,FXD,FILM:250K OHM,1%,0.25W,TC=T0	75042	CEBT0-2503F
A2R4	317-0082-00			RES,FXD,CMPSN:8.2 OHM,5%,0.125W	01121	BB82G5
A2R5	321-0469-00			RES,FXD,FILM:750K OHM,1%,0.125W,TC=T0	80009	321-0469-00
A2R6	317-0105-00			RES,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A2R7	315-0180-00	B010100	B010184	RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A2R7	315-0160-00	B010185		RES,FXD,FILM:16 OHM,5%,0.25W	19701	5043CX16R00J
A2R8	315-0620-02			RES,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2R9	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W	57668	NTR25J-E04K3
A2R10	311-2238-00			RES,VAR,NONWW:TRMR,50K OHM,20%,0.5W LINEAR	TK1450	GF06UT 50 K
A2R11	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A2R12	315-0360-00			RES,FXD,FILM:36 OHM,5%,0.25W	19701	5043CX36R00J
A2R12	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A2R12	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
				(R12 IS SELECTED)		
A2R13	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A2R14	317-0161-00			RES,FXD,CMPSN:160 OHM,5%,0.125W	01121	BB1615
A2R15	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A2R16	315-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.25W	19701	5043CX1K600J
A2R17	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A2R18	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A2R19	307-0843-00			RES NTWK,FXD,FI:INPUT ATTENUATOR	80009	307-0843-00
A2R21	315-0160-00			RES,FXD,FILM:16 OHM,5%,0.25W	19701	5043CX16R00J
A2R22	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A2R23	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A2R25	311-2226-00			RES,VAR,NONWW:TRMR,50 OHM,20%,0.5W	TK1450	GF06UT 50 OHM
A2R26	311-0643-00			RES,VAR,NONWW:TRMR,50 OHM,0.5W	32997	3329H-L58-500
A2R27	315-0160-00			RES,FXD,FILM:16 OHM,5%,0.25W	19701	5043CX16R00J
A2R29	321-0090-00			RES,FXD,FILM:84.5 OHM,1%,0.125W,TC=T0	91637	CMF55116G84R50F
A2R30	315-0124-00			RES,FXD,FILM:120K OHM,5%,0.25W	19701	5043CX120K0J
A2R31	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A2R33	311-2238-00			RES,VAR,NONWW:TRMR,50K OHM,20%,0.5W LINEAR	TK1450	GF06UT 50 K
A2R34	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A2R35	321-0144-00			RES,FXD,FILM:309 OHM,1%,0.125W,TC=T0	07716	CEAD309R0F
A2R37	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A2R38	321-0144-00			RES,FXD,FILM:309 OHM,1%,0.125W,TC=T0	07716	CEAD309R0F
A2R39	315-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A2R41	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A2R42	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A2R43	311-2218-00			RES,VAR,NONWW:PNL,10K OHM,20%,0.25W,DPST	01121	ORDER BY DESCR
A2R46	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A2R47	311-2230-00			RES,VAR,NONWW:TRMR,500 OHM,20%,0.50 LINEAR	TK1450	GF06UT 500
A2R48	315-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A2R51	315-0620-02			RES,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A2R52	317-0105-00			RES,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A2R53	322-0614-00			RES,FXD,FILM:250K OHM,1%,0.25W,TC=T0	75042	CEBT0-2503F
A2R54	317-0082-00			RES,FXD,CMPSN:8.2 OHM,5%,0.125W	01121	BB82G5
A2R55	321-0469-00			RES,FXD,FILM:750K OHM,1%,0.125W,TC=T0	80009	321-0469-00
A2R56	317-0105-00			RES,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A2R57	315-0180-00	B010100	B010184	RES,FXD,FILM:18 OHM,5%,0.25W	19701	5043CX18R00J
A2R57	315-0160-00	B010185		RES,FXD,FILM:16 OHM,5%,0.25W	19701	5043CX16R00J
A2R58	315-0620-02			RES,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A2R59	315-0432-00			RES,FXD,FILM:4.3K OHM,5%,0.25W	57668	NTR25J-E04K3
A2R60	311-2238-00			RES,VAR,NONWW:TRMR,50K OHM,20%,0.5W LINEAR	TK1450	GF06UT 50 K
A2R61	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A2R62	315-0360-00			RES,FXD,FILM:36 OHM,5%,0.25W	19701	5043CX36R00J
A2R62	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A2R62	315-0560-00			RES,FXD,FILM:56 OHM,5%,0.25W	57668	NTR25J-E56E0
				(R62 IS SELECTED)		
A2R63	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A2R64	317-0161-00			RES,FXD,CMPSN:160 OHM,5%,0.125W	01121	BB1615
A2R65	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A2R66	315-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.25W	19701	5043CX1K600J
A2R67	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A2R68	315-0911-00			RES,FXD,FILM:910 OHM,5%,0.25W	57668	NTR25J-E910E
A2R69	307-0843-00			RES NTWK,FXD,FI:INPUT ATTENUATOR	80009	307-0843-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2R71	315-0160-00			RES,FXD,FILM:16 OHM,5%,0.25W	19701	5043CX16R00J
A2R72	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A2R73	321-0210-00			RES,FXD,FILM:1.50K OHM,1%,0.125W,TC=T0	19701	5033ED1K50F
A2R75	311-2226-00			RES,VAR,NONWW:TRMR,50 OHM,20%,0.5W	TK1450	GF06UT 50 OHM
A2R76	311-0643-00			RES,VAR,NONWW:TRMR,50 OHM,0.5W	32997	3329H-L58-500
A2R77	315-0160-00			RES,FXD,FILM:16 OHM,5%,0.25W	19701	5043CX16R00J
A2R79	321-0090-00			RES,FXD,FILM:84.5 OHM,1%,0.125W,TC=T0	91637	CMF55116G84R50F
A2R80	315-0124-00			RES,FXD,FILM:120K OHM,5%,0.25W	19701	5043CX120K0J
A2R81	315-0750-00			RES,FXD,FILM:75 OHM,5%,0.25W	57668	NTR25J-E75E0
A2R83	311-2238-00			RES,VAR,NONWW:TRMR,50K OHM,20%,0.5W LINEAR	TK1450	GF06UT 50 K
A2R84	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A2R85	321-0144-00			RES,FXD,FILM:309 OHM,1%,0.125W,TC=T0	07716	CEAD309R0F
A2R87	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A2R88	321-0144-00			RES,FXD,FILM:309 OHM,1%,0.125W,TC=T0	07716	CEAD309R0F
A2R91	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A2R93	311-2218-00			RES,VAR,NONWW:PNL,10K OHM,20%,0.25W,DPST	01121	ORDER BY DESCR
A2R96	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A2R97	311-2230-00			RES,VAR,NONWW:TRMR,500 OHM,20%,0.50 LINEAR	TK1450	GF06UT 500
A2R98	315-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A2S1	263-1040-01			SWITCH ASSEMBLY:ACTUATOR,COUPLING	80009	263-1040-01
A2S10	263-1041-00			SWITCH ASSEMBLY:ACTUATOR,VOLTS/DIV	80009	263-1041-00
A2S43	----- -----			(PART OF R43)		
A2S51	263-1040-01			SWITCH ASSEMBLY:ACTUATOR,COUPLING	80009	263-1040-01
A2S60	263-1041-00			SWITCH ASSEMBLY:ACTUATOR,VOLTS/DIV	80009	263-1041-00
A2S93	----- -----			(PART OF R93)		
A2U10	156-2469-00			MICROCKT,DGTL:OP AMP	01295	TLC271ACP
A2U30	155-0273-00			MICROCKT,LINEAR:ATTEN AMPLIFIER	80009	155-0273-00
A2U60	156-2469-00			MICROCKT,DGTL:OP AMP	01295	TLC271ACP
A2U80	155-0273-00			MICROCKT,LINEAR:ATTEN AMPLIFIER	80009	155-0273-00
A2VR10	152-0744-00			SEMICOND DVC,DI:ZEN,SI,3.6V,5%,0.4W,DO-7	15238	IN747ATK
A2VR60	152-0744-00			SEMICOND DVC,DI:ZEN,SI,3.6V,5%,0.4W,DO-7	15238	IN747ATK
A2W43	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A2W93	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A2W94	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A2W96	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3	670-8710-00	B010100	B019999	CIRCUIT BD ASSY:FR PNL	80009	670-8710-00
A3	670-8710-01	B020000		CIRCUIT BD ASSY:FRONT PNL	80009	670-8710-01
A3C376	283-0006-00			CAP,FXD,CER DI:0.02UF,+80-20%,500V	59660	0841545Z5V00203Z
A3C377	281-0576-00			CAP,FXD,CER DI:11PF,5%,500V	52763	2RDPLZ007 MPOJC
A3C379	283-0780-00			CAP,FXD,MICA DI:125PF,1%,500V	00853	D155F1250F0
A3C380	281-0578-00			CAP,FXD,CER DI:18PF,5%,500V	52763	2RDPLZ007 18POJC
A3C901	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A3C905	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C905	281-0775-01	B010552		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C987	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A3CR534	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A3CR537	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A3CR538	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A3CR539	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A3CR648	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A3CR988	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A3CR989	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A3DS518	150-1029-00			LT EMITTING DIO:GREEN,565NM,35MA	58361	Q6480/MV5274C
A3J9006	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	48283-029
A3J9200	136-0499-02			CONN,RCPT,ELEC:CIRCUIT BD,2 CONTACTS	00779	3-380949-2
A3J9250	136-0499-02			CONN,RCPT,ELEC:CIRCUIT BD,2 CONTACTS	00779	3-380949-2

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
				(QUANTITY OF 2)		
A3Q7410	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A3R89	315-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A3R92	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A3R111	321-0251-00			RES,FXD,FILM:4.02K OHM,1%,0.125W,TC=T0	19701	5033ED4K020F
A3R112	311-2178-00			RES,VAR,NONWW:CKT BD,500 OHM,10%,0.5W	12697	CM43473
A3R161	321-0251-00			RES,FXD,FILM:4.02K OHM,1%,0.125W,TC=T0	19701	5033ED4K020F
A3R162	311-2178-00			RES,VAR,NONWW:CKT BD,500 OHM,10%,0.5W	12697	CM43473
A3R224	315-0200-00			RES,FXD,FILM:20 OHM,5%,0.25W	19701	5043CX20R00J
A3R280	311-2147-00			RES,VAR,NONWW:CKT BD,5K OHM,20%,0.50W	12697	CM41769
A3R377	321-0807-00			RES,FXD,FILM:900K OHM,1%,0.125W,TC=T0	19701	5033RD900K0F
A3R378	321-0617-00			RES,FXD,FILM:111K OHM,1%,0.125W,TC=T0	19701	5043ED250K0F
A3R379	315-0220-00			RES,FXD,FILM:22 OHM,5%,0.25W	19701	5043CX22R00J
A3R380	321-0459-00			RES,FXD,FILM:590K OHM,1%,0.125W,TC=T0	19701	5043ED590K0F
A3R401	315-0200-00			RES,FXD,FILM:20 OHM,5%,0.25W	19701	5043CX20R00J
A3R438	311-2284-00			RES,VAR,NONWW:CKT BD,500 OHM,10%,0.25W,SPST	12697	CM43479
A3R519	315-0563-00			RES,FXD,FILM:56K OHM,5%,0.25W	19701	5043CX56K00J
A3R520	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A3R602	311-2147-00			RES,VAR,NONWW:CKT BD,5K OHM,20%,0.50W	12697	CM41769
A3R726	311-2147-00			RES,VAR,NONWW:CKT BD,5K OHM,20%,0.50W	12697	CM41769
A3R951	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A3R952	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A3R960	311-2286-00			RES,VAR,NONWW:CKT BD,10K OHM,20%,0.5W	12697	CM43461
A3R961	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A3R982	311-1560-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3352T-1-502
A3R983	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A3R985	315-0114-00			RES,FXD,FILM:110K OHM,5%,0.25W	19701	5043CX110K0J
A3R986	315-0434-00			RES,FXD,FILM:430K OHM,5%,0.25W	57668	NTR25J-E430K
A3R987	315-0124-00			RES,FXD,FILM:120K OHM,5%,0.25W	19701	5043CX120K0J
A3R988	315-0182-00			RES,FXD,FILM:1.8K OHM,5%,0.25W	57668	NTR25J-E1K8
A3R989	321-0239-00			RES,FXD,FILM:3.01K OHM,1%,0.125W,TC=T0	19701	5043ED3K010F
A3R990	321-0126-00			RES,FXD,FILM:200 OHM,1%,0.125W,TC=T0	19701	5033ED200R0F
A3R7362	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A3R7401	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A3R7402	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25W	19701	5043CX6K200J
A3R7403	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A3S90	260-1995-00			SWITCH,PUSH:1 BUTTON,2 POLE,SLOPE	71590	K40352AB
A3S200	260-2075-00			SWITCH,PUSH:SPDT,50VDC,500M AMP	80009	260-2075-00
A3S226	260-2075-00			SWITCH,PUSH:SPDT,50VDC,500M AMP	80009	260-2075-00
A3S380	260-2033-00			SWITCH,SLIDE:DPTT,125V,0.5A	82389	ORDER BY DESCR
A3S390	260-2111-00			SWITCH,PUSH:SPDT,MOMENTARY	59821	2LL199NB021085
A3S392	260-2033-00			SWITCH,SLIDE:DPTT,125V,0.5A	82389	ORDER BY DESCR
A3S401	260-2110-00			SWITCH,PUSH:1 SPDT/2 DPDT	59821	ORDER BY DESCR
A3S438	----- -----			(PART OF R438)		
A3S460	260-2075-00			SWITCH,PUSH:SPDT,50VDC,500M AMP	80009	260-2075-00
A3S545	260-2033-00			SWITCH,SLIDE:DPTT,125V,0.5A	82389	ORDER BY DESCR
A3S550	260-2033-00			SWITCH,SLIDE:DPTT,125V,0.5A	82389	ORDER BY DESCR
A3S555	260-2033-00			SWITCH,SLIDE:DPTT,125V,0.5A	82389	ORDER BY DESCR
A3S602	260-2075-00			SWITCH,PUSH:SPDT,50VDC,500M AMP	80009	260-2075-00
A3S648	260-2033-00			SWITCH,SLIDE:DPTT,125V,0.5A	82389	ORDER BY DESCR
A3S7401	260-2075-00			SWITCH,PUSH:SPDT,50VDC,500M AMP	80009	260-2075-00
A3U985	156-0067-00			MICROCKT,LINEAR:OPNL AMPL,SEL	04713	MC1741CP1
A3W515	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W534	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W539	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W630	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W901	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W902	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A3W903	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W904	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W7457	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W7458	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W9000	131-3345-00			TERM SET,PIN:HEADER,MALE,24 PIN	TK1483	082-2940-SS45
A3W9000	131-3346-00			TERM SET,PIN:HEADER,MALE,21 PIN	TK1483	082-3040-SS46
A3W9520	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W9521	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A3W9900						
A4	670-8709-00	B010100	B012199	CIRCUIT BD ASSY:TIMING	80009	670-8709-00
A4	670-8709-02	B012200	B022101	CIRCUIT BD ASSY:TIMING	80009	670-8709-02
A4	670-8709-02	B022102		CIRCUIT BD ASSY:TIMING	80009	670-8709-02
A4C673	281-0797-00			CAP,FXD,CER DI:15PF,10%,100V	04222	MA106A150KAA
A4C701	295-0003-00			CAP SET,MATCHED:1,1.0UF,1.5%,50V,0.0.0.1UF	80009	295-0003-00
A4C702	283-0674-00			CAP,FXD,MICA DI:85PF,1%,500V	00853	D155F850F0
A4C703	281-0207-00			CAP,VAR,PLASTIC:2-18PF,100V	52769	GXA 18000
A4C705	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A4C706	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A4C707	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C708	281-0756-00			CAP,FXD,CER DI:2.2PF,+/-0.5PF,200V	04222	MA106A2R2DAA
A4C710	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A4C712	283-0674-00			CAP,FXD,MICA DI:85PF,1%,500V	00853	D155F850F0
A4C713	281-0207-00			CAP,VAR,PLASTIC:2-18PF,100V	52769	GXA 18000
A4C714	281-0756-00			CAP,FXD,CER DI:2.2PF,+/-0.5PF,200V	04222	MA106A2R2DAA
A4C720	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C724	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A4C728	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A4C749	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C750	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A4C751	281-0809-00			CAP,FXD,CER DI:200 PF,5%,100V	04222	MA101A201JAA
A4C752	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C755	283-0107-00			CAP,FXD,CER DI:51PF,5%,200V	04222	SR206A510JAA
A4CR732	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR742	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR760	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4CR761	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A4J9700	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 10)	22526	48283-036
A4J9705	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 8)	22526	48283-036
A4P9250	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ (QUANTITY OF 3)	22526	47359-000
A4Q701	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A4Q704	151-1042-00			SEMICOND DVC SE:FET,SI,TO-92	04713	SPF627M2
A4Q706	151-0736-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0736-00
A4Q709	151-0424-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8246
A4Q710	151-1042-00			SEMICOND DVC SE:FET,SI,TO-92	04713	SPF627M2
A4Q712	151-0736-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0736-00
A4Q732	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A4Q737	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A4Q742	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A4R673	317-0472-02	B010100	B022093	RES,FXD,CMPSN:4.7K OHM,5%,0.125W MI	57668	TR20JE-04K7
A4R673	313-1472-00	B022094		RES,FXD,FILMN:4.7K OHM,5%,0.2W	57668	TR20JE 04K7
A4R701	307-0780-01			RES NTWK,FXD,FI:TIMING	80009	307-0780-01
A4R702	322-0519-01			RES,FXD,FILM:2.49M OHM,0.5%,0.25W,TC=T0	07716	CCAD24903D
A4R703	317-0100-02	B010100	B022093	RES,FXD,CMPSN:10 OHM,5%,0.125W	57668	TR20J-E10E
A4R703	313-1100-00	B022094		RES,FXD,FILM:10 OHM,5%,0.2W	57668	TR20JE10E0
A4R704	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25W	19701	5043CX6K200J

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A4R705	317-0151-03	B010100	B022093	RES,FXD,CMPSN:150 OHM,5%,0.125W	57668	TR20J-E150E
A4R705	313-1151-00	B022094		RES,FXD,FILM:150 OHM,5%,0.2W	57668	TR20JE150E
A4R707	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A4R709	317-0100-02	B010100	B022093	RES,FXD,CMPSN:10 OHM,5%,0.125W	57668	TR20J-E10E
A4R709	313-1100-00	B022094		RES,FXD,FILM:10 OHM,5%,0.2W	57668	TR20JE10E0
A4R710	317-0151-03	B010100	B022093	RES,FXD,CMPSN:150 OHM,5%,0.125W	57668	TR20J-E150E
A4R710	313-1151-00	B022094		RES,FXD,FILM:150 OHM,5%,0.2W	57668	TR20JE150E
A4R711	307-0780-01			RES NTWK,FXD,FI:TIMING	80009	307-0780-01
A4R713	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A4R724	317-0100-02	B010100	B022093	RES,FXD,CMPSN:10 OHM,5%,0.125W	57668	TR20J-E10E
A4R724	313-1100-00	B022094		RES,FXD,FILM:10 OHM,5%,0.2W	57668	TR20JE10E0
A4R727	321-0246-00			RES,FXD,FILM:3.57K OHM,1%,0.125W,TC=T0	19701	5043ED3K570F
A4R728	321-0211-00			RES,FXD,FILM:1.54K OHM,1%,0.125W,TC=T0	07716	CEAD15400F
A4R730	311-2231-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A4R731	321-0244-00	B010100	B010399	RES,FXD,FILM:3.40K OHM,1%,0.125W,TC=T0	19701	5043ED3K400F
A4R731	321-0240-00	B010400		RES,FXD,FILM:3.09K OHM,1%,0.125W,TC=T0	07716	CEAD30900F
A4R732	321-0198-00			RES,FXD,FILM:1.13K OHM,1%,0.125W,TC=T0	07716	CEAD11300F
A4R733	321-0203-00			RES,FXD,FILM:1.27K OHM,1%,0.125W,TC=T0	07716	CEAD12700F
A4R737	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A4R738	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A4R740	311-2231-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A4R741	321-0244-00	B010100	B010399	RES,FXD,FILM:3.40K OHM,1%,0.125W,TC=T0	19701	5043ED3K400F
A4R741	321-0240-00	B010400		RES,FXD,FILM:3.09K OHM,1%,0.125W,TC=T0	07716	CEAD30900F
A4R742	321-0198-00			RES,FXD,FILM:1.13K OHM,1%,0.125W,TC=T0	07716	CEAD11300F
A4R743	321-0203-00			RES,FXD,FILM:1.27K OHM,1%,0.125W,TC=T0	07716	CEAD12700F
A4R744	315-0101-00	B010100	B010245	RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R744	315-0470-00	B010246		RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A4R745	321-0177-00			RES,FXD,FILM:681 OHM,1%,0.125W,TC=T0	07716	CEAD681R0F
A4R746	321-0184-00	B010100	B012199	RES,FXD,FILM:806 OHM,1%,0.125W,TC=T0	19701	5033ED806R0F
A4R746	321-0133-00	B012200	B012337	RES,FXD,FILM:237 OHM,1%,0.125W,TC=T0	07716	CEAD237R0F
A4R746	321-0128-00	B012338	B022101	RES,FXD,FILM:210 OHM,1%,0.125W,TC=T0	07716	CEAD210R0F
A4R746	321-0133-00	B022102		RES,FXD,FILM:237 OHM,1%,0.125W,TC=T0	07716	CEAD237R0F
A4R747	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R748	315-0113-00			RES,FXD,FILM:11K OHM,5%,0.25W	19701	5043CX11K00J
A4R749	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A4R750	315-0113-00			RES,FXD,FILM:11K OHM,5%,0.25W	19701	5043CX11K00J
A4R751	321-0326-00			RES,FXD,FILM:24.3K OHM,1%,0.125W,TC=T0	19701	5043ED24K30F
A4R752	317-0100-02	B010100	B022093	RES,FXD,CMPSN:10 OHM,5%,0.125W	57668	TR20J-E10E
A4R752	313-1100-00	B022094		RES,FXD,FILM:10 OHM,5%,0.2W	57668	TR20JE10E0
A4R753	321-0216-00			RES,FXD,FILM:1.74K OHM,1%,0.125W,TC=T0	07716	CEAD17400F
A4R754	311-2227-00			RES,VAR,NONWW:TRMR,100 OHM,20%,0.5W LINEAR	TK1450	GF06UT 100
A4R755	315-0620-00			RES,FXD,FILM:62 OHM,5%,0.25W	19701	5043CX63R00J
A4R763	315-0224-00			RES,FXD,FILM:220K OHM,5%,0.25W	57668	NTR25J-E220K
A4R765	321-0414-00			RES,FXD,FILM:200K OHM,1%,0.125W,TC=T0	07716	CEAD20002F
A4R767	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A4R769	315-0163-00			RES,FXD,FILM:16K OHM,5%,0.25W	57668	NTR25J-E 16K
A4R771	317-0473-02	B010100	B011439	RES,FXD,CMPSN:47K OHM,5%,0.125W	57668	TR20J-E47K0
A4R771	317-0104-00	B011440	B011872	RES,FXD,CMPSN:100K OHM,5%,0.125W	01121	BB1045
A4R771	313-1104-00	B011873		RES,FXD,FILM:100K OHM,5%,0.2W	57668	TR20JE100K
A4R772	315-0473-00	B010100	B011439	RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A4R772	315-0104-00	B011440		RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A4R774	315-0224-00			RES,FXD,FILM:220K OHM,5%,0.25W	57668	NTR25J-E220K
A4R781	321-0385-00			RES,FXD,FILM:100K OHM,1%,0.125W,TC=T0	19701	5033ED100K0F
A4R790	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A4S701	260-2023-02			SWITCH,ROTARY:TIMING,A/B SWEEP	80009	260-2023-02
A4U715	156-1191-01			MICROCKT,LINEAR:DUAL BI-FET OP-AMP,8 DIP	80009	156-1191-01
A4U750	156-1150-00			MICROCKT,LINEAR:VOLTAGE REGULATOR,NEGATIVE	04713	MC79L05ACP
A4U751	156-0991-00			MICROCKT,LINEAR:VOLTAGE REGULATOR	04713	MC78L05ACP

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A4U760	155-0124-00			MICROCKT,LINEAR:HORIZ PREAMP	80009	155-0124-00
A4VR746	152-0667-00	B012200		SEMICOND DVC,DI:ZEN,SI,3.0 V # 2% AT 2MA	04713	SZG30025RL
A4VR749	152-0149-00			SEMICOND DVC,DI:ZEN,SI,10V,5%,0.4W,DO-7	15238	Z5406
A5	670-8711-00	B010100	B022042	CIRCUIT BD ASSY:ALT SW	80009	670-8711-00
A5	670-8711-01	B022043		CIRCUIT BD ASSY:ALTERNATE SWEEP	80009	670-8711-01
A5C605	281-0771-00			CAP,FXD,CER DI:2200PF,20%,200V	04222	MA106E222MAA
A5C606	290-0776-00			CAP,FXD,ELCTLT:22UF,+50-10 %,10V	55680	ULA1A220TAA
A5C610	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C102MAA
A5C643	281-0811-00			CAP,FXD,CER DI:10PF,10%,100V	04222	MA101A100KAA
A5C655	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A5C657	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C102MAA
A5C659	281-0773-00	B010100	B022042	CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A5C659	290-0246-00	B022043		CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A5C665	281-0797-00			CAP,FXD,CER DI:15PF,10%,100V	04222	MA106A150KAA
A5C667	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A5C672	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A5C694	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5CR625	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR626	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR680	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR684	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR685	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR687	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5CR816	152-0153-00			SEMICOND DVC,DI:SW,SI,10V,50MA,.DO-7	07263	FD7003
A5CR817	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A5J4220	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A5L667	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A5Q630	151-0369-00			TRANSISTOR:PNP,SI,X-55	04713	SPS8273
A5Q631	151-0369-00			TRANSISTOR:PNP,SI,X-55	04713	SPS8273
A5Q637	151-0276-01			TRANSISTOR:PNP,SI,TO-92	TK1016	S1423-TPE2
A5Q643	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A5Q670	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q674	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q682	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q683	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A5Q684	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A5Q687	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A5R604	321-0180-00			RES,FXD,FILM:732 OHM,1%,0.125W,TC=T0	07716	CEAD732R0F
A5R605	321-0141-00			RES,FXD,FILM:287 OHM,1%,0.125W,TC=T0	19701	5033ED287R0F
A5R606	321-0196-00			RES,FXD,FILM:1.07K OHM,1%,0.125W,TC=T0	07716	CEAD10700F
A5R609	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A5R610	315-0241-00			RES,FXD,FILM:240 OHM,5%,0.25W	19701	5043CX240R0J
A5R611	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A5R613	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A5R614	321-0130-00			RES,FXD,FILM:221 OHM,1%,0.125W,TC=T0	19701	5043ED221R0F
A5R616	321-0145-00			RES,FXD,FILM:316 OHM,1%,0.125W,TC=T0	07716	CEAD316R0F
A5R617	321-0182-00			RES,FXD,FILM:768 OHM,1%,0.125W,TC=T0	07716	CEAD768R0F
A5R618	321-0141-00			RES,FXD,FILM:287 OHM,1%,0 125W,TC=T0	19701	5033ED287R0F
A5R619	321-0215-00			RES,FXD,FILM:1.69K OHM,1%,0.125W,TC=T0	07716	CEAD16900F
A5R621	321-0215-00			RES,FXD,FILM:1.69K OHM,1%,0.125W,TC=T0	07716	CEAD16900F
A5R623	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A5R624	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A5R625	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R626	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R627	311-1237-00	B010100	B022633	RES,VAR,NONWW:1K OHM,10%,0.50W	32997	3386X-DY6-102

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5R627	311-1239-00	B022634		RES,VAR,NONWW:TRMR,2.5K OHM,0.5W	32997	3386X-T07-252
A5R628	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R630	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A5R631	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A5R632	315-0201-00			RES,FXD,FILM:200 OHM,5%,0.25W	57668	NTR25J-E200E
A5R633	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A5R634	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A5R637	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A5R638	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R640	315-0185-00			RES,FXD,FILM:1.8M OHM,5%,0.25W	01121	CB1855
A5R642	321-0314-00			RES,FXD,FILM:18.2K OHM,1%,0.125W,TC=T0	19701	5043ED18K20F
A5R643	321-0322-00			RES,FXD,FILM:22.1K OHM,0.1%,0.125W,TC=T0	19701	5033ED22K10F
A5R644	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R650	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R651	321-0277-00			RES,FXD,FILM:7.50K OHM,1%,0.125W,TC=T0	24546	NA55D7501F
A5R652	311-1238-00			RES,VAR,NONWW:TRMR,5K OHM,0.5W	32997	3386X-DY6-502
A5R653	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A5R655	315-0470-00	B022043		RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A5R657	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R659	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A5R660	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R662	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A5R663	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R664	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A5R665	315-0513-00			RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A5R667	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A5R668	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A5R669	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R670	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R671	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R672	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A5R674	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R678	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A5R679	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A5R682	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A5R683	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A5R684	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A5R686	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A5R687	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A5R688	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A5R689	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5R816	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A5R817	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A5U605	234-0107-20			INTEGRATED CKT:SCHMITT TRIGGER	80009	234-0107-20
A5U655	156-1126-00			MICROCKT,LINEAR:VOLTAGE COMPARATOR	01295	LM311P
A5U660	156-0385-02	B010100	B022299	MICROCKT,DGTL:HEX INVERTER	07263	74LS04PCQR
A5U660	156-0385-00	B022300		MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A5U665	156-0382-02	B010100	B022299	MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A5U665	156-0382-00	B022300		MICROCKT,DGTL:QUAD 2-INP NAND GATE	01295	SN74LS00(N OR J)
A5U670	156-1639-00			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	04713	MC10H131(P OR L)
A5U680	156-0382-02	B010100	B022299	MICROCKT,DGTL:QUAD 2 INP NAND GATE BURN	18324	N74LS00NB
A5U680	156-0382-00	B022300		MICROCKT,DGTL:QUAD 2-INP NAND GATE	01295	SN74LS00(N OR J)
A5VR660	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A5W638	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W643	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W655	131-0566-00	B010100	B022042	BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W668	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W672	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5W678	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W690	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W691	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W695	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W696	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A5W9400	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 27)	22526	48283-029
A6	670-7615-00			CIRCUIT BD ASSY:EMI FILTER	80009	670-7615-00
A6C900	285-1252-00			CAP,FXD,PLASTIC:0.15UF,10%,250VAC	D5243	F1772-415-2000
A6C902	285-1192-00			CAP,FXD,PPR DI:0.0022 UF,20%,250VAC	TK0515	PME271Y510
A6C903	285-1192-00			CAP,FXD,PPR DI:0.0022 UF,20%,250VAC	TK0515	PME271Y510
A6R900	301-0474-00			RES,FXD,FILM:470K OHM,5%,0.5W	19701	5053CX470K0J
A6R901	301-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.5W	19701	5053CX5K100J
A6R903	301-0131-00			RES,FXD,FILM:130 OHM,5%,0.5W	19701	5053CX130R0J
A6RT901	307-0863-00			RES,THERMAL:10 OHM,10%,NTC	15454	SG-13S
A6T901	120-1449-00			TRANSFORMER,RF:COMMON MODE,2.7MH,2A	02113	P104
A6T903	120-1455-00			TRANSFORMER,RF:DIFFERENTIAL MODE,POT CORE	TK1421	120-1455-00
A6VR901	307-0456-00			RES,V SENSITIVE:250VAC,15W,METAL OXIDE	03508	MOV-V250LA15A
A6W9011	196-0531-00			LEAD,ELECTRICAL:18 AWG,3.0 L,8-01	80009	196-0531-00
A6W9041	195-7745-00			LEAD,ELECTRICAL:18 AWG,3.5 L,8-04	80009	195-7745-00
A6W9091	196-0505-00			LEAD,ELECTRICAL:18 AWG,3.0 L,8-9	80009	196-0505-00
A6W9191	195-7747-00			LEAD,ELECTRICAL:18 AWG,3.5 L,8-19	80009	195-7747-00
A7	----- -----			CIRCUIT BD ASSY:INTENS POT (SEE R9802 REPL)		
A10	670-8702-00	B010100	B019999	CIRCUIT BD ASSY:STORAGE	80009	670-8702-00
A10	670-8702-01	B020000	B021984	CIRCUIT BD ASSY:STORAGE	80009	670-8702-01
A10	670-8702-02	B021985		CIRCUIT BD ASSY:STORAGE	80009	670-8702-02
A10C2101	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V	04222	MA101A100MAA
A10C2102	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V	04222	MA101A100MAA
A10C2103	281-0123-00			CAP,VAR,CER DI:5-25PF,100V	59660	518-000A5-25
A10C2104	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A10C2111	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V	04222	MA101A100MAA
A10C2112	281-0757-00			CAP,FXD,CER DI:10PF,20%,100V	04222	MA101A100MAA
A10C2113	281-0123-00			CAP,VAR,CER DI:5-25PF,100V	59660	518-000A5-25
A10C2114	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A10C2115	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C2116	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C2117	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2118	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2119	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2120	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2123	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2151	283-0260-00			CAP,FXD,CER DI:5.6PF,+/-0.25PF,200V	51642	150 200NP0569C
A10C2152	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2153	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2154	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2203	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2206	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2224	281-0758-00			CAP,FXD,CER DI:15PF,20%,100V	04222	MA101A150MAA
A10C2225	281-0756-00			CAP,FXD,CER DI:2.2PF,+/-0.5PF,200V	04222	MA106A2R2DAA
A10C2226	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2228	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2229	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2230	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10C2233	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A10C2235	281-0898-00			CAP,FXD,CER DI:7.5PF,+/-0.5PF,500V	96733	XR3446
A10C2236	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2237	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2238	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2239	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2240	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2241	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2242	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2245	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2246	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2247	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C2248	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C3101	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C3102	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C3104	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C3105	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C3112	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C3232	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C3236	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C3306	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C3307	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C3308	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C4101	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C4106	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C4110	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C4115	281-0763-00			CAP,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A10C4118	281-0861-00	B021130		CAP,FXD,CER DI:270PF,5%,50V	54583	MA12C0G1H271J
A10C4125	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C4126	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A10C4201	283-0789-00			CAP,FXD,MICA DI:600PF,1%,500V	00853	D153F601F0
A10C4202	281-0158-00			CAP,VAR,CER DI:7-45PF,25V	59660	518-006 G 7-45
A10C4203	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V (SELECTED. MAY NOT BE REQUIRED)	04222	MA101A220KAA
A10C4217	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C4232	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9001	290-0297-00	B010100	B012599	CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A10C9002	290-0297-00	B010100	B012599	CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A10C9002	290-0847-00	B012600		CAP,FXD,ELCTLT:47UF,+50-10%,10V	55680	TLB1A470MAA
A10C9003	290-0297-00	B010100	B012599	CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A10C9004	290-0297-00	B010100	B012599	CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A10C9005	290-0297-00	B010100	B012599	CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A10C9006	290-0297-00	B010100	B012599	CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A10C9006	290-0847-00	B012600		CAP,FXD,ELCTLT:47UF,+50-10%,10V	55680	TLB1A470MAA
A10C9007	290-0297-00	B010100	B012599	CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A10C9007	290-0847-00	B012600		CAP,FXD,ELCTLT:47UF,+50-10%,10V	55680	TLB1A470MAA
A10C9011	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9012	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9013	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9014	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9015	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9021	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9022	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9023	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9024	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9025	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9031	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9032	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10C9033	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9034	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9035	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9041	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9042	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9043	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9044	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9045	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9071	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9072	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9073	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9074	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9075	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9091	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9092	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9093	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9094	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9095	281-0775-01	B021985		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9101	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9102	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9104	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9107	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A10C9109	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9201	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9202	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9203	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9205	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9206	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9207	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9210	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A10C9211	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9212	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9220	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A10C9221	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9222	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9223	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9250	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9301	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9302	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A10C9410	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C102MAA
A10C9411	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C102MAA
A10CR2101	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2102	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2103	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2104	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2105	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2106	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2107	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2108	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2109	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A10CR2111	152-0269-00			SEMICOND DVC,DI:VVC,SI,35V,33PF,DO-7	04713	SMV1263
A10CR2112	152-0269-00			SEMICOND DVC,DI:VVC,SI,35V,33PF,DO-7	04713	SMV1263
A10CR2203	152-0585-00			SEMICOND DVC,DI:SCHOTTKY BARRIER,SI,5V,10UA	96341	4E722
A10J2111	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ (QUANTITY OF 4)	22526	47359-000
A10J2112	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ (QUANTITY OF 4)	22526	47359-000
A10J4104	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10J6100	131-0608-00	B010100	B011352	(QUANTITY OF 3)		
A10J6100	131-0091-00	B011353		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10J8100	131-0608-00	B010100	B011352	CONN,RCPT,ELEC:HEADER,2 X 17,0.1 SPACING	22526	65610-134
A10J8100	131-2401-00	B011353		TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10J9104	131-0608-00			CONN,RCPT,ELEC:2 X 25,MALE	TK1483	082-2543-SD10
				TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10J9105	131-0608-00			(QUANTITY OF 3)		
				TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
				(QUANTITY OF 12)		
A10J9107	131-0608-00					
				TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A10L2137	108-0245-00			(QUANTITY OF 3)		
A10L2139	108-0245-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A10P4104	131-0993-00			CHOKE,RF:FIXED,3.9UH	76493	B6310-1
A10P9104	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A10P9105	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
				BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A10P9107	131-0993-00					
A10Q2101	151-0712-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A10Q2102	151-0712-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A10Q2103	151-0271-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8223
A10Q2104	151-0711-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8236
A10Q2105	151-0472-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
				TRANSISTOR:NPN,SI,TO-92	51984	NE41632B
A10Q2106	151-0369-00					
A10Q2107	151-0369-00			TRANSISTOR:PNP,SI,X-55	04713	SPS8273
A10Q2150	151-0190-00			TRANSISTOR:PNP,SI,X-55	04713	SPS8273
A10Q2207	151-0711-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q2208	151-0711-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A10Q2209	151-1042-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
				SEMICOND DVC SE:FET,SI,TO-92	04713	SPF627M2
A10Q2211	151-0711-00					
A10Q2212	151-0472-00			TRANSISTOR:NPN,SI,TO-92B	80009	151-0711-00
A10Q2213	151-0188-00			TRANSISTOR:NPN,SI,TO-92	51984	NE41632B
A10Q4203	151-0220-03			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A10Q4204	151-0220-03			TRANSISTOR:PNP,SI,TO-92	04713	SPS6915
A10Q4205	151-0190-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6915
				TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10Q4207	151-1121-00					
A10Q4227	151-0190-00			TRANSISTOR:FE,N CHANNEL,SI,TO-92	17856	V10206
A10Q9100	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10R2101	321-0165-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A10R2102	321-0165-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
A10R2104	315-0151-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
				RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R2105	315-0510-00					
A10R2106	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R2107	321-0068-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R2108	311-2226-00			RES,FXD,FILM:49.9 OHM,0.5%,0.125W,TC=T0	91637	CMF55116G49R90F
A10R2109	321-0109-00			RES,VAR,NONWW:TRMR,50 OHM,20%,0.5W	TK1450	GF06UT 50 OHM
A10R2110	321-0109-00			RES,FXD,FILM:133 OHM,1%,0.125W,TC=T0	07716	CEAD133R0F
				RES,FXD,FILM:133 OHM,1%,0.125W,TC=T0	07716	CEAD133R0F
A10R2111	321-0165-00					
A10R2112	321-0165-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
A10R2114	315-0151-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
A10R2115	315-0510-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A10R2116	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R2117	321-0068-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
				RES,FXD,FILM:49.9 OHM,0.5%,0.125W,TC=T0	91637	CMF55116G49R90F
A10R2118	311-2226-00					
A10R2119	315-0242-00			RES,VAR,NONWW:TRMR,50 OHM,20%,0.5W	TK1450	GF06UT 50 OHM
A10R2120	321-0069-00			RES,FXD,FILM:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A10R2121	321-0069-00			RES,FXD,FILM:51.1 OHM,1%,0.125W,TC=T0	91637	CMF55116G51R10F
A10R2122	321-0139-00			RES,FXD,FILM:51.1 OHM,1%,0.125W,TC=T0	91637	CMF55116G51R10F
A10R2123	321-0069-00			RES,FXD,FILM:274 OHM,1%,0.125W,TC=T0	07716	CEAD274R0F
				RES,FXD,FILM:51.1 OHM,1%,0.125W,TC=T0	91637	CMF55116G51R10F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R2124	321-0069-00			RES,FXD,FILM:51.1 OHM,1%,0.125W,TC=T0	91637	CMF55116G51R10F
A10R2125	321-0139-00			RES,FXD,FILM:274 OHM,1%,0.125W,TC=T0	07716	CEAD274R0F
A10R2126	321-0207-00			RES,FXD,FILM:1.40K OHM,1%,0.125W,TC=T0	19701	5033ED1K400F
A10R2127	321-0255-00			RES,FXD,FILM:4.42K OHM,1%,0.125W,TC=T0	19701	5033ED4K420F
A10R2128	321-0162-00			RES,FXD,FILM:475 OHM,1%,0.125W,TC=T0	19701	5033ED475R0F
A10R2129	321-0165-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
A10R2130	315-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A10R2131	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R2133	321-0165-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
A10R2137	321-0102-00			RES,FXD,FILM:113 OHM,1%,0.125W,TC=T0	07716	CEAD113R0F
A10R2138	311-2223-00			RES,VAR,NONWW:TRMR,10 OHM,20%,0.5W LINEAR	80009	311-2223-00
A10R2139	321-0098-00			RES,FXD,FILM:102 OHM,1%,0.125W,TC=T0	07716	CEAD102R0F
A10R2140	321-0165-00			RES,FXD,FILM:511 OHM,1%,0.125W,TC=T0	07716	CEAD511R0F
A10R2141	321-0179-00			RES,FXD,FILM:715 OHM,1%,0.125W,TC=T0	07716	CEAD715R0F
A10R2143	321-0200-00			RES,FXD,FILM:1.18K OHM,1%,0.125W,TC=T0	19701	5033ED11K80F
A10R2144	321-0151-00			RES,FXD,FILM:365 OHM,1%,0.125W,TC=T0	07716	CEAD365R0F
A10R2145	315-0270-00			RES,FXD,FILM:27 OHM,5%,0.25W	19701	5043CX27R00J
A10R2146	321-0149-00			RES,FXD,FILM:348 OHM,1%,0.125W,TC=T0	07716	CEAD348R0F
A10R2147	321-0149-00			RES,FXD,FILM:348 OHM,1%,0.125W,TC=T0	07716	CEAD348R0F
A10R2148	315-0561-00			RES,FXD,FILM:560 OHM,5%,0.25W	19701	5043CX560R0J
A10R2149	315-0391-00	B010100	B012599	RES,FXD,FILM:390 OHM,5%,0.25W	57668	NTR25J-E390E
A10R2149	315-0221-00	B010200	B012599	RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A10R2149	311-2230-00	B012600		RES,VAR,NONWW:TRMR,500 OHM,20%,0.50 LINEAR	TK1450	GF06UT 500
A10R2150	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25W	57668	NTR25J-E220E
A10R2151	301-0271-00			RES,FXD,FILM:270 OHM,5%,0.5W	19701	5053CX270R0J
A10R2152	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R2153	321-0214-00			RES,FXD,FILM:1.65K OHM,1%,0.125W,TC=T0	19701	5033ED1K65F
A10R2154	321-0657-00			RES,FXD,FILM:60 OHM,1%,0.125W,TC=T0	57668	CRB14 FXE 60 OHM
A10R2155	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A10R2156	321-0641-00			RES,FXD,FILM:1.8K OHM,1%,0.125W,TC=T0	91637	MFF1816G18000F
A10R2157	321-0197-00			RES,FXD,FILM:1.10K OHM,1%,0.125W,TC=T0	07716	CEAD11000F
A10R2257	321-0197-00			RES,FXD,FILM:1.10K OHM,1%,0.125W,TC=T0	07716	CEAD11000F
A10R2258	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A10R2259	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125W,TC=T0	24546	NA55D5001F
A10R2260	321-0641-00			RES,FXD,FILM:1.8K OHM,1%,0.125W,TC=T0	91637	MFF1816G18000F
A10R2265	321-0177-00			RES,FXD,FILM:681 OHM,1%,0.125W,TC=T0	07716	CEAD681R0F
A10R2266	321-0183-00			RES,FXD,FILM:787 OHM,1%,0.125W,TC=T0	07716	CEAD787R0F
A10R2267	321-0188-00			RES,FXD,FILM:887 OHM,1%,0.125W,TC=T0	07716	CEAD887R0F
A10R2268	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R2269	307-0526-00			RES NTWK,FXD,FI:5,510 OHM,10%,0.125 W	11236	750-61-R510 OHM
A10R2270	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A10R2274	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A10R2275	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R2276	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R2277	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R2278	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R2279	315-0220-00			RES,FXD,FILM:22 OHM,5%,0.25W	19701	5043CX22R00J
A10R2281	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A10R2285	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R2287	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R2289	315-0621-00			RES,FXD,FILM:620 OHM,5%,0.25W	57668	NTR25J-E620E
A10R2290	315-0431-00			RES,FXD,FILM:430 OHM,5%,0.25W	19701	5043CX430R0J
A10R2291	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R2292	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R2293	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R2295	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A10R2296	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J
A10R2297	315-0510-00			RES,FXD,FILM:51 OHM,5%,0.25W	19701	5043CX51R00J

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R3102	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R3104	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R3105	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R3232	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R3234	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R3301	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R3307	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R3310	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R3417	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R3423	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R4101	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4102	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4103	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4104	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4105	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4106	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4107	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4108	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4110	315-0470-00	B010100	B021129	RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R4110	315-0271-00	B021130		RES,FXD,FILM:270 OHM,5%,0.25W	57668	NTR25J-E270E
A10R4115	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R4119	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A10R4201	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4202	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R4203	315-0470-00	B010100	B010199	RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A10R4203	315-0100-00	B010200		RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A10R4204	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R4205	321-0145-00			RES,FXD,FILM:316 OHM,1%,0.125W,TC=T0	07716	CEAD316R0F
A10R4206	321-0183-00			RES,FXD,FILM:787 OHM,1%,0.125W,TC=T0	07716	CEAD787R0F
A10R4207	321-0612-00			RES,FXD,FILM:500 OHM,1%,0.125W,TC=T0	07716	CEAD500R0F
A10R4208	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R4209	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R4210	321-0161-00			RES,FXD,FILM:464 OHM,1%,0.125W,TC=T0	07716	CEAD464R0F
A10R4211	321-0204-00			RES,FXD,FILM:1.30K OHM,1%,0.125W,TC=T0	19701	5033ED1K300F
A10R4212	321-0406-00			RES,FXD,FILM:165K OHM,1%,0.125W,TC=T0	07716	CEAD16502F
A10R4213	311-2229-00			RES,VAR,NONWW:TRMR,250 OHM,20%,0.5W LINEAR	TK1450	GF06UT 250
A10R4214	321-0276-00			RES,FXD,FILM:7.32K OHM,1%,0.125W,TC=T0	19701	5043ED7K320F
A10R4215	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125W,TC=T0	19701	5033ED1K00F
A10R4216	321-0318-00			RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A10R4217	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A10R4220	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R4227	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A10R9101	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A10R9102	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9103	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9104	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9105	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9106	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9107	315-0274-00			RES,FXD,FILM:270K OHM,5%,0.25W	57668	NTR25J-E270K
A10R9108	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A10R9109	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A10R9110	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9112	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9113	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A10R9114	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9115	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R9120	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A10R9210	321-0251-00			RES,FXD,FILM:4.02K OHM,1%,0.125W,TC=T0	19701	5033ED4K020F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R9211	321-0256-00			RES,FXD,FILM:4.53K OHM,1%,0.125W,TC=T9	19701	5033ED4K530F
A10R9212	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A10R9213	321-0299-00	B010100	B011086	RES,FXD,FILM:12.7K OHM,1%,0.125W,TC=T0	19701	5033ED12K70F
A10R9213	321-0289-00	B011087		RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R9214	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A10R9219	307-0540-00			RES NTWK,FXD,FI:(5)1K OHM,10%,0.7W	11236	750-61-R1KOHM
A10R9220	321-0197-00			RES,FXD,FILM:1.10K OHM,1%,0.125W,TC=T0	07716	CEAD11000F
A10R9221	321-0256-00			RES,FXD,FILM:4.53K OHM,1%,0.125W,TC=T9	19701	5033ED4K530F
A10R9222	311-2236-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W LINEAR	TK1450	GF06UT 20K
A10R9223	321-0299-00	B010100	B010549	RES,FXD,FILM:12.7K OHM,1%,0.125W,TC=T0	19701	5033ED12K70F
A10R9223	321-0289-00	B010550		RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A10R9224	311-2234-00			RES,VAR,NONWW:TRMR,5K OHM,20%,0.5W LINEAR	TK1450	GF06UT 5K
A10R9230	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A10R9301	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A10R9302	307-0446-00			RES NTWK,FXD,FI:10K OHM,20%,(9)RES	11236	750-101-R10K
A10R9401	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A10R9402	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A10R9412	311-2285-00	B010100	B012599	RES,VAR,NONWW:CKT BD,10K OHM,20%,0.25W	12697	CM43480
A10RT2101	307-0124-00			RES,THERMAL:5K OHM,10%,NTC	15454	1DC502K-220-EC
A10RT2102	307-0751-00			RES,THERMAL:20K OHM,5%	56866	QTMC-19J
A10RT2103	307-0124-00			RES,THERMAL:5K OHM,10%,NTC	15454	1DC502K-220-EC
A10RT2111	307-0124-00			RES,THERMAL:5K OHM,10%,NTC	15454	1DC502K-220-EC
A10RT2112	307-0751-00			RES,THERMAL:20K OHM,5%	56866	QTMC-19J
A10RT2113	307-0124-00			RES,THERMAL:5K OHM,10%,NTC	15454	1DC502K-220-EC
A10RT2131	307-0751-00			RES,THERMAL:20K OHM,5%	56866	QTMC-19J
A10RT2132	307-0124-00	B012600		RES,THERMAL:5K OHM,10%,NTC	15454	1DC502K-220-EC
A10S9401	260-2254-00			SWITCH,PUSH:5 BUTTON,2 POLE,MEMORY	80009	260-2254-00
A10S9402	260-2253-00			SWITCH,PUSH:5 BUTTON,2 POLE,STORAGE	80009	260-2253-00
A10S9403	260-1132-02			SWITCH,PUSH:DPDT,1A,28VDC,1 BUTTON	59821	2KAB010000543
A10S9412	----- -----	B010100	B012599	(PART OF R9412)		
A10T2201	120-1681-00			TRANSFORMER,RF:7 TURNS,BIFILAR,COMMON MODE	TK1345	ORDER BY DESCR
A10T2202	120-1680-00			TRANSFORMER,RF:5 TURN,BIBILAR	80009	120-1680-00
A10T2203	120-0444-00			XFMR,TOROID:	80009	120-0444-00
A10U1343	160-2998-05	B010100	B020989	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-05
A10U1343	160-2998-06	B020990		MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-06
A10U2101	155-0022-00			MICROCKT,DGTL:CHANNEL SWITCH	80009	155-0022-00
A10U2202	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A10U2203	156-1642-00			MICROCKT,DGTL:TPL 2-3-2 INP OR/NOR GATE	04713	MC10H105(L OR P)
A10U2204	156-2248-00			MICROCKT,DGTL:ECL,8 BIT A/D HIGH SPEED	80009	156-2248-00
A10U2205	156-0316-00			MICROCKT,DGTL:ECL,QUAD 2-INP ECL TO TTL	04713	MC10125L
A10U2206	156-0316-00			MICROCKT,DGTL:ECL,QUAD 2-INP ECL TO TTL	04713	MC10125L
A10U3101	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U3102	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U3103	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U3104	156-2091-00			MICROCKT,DGTL:QUAD 2-INP POS NAND GATES	01295	SN74ALS00AN3
A10U3105	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U3106	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U3112	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE	04713	MC7400(NDORJD)
A10U3229	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
A10U3230	156-2326-00			MICROCKT,DGTL:4 BIT COUNTERS W/3 STATE OUT	01295	SN74ALS561AN3J4
A10U3231	156-2326-00			MICROCKT,DGTL:4 BIT COUNTERS W/3 STATE OUT	01295	SN74ALS561AN3J4
A10U3232	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
A10U3233	156-2336-00			MICROCKT,DGTL:LSTTL,8 BIT MAGTD COMPARATOR	01295	SN74LS684N3
A10U3234	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
A10U3235	156-2336-00			MICROCKT,DGTL:LSTTL,8 BIT MAGTD COMPARATOR	01295	SN74LS684N3
A10U3236	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
A10U3237	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
A10U3238	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10U3239	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
A10U3306	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U3307	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U3308	156-1743-00			MICROCKT,DGTL:ASTTL,QUAD 2-INPUT NOR GATE	18324	74F02 NB OR FB
A10U3309	156-1662-00			MICROCKT,DGTL:	04713	MC74F153 ND/JD
A10U3310	156-2357-00			MICROCKT,DGTL:CMOS,OCTAL LATCH,NONINVERTING	01295	SN74HCT574N3
A10U3313	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE	04713	MC7400(NDORJD)
A10U3416	156-2094-00			MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS04BN3/J4
A10U3417	156-1997-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F158 ND/JD
A10U3418	156-1993-00			MICROCKT,DGTL:2048 X 8 SRAM W/3-STATE OUT	04713	MCM2016HN-70
A10U3419	156-1993-00			MICROCKT,DGTL:2048 X 8 SRAM W/3-STATE OUT	04713	MCM2016HN-70
A10U3420	156-2093-00			MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3
A10U3421	156-1921-00			MICROCKT,DGTL:OCTAL BUS XSCVR E/3-ST OUT	27014	MM74HCT245N
A10U3422	156-1921-00			MICROCKT,DGTL:OCTAL BUS XSCVR E/3-ST OUT	27014	MM74HCT245N
A10U3423	156-2334-00			MICROCKT,DGTL:SYNC,4 BUT UP/DOWN CNTR	01295	SN74ALS191N3
A10U3424	156-2334-00			MICROCKT,DGTL:SYNC,4 BUT UP/DOWN CNTR	01295	SN74ALS191N3
A10U3425	156-2334-00			MICROCKT,DGTL:SYNC,4 BUT UP/DOWN CNTR	01295	SN74ALS191N3
A10U3426	156-2091-00			MICROCKT,DGTL:QUAD 2-INP POS NAND GATES	01295	SN74ALS00AN3
A10U3427	156-2369-00			MICROCKT,DGTL:OCT BFR/LINE DRVR W/3 ST OUT	04713	MC74HCT541N
A10U3428	156-2369-00			MICROCKT,DGTL:OCT BFR/LINE DRVR W/3 ST OUT	04713	MC74HCT541N
A10U4101	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE	04713	MC74F08 ND OR JD
A10U4102	156-1919-00			MICROCKT,DGTL:DUAL POS EDGE TRIG FLIP-FLOP	04713	MC74F109 ND/JD
A10U4103	156-1662-00			MICROCKT,DGTL:	04713	MC74F153 ND/JD
A10U4104	156-1919-00			MICROCKT,DGTL:DUAL POS EDGE TRIG FLIP-FLOP	04713	MC74F109 ND/JD
A10U4105	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U4106	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE	04713	MC7400(NDORJD)
A10U4107	156-2333-00			MICROCKT,DGTL:ALSTTL,SYNC,4 BIT DECADE CNTR	01295	SN74ALS162BN3
A10U4108	156-2333-00			MICROCKT,DGTL:ALSTTL,SYNC,4 BIT DECADE CNTR	01295	SN74ALS162BN3
A10U4109	156-2333-00			MICROCKT,DGTL:ALSTTL,SYNC,4 BIT DECADE CNTR	01295	SN74ALS162BN3
A10U4110	156-2333-00			MICROCKT,DGTL:ALSTTL,SYNC,4 BIT DECADE CNTR	01295	SN74ALS162BN3
A10U4111	156-2333-00			MICROCKT,DGTL:ALSTTL,SYNC,4 BIT DECADE CNTR	01295	SN74ALS162BN3
A10U4112	156-2333-00			MICROCKT,DGTL:ALSTTL,SYNC,4 BIT DECADE CNTR	01295	SN74ALS162BN3
A10U4113	156-2357-00			MICROCKT,DGTL:CMOS,OCTAL LATCH,NONINVERTING	01295	SN74HCT574N3
A10U4114	156-2093-00			MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3
A10U4115	156-2326-00			MICROCKT,DGTL:4 BIT COUNTERS W/3 STATE OUT	01295	SN74ALS561AN3J4
A10U4116	156-2326-00			MICROCKT,DGTL:4 BIT COUNTERS W/3 STATE OUT	01295	SN74ALS561AN3J4
A10U4117	156-2326-00			MICROCKT,DGTL:4 BIT COUNTERS W/3 STATE OUT	01295	SN74ALS561AN3J4
A10U4118	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U4119	156-2357-00			MICROCKT,DGTL:CMOS,OCTAL LATCH,NONINVERTING	01295	SN74HCT574N3
A10U4120	156-2332-00			MICROCKT,DGTL:QUAD 2 IN POS NAND GATE	01295	SN74ALS01N3
A10U4121	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U4122	156-2093-00			MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3
A10U4123	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
A10U4124	156-1664-00			MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
A10U4125	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U4126	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U4127	156-1743-00			MICROCKT,DGTL:ASTTL,QUAD 2-INPUT NOR GATE	18324	74F02 NB OR FB
A10U4226	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U4227	156-1662-00			MICROCKT,DGTL:	04713	MC74F153 ND/JD
A10U4228	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U4229	156-1126-00			MICROCKT,LINEAR:VOLTAGE COMPARATOR	01295	LM311P
A10U4230	156-2331-00			MICROCKT,DGTL:8 BIT CNTR W/RGSTR,3 ST OUT	01295	SN74LS590N3
A10U4231	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U4232	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGGERED FF	80009	156-1611-00
A10U9101	156-2113-00			MICROCKT,DI:QUAD 2-INPUT POSITIVE-AND GATE	01295	SN74ALS08N3
A10U9102	156-2093-00			MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3
A10U9103	156-1753-00			MICROCKT,DGTL:OCT BFR/LINE DRVR W/2-ST OUT	01295	74ALS240NP3
A10U9104	156-2344-00			MICROCKT,DGTL:CMOS,CLOCK GEN & DRIVER	34371	IP82C84A/+

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10U9105	156-2293-00			MICROCKT,DGTL:DUAL 2 TO 4-LINE DECODER/MUX	01295	SN74ALS139N3
A10U9106	156-2293-00			MICROCKT,DGTL:DUAL 2 TO 4-LINE DECODER/MUX	01295	SN74ALS139N3
A10U9107	156-2093-00			MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3
A10U9108	156-2355-00			MICROCKT,DGTL:14 STAGE BINARY RIPPLE CNTR	02735	CD74HCT4020EX
A10U9109	160-3633-01	B010100	B010753	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3633-01
A10U9109	160-3633-02	B010754	B011017	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3633-02
A10U9109	160-3633-03	B011018	B020678	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3633-03
A10U9109	160-3633-05	B020679	B020989	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3633-05
A10U9109	160-3633-06	B020990	B021935	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3633-06
A10U9109	160-3633-07	B021936	B022326	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3633-07
A10U9109	160-3633-08	B022327	B023053	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3633-08
A10U9109	160-3633-09	B023054		MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3633-09
A10U9110	160-3532-01	B010100	B010753	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3532-01
A10U9110	160-3532-02	B010754	B011017	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3532-02
A10U9110	160-3532-03	B011018	B020678	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3532-03
A10U9110	160-3532-05	B020679	B020989	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3532-05
A10U9110	160-3532-06	B020990	B021935	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3532-06
A10U9110	160-3532-07	B021936	B022326	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3532-07
A10U9110	160-3532-08	B022327	B023053	MICROCKT,DGTL:64K X 8 EPROM,PRGM	80009	160-3532-08
A10U9110	160-3532-09	B023054		MICROCKT,DGTL:64K X 8 EPROM,PRGM (U9109/U9110 MUST BE REPLACED AS A PAIR)	80009	160-3532-09
A10U9111	156-1609-01			MICROCKT,DGTL:HMOS,8 BIT MICROPROCESSOR	34649	D8088-2PC
A10U9112	156-1858-00			MICROCKT,DGTL:TRANSPARENT D-TYPE LATCHES	01295	SN74LS573(NP3)
A10U9113	156-1748-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3-STATE OUT	01295	SN74ALS245AN3
A10U9114	156-1858-00			MICROCKT,DGTL:TRANSPARENT D-TYPE LATCHES	01295	SN74LS573(NP3)
A10U9201	156-1859-00			MICROCKT,DGTL:MOS,DYNAMIC RAM,SCRN	01295	TMS4416-15
A10U9202	156-1859-00			MICROCKT,DGTL:MOS,DYNAMIC RAM,SCRN	01295	TMS4416-15
A10U9203	156-1859-00			MICROCKT,DGTL:MOS,DYNAMIC RAM,SCRN	01295	TMS4416-15
A10U9204	156-2210-00			MICROCKT,DGTL:QUAD SEL/MUX W/3-STATE OUT	01295	SN74ALS257N3
A10U9205	156-2210-00			MICROCKT,DGTL:QUAD SEL/MUX W/3-STATE OUT	01295	SN74ALS257N3
A10U9206	156-1921-00			MICROCKT,DGTL:OCTAL BUS XSCVR E/3-ST OUT	27014	MM74HCT245N
A10U9207	156-1921-00			MICROCKT,DGTL:OCTAL BUS XSCVR E/3-ST OUT	27014	MM74HCT245N
A10U9208	156-2452-00			MICROCKT,DGTL:SEMI-CUSTOM,STD CELL	TK1856	VF4172
A10U9210	156-1638-00			MICROCKT,LINEAR:10 BIT HS,MULT,D/A CONV	06665	DAC-10GX
A10U9211	160-3586-00			MICROCKT,DGTL:GATE ARRAY,PRGM	80009	160-3586-00
A10U9220	156-1638-00			MICROCKT,LINEAR:10 BIT HS,MULT,D/A CONV	06665	DAC-10GX
A10U9231	156-1859-00			MICROCKT,DGTL:MOS,DYNAMIC RAM,SCRN	01295	TMS4416-15
A10U9232	156-1859-00			MICROCKT,DGTL:MOS,DYNAMIC RAM,SCRN	01295	TMS4416-15
A10U9233	156-1859-00			MICROCKT,DGTL:MOS,DYNAMIC RAM,SCRN	01295	TMS4416-15
A10U9301	156-2369-00			MICROCKT,DGTL:OCT BFR/LINE DRVR W/3 ST OUT	04713	MC74HCT541N
A10U9302	156-2369-00			MICROCKT,DGTL:OCT BFR/LINE DRVR W/3 ST OUT	04713	MC74HCT541N
A10W2101	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W2102	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W2103	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W2104	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W2105	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W2107	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W2203	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W3234	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W4100	179-2950-00			WIRING HARNESS:STORAGE	80009	179-2950-00
A10W4200	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W4201	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9012	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9013	131-0566-00	B010100	B021984	BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9014	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9015	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9016	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9017	131-3299-00	B010100	B021984	BUS,CONDUCTOR:CKT BD,POWER DIST NETWORK	TK1884	1TEKQP03Z
A10W9018	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10W9019	131-3299-00	B010100	B021984	BUS,CONDUCTOR:CKT BD,POWER DIST NETWORK	TK1884	1TEKQP03Z
A10W9021	131-3299-00	B010100	B021984	BUS,CONDUCTOR:CKT BD,POWER DIST NETWORK	TK1884	1TEKQP03Z
A10W9022	131-3299-00	B010100	B021984	BUS,CONDUCTOR:CKT BD,POWER DIST NETWORK	TK1884	1TEKQP03Z
A10W9023	131-3299-00	B010100	B021984	BUS,CONDUCTOR:CKT BD,POWER DIST NETWORK	TK1884	1TEKQP03Z
A10W9024	131-3299-00	B010100	B021984	BUS,CONDUCTOR:CKT BD,POWER DIST NETWORK	TK1884	1TEKQP03Z
A10W9025	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9026	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9027	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9028	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9029	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10W9208	136-0848-00			SKT,PL-IN ELEK:68 PIN 5162-2	00779	55162-2
A10W9211	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A10Y4100	119-1460-00			OSCILLATOR,RF:40.0MHZ	01537	K1114AM 40 MHz
A11	672-1194-00	B010100	B022101	CIRCUIT BD ASSY:INPUT/OUTPUT & VECTOR GEN	80009	672-1194-00
A11	672-1194-01	B022102		CIRCUIT BD ASSY:INPUT/OUTPUT & VECTOR GEN	80009	672-1194-01
A11A1	----- -----			CKT BOARD ASSY:INPUT/OUTPUT (NOT AVAILABLE, USE A11)		
A11A1C6101	281-0861-00			CAP,FXD,CER DI:270PF,5%,50V	54583	MA12C0G1H271J
A11A1C6102	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6103	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6104	281-0775-01	B010100	B011043	CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6105	281-0775-01	B010100	B011043	CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6106	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6107	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6108	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6109	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6110	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6111	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6112	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6113	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6114	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6115	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6116	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6117	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6118	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6130	281-0862-00			CAP,FXD,CER DI:0.001UF,+80-20%,100V	04222	MA101C102MAA
A11A1C6201	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A11A1C6202	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6203	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6204	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6205	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6206	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6207	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6208	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A1C6210	290-0920-00			CAP,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TAAANA
A11A1C6211	290-0920-00			CAP,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TAAANA
A11A1C6212	290-0920-00			CAP,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TAAANA
A11A1C6220	281-0861-00			CAP,FXD,CER DI:270PF,5%,50V	54583	MA12C0G1H271J
A11A1C6221	281-0861-00			CAP,FXD,CER DI:270PF,5%,50V	54583	MA12C0G1H271J
A11A1CR6101	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A1CR6102	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A1CR6103	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A1CR6104	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A1CR6201	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A1CR6202	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A11A1CR6203	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A1CR6204	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A1J6110	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 8)	22526	48283-029
A11A1J6120	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 9)	22526	48283-029
A11A1J6130	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 8)	22526	48283-029
A11A1J6140	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A11A1J6150	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A11A1L6201	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A11A1L6202	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A11A1L6203	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A11A1L6204	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A11A1L6205	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A11A1L6206	120-0382-00			COIL,RF:210UH,+28%-43%,14 TURNS	80009	120-0382-00
A11A1Q6101	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A11A1Q6201	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A11A1Q6202	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A11A1Q6203	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A11A1R6101	307-0595-00			RES NTWK,FXD,FI:7,5.6K OHM,2%,1.0W	11236	750-81-5.6K
A11A1R6102	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11A1R6103	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6104	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6105	321-0405-00			RES,FXD,FILM:162K OHM,1%,0.125W,TC=T0	07716	CEAD16202F
A11A1R6106	321-0405-00			RES,FXD,FILM:162K OHM,1%,0.125W,TC=T0	07716	CEAD16202F
A11A1R6107	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6108	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6109	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6110	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6111	321-0414-00			RES,FXD,FILM:200K OHM,1%,0.125W,TC=T0	07716	CEAD20002F
A11A1R6112	321-0414-00			RES,FXD,FILM:200K OHM,1%,0.125W,TC=T0	07716	CEAD20002F
A11A1R6113	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6114	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6115	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6116	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6117	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6118	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A1R6119	311-2267-00			RES,VAR,NONWW:TRMR,50K OHM,20%,0.5W	TK1450	GF06VT B50K-OHM
A11A1R6120	321-0354-00			RES,FXD,FILM:47.5K OHM,1%,0.125W,TC=T0	19701	5043ED47K50F
A11A1R6121	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A1R6122	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A1R6123	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A1R6124	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A1R6125	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A1R6126	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A1R6127	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A1R6128	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6129	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6130	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6131	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6132	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6133	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6134	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6135	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6136	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6137	315-0164-00			RES,FXD,FILM:160K OHM,5%,0.25W	57668	NTR25J-E160K
A11A1R6138	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A11A1R6201	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6202	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6203	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6204	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6205	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6206	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6207	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6208	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6209	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6210	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6211	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6212	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6213	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6214	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6215	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6216	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6217	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A11A1R6218	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6219	315-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.25W	57668	NTR25J-E02K4
A11A1R6220	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A11A1R6221	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A11A1R6222	315-0184-00			RES,FXD,FILM:180K OHM,5%,0.25W	19701	5043CX180K0J
A11A1R6223	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A11A1R6224	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A11A1R6225	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A11A1R6226	321-0281-00			RES,FXD,FILM:8.25K OHM,1%,0.125W,TC=T0	19701	5043ED8K250F
A11A1R6227	321-0302-00			RES,FXD,FILM:13.7K OHM,1%,0.125W,TC=T0	07716	CEAD 13701F
A11A1R6228	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A11A1R6229	315-0164-00			RES,FXD,FILM:160K OHM,5%,0.25W	57668	NTR25J-E160K
A11A1R6230	315-0564-00			RES,FXD,FILM:560K OHM,5%,0.25W	19701	5043CX560K0J
A11A1R6231	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A11A1R6232	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A1R6233	321-0302-00			RES,FXD,FILM:13.7K OHM,1%,0.125W,TC=T0	07716	CEAD 13701F
A11A1R6234	321-0281-00			RES,FXD,FILM:8.25K OHM,1%,0.125W,TC=T0	19701	5043ED8K250F
A11A1U5101	156-2026-00			MICROCKT,DGTL:CMOS,QUAD 2 INPUT NOR GATE	04713	MC74HC02(N OR J)
A11A1U6102	156-2369-00			MICROCKT,DGTL:OCT BFR/LINE DRVR W/3 ST OUT	04713	MC74HCT541N
A11A1U6103	156-2369-00			MICROCKT,DGTL:OCT BFR/LINE DRVR W/3 ST OUT	04713	MC74HCT541N
A11A1U6104	156-2357-00			MICROCKT,DGTL:CMOS,OCTAL LATCH,NONINVERTING	01295	SN74HCT574N3
A11A1U6105	156-2347-00			MICROCKT,LINEAR:A/D CONVERTER,217 US,10 BIT	27014	ADC1001CCJA+
A11A1U6106	156-0513-02	B010100	B022299	MICROCKT,DGTL:CMOS,ANALOG MUX/DEMUX	02735	CD4051BFX
A11A1U6106	156-0513-00	B022300		MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A11A1U6107	156-0495-00			MICROCKT,LINEAR:OPNL AMPL	01295	LM324N
A11A1U6108	156-0513-02	B010100	B022299	MICROCKT,DGTL:CMOS,ANALOG MUX/DEMUX	02735	CD4051BFX
A11A1U6108	156-0513-00	B022300		MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A11A1U6201	156-0991-00			MICROCKT,LINEAR:VOLTAGE REGULATOR	04713	MC78L05ACP
A11A1U6202	156-1225-00			MICROCKT,LINEAR:DUAL COMPARATOR	01295	LM393P
A11A1W6000	259-0017-00			FLEX CIRCUIT:IO & VG BOARD	80009	259-0017-00
A11A1W6100	175-9853-00			CA ASSY,SP,ELEC:34,28 AWG,5.125 L,RIBBON	80009	175-9853-00
A11A1W6119	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A11A1W6201	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A11A1W6202	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A11A2	----- -----			CKT BOARD ASSY:VECTOR GENERATOR (NOT AVAILABLE, USE A11)		
A11A2C6301	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6302	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6303	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A11A2C6304	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6305	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6306	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6307	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6308	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6309	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6310	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A11A2C6311	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A11A2C6312	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A11A2C6314	283-0594-00			CAP,FXD,MICA DI:0.001UF,1%,100V	00853	D151F102F0
A11A2C6315	283-0594-00			CAP,FXD,MICA DI:0.001UF,1%,100V	00853	D151F102F0
A11A2C6316	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A11A2C6317	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A11A2C6401	281-0861-00			CAP,FXD,CER DI:270PF,5%,50V	54583	MA12C0G1H271J
A11A2C6402	290-0920-00			CAP,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TAAANA
A11A2C6403	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6404	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6407	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A11A2C6408	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A11A2C6409	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6421	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6422	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6440	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6441	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2C6442	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11A2CR6301	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6302	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6303	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6304	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6305	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6306	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6307	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6308	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6401	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6403	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2CR6405	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A11A2J6410	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 10)	22526	48283-029
A11A2J6420	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 9)	22526	48283-029
A11A2Q6301	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A11A2R6301	315-0751-00			RES,FXD,FILM:750 OHM,5%,0.25W	57668	NTR25J-E750E
A11A2R6303	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A11A2R6304	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A11A2R6305	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A11A2R6306	321-0932-00			RES,FXD,FILM:2.5K OHM,1%,0.125W,TC=T0	24546	NA55D2501F
A11A2R6307	321-0202-00			RES,FXD,FILM:1.24K OHM,1%,0.125W,TC=T0	24546	NA55D1241F
A11A2R6308	321-0202-00			RES,FXD,FILM:1.24K OHM,1%,0.125W,TC=T0	24546	NA55D1241F
A11A2R6309	321-0816-07			RES,FXD,FILM:5K OHM,0.1%,0.125W,TC=T9	19701	5033RE5K000B
A11A2R6310	321-0816-07			RES,FXD,FILM:5K OHM,0.1%,0.125W,TC=T9	19701	5033RE5K000B
A11A2R6311	321-0926-07			RES,FXD,FILM:4K OHM,0.1%,0.125W,TC=T9	19701	5033RE4K00B
A11A2R6312	311-2227-00	B010100	B010486	RES,VAR,NONWW:TRMR,100 OHM,20%,0.5W LINEAR	TK1450	GF06UT 100
A11A2R6312	311-2229-00	B010487		RES,VAR,NONWW:TRMR,250 OHM,20%,0.5W LINEAR	TK1450	GF06UT 250
A11A2R6315	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11A2R6316	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A11A2R6317	321-0211-00			RES,FXD,FILM:1.54K OHM,1%,0.125W,TC=T0	07716	CEAD15400F
A11A2R6318	321-0207-00			RES,FXD,FILM:1.40K OHM,1%,0.125W,TC=T0	19701	5033ED1K400F
A11A2R6320	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A11A2R6321	311-2227-00			RES,VAR,NONWW:TRMR,100 OHM,20%,0.5W LINEAR	TK1450	GF06UT 100
A11A2R6322	321-0816-07			RES,FXD,FILM:5K OHM,0.1%,0.125W,TC=T9	19701	5033RE5K000B
A11A2R6323	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A11A2R6330	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25W	57668	NTR25J-E01K2
A11A2R6331	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A11A2R6401	321-0189-00			RES,FXD,FILM:909 OHM,1%,0.125W,TC=T2	19701	5033ED909ROF
A11A2R6402	321-0189-00			RES,FXD,FILM:909 OHM,1%,0.125W,TC=T2	19701	5033ED909ROF
A11A2R6403	321-0183-00			RES,FXD,FILM:787 OHM,1%,0.125W,TC=T0	07716	CEAD787ROF
A11A2R6404	321-0201-00			RES,FXD,FILM:1.21K OHM,1%,0.125W,TC=T0	19701	5043ED1K210F
A11A2R6405	321-0201-00			RES,FXD,FILM:1.21K OHM,1%,0.125W,TC=T0	19701	5043ED1K210F
A11A2R6406	321-0212-00			RES,FXD,FILM:1.58K OHM,1%,0.125W,TC=70	19701	5033ED1K58F
A11A2R6407	315-0472-00	B010339		RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A2R6410	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A11A2R6411	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A2R6412	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11A2R6413	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A2R6414	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A11A2R6415	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A11A2R6416	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A2R6417	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A11A2R6418	321-0269-00			RES,FXD,FILM:6.19K OHM,1%,0.125W,TC=T0	07716	CEAD61900F
A11A2R6419	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A11A2R6420	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A11A2R6421	315-0164-00			RES,FXD,FILM:160K OHM,5%,0.25W	57668	NTR25J-E160K
A11A2R6422	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A11A2R6423	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A11A2R6424	321-0344-00			RES,FXD,FILM:37.4K OHM,1%,0.125W,TC=T0	19701	5033ED 37K40F
A11A2R6425	321-0344-00			RES,FXD,FILM:37.4K OHM,1%,0.125W,TC=T0	19701	5033ED 37K40F
A11A2R6426	315-0363-00			RES,FXD,FILM:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A11A2R6427	315-0513-00			RES,FXD,FILM:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A11A2R6428	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A11A2R6429	321-0354-00	B010100	B022101	RES,FXD,FILM:47.5K OHM,1%,0.125W,TC=T0	19701	5043ED47K50F
A11A2R6429	321-0326-00	B022102		RES,FXD,FILM:24.3K OHM,1%,0.125W,TC=T0	19701	5043ED24K30F
A11A2R6430	311-2238-00	B022102		RES,VAR,NONWW:TRMR,50K OHM,20%,0.5W LINEAR	TK1450	GF06UT 50 K
A11A2R5432	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125W,TC=T0	19701	5033ED10K0F
A11A2R6433	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11A2R6434	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A11A2R6440	321-0243-00			RES,FXD,FILM:3.32K OHM,1%,0.125W,TC=T0	19701	5033ED3K32F
A11A2R6441	321-0243-00			RES,FXD,FILM:3.32K OHM,1%,0.125W,TC=T0	19701	5033ED3K32F
A11A2R6442	321-0221-00			RES,FXD,FILM:1.96K OHM,1%,0.125W,TC=T0	19701	5043ED1K960F
A11A2R6443	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A11A2R6444	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A11A2R6445	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A11A2U6301	156-0515-02	B010100	B022299	MICROCKT,DGTL:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A11A2U6301	156-0515-00	B022300		MICROCKT,DGTL:CMOS,TRIPLE 3-CHAN MUX	02735	CD4053BF
A11A2U6302	156-1437-00			MICROCKT,LINEAR:VOLTAGE REF	04713	MC1404AU5DS
A11A2U6303	156-1156-00			MICROCKT,LINEAR:OPERATIONAL AMPLIFIER	80009	156-1156-00
A11A2U6304	156-1156-00			MICROCKT,LINEAR:OPERATIONAL AMPLIFIER	80009	156-1156-00
A11A2U6305	156-2348-00			MICROCKT,LINEAR:HIGH PERF DIFF INPUT	80009	156-2348-00
A11A2U6306	156-2348-00			MICROCKT,LINEAR:HIGH PERF DIFF INPUT	80009	156-2348-00
A11A2U6307	156-1156-00			MICROCKT,LINEAR:OPERATIONAL AMPLIFIER	80009	156-1156-00
A11A2U6308	156-1156-00			MICROCKT,LINEAR:OPERATIONAL AMPLIFIER	80009	156-1156-00
A11A2U6401	156-0048-00			MICROCKT,LINEAR:5 XSTR ARRAY	02735	CA3046
A11A2U6402	156-0048-00			MICROCKT,LINEAR:5 XSTR ARRAY	02735	CA3046
A11A2U6403	156-1381-00			MICROCKT,LINEAR:3 NPN,2 PNP,XSTR ARRAY	02735	CA3096AE-17
A11A2U6404	156-0901-00			MICROCKT,LINEAR:OPNL XCONDUCTANCE AMPL	02735	CA3060E
A11A2U6405	156-0853-00			MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
A11A2W6310	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A11A2W6320	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A13	670-8705-00			CIRCUIT BD ASSY:SWEEP INTFC	80009	670-8705-00
A13C766	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A13C767	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A13C768	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A13C6313	290-0920-00	B010339		CAP,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TAAANA
A13J1304	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 22)	22526	48283-029
A13J6421	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 5)	22526	48283-036
A13R723	321-0273-00			RES,FXD,FILM:6.81K OHM,1%,0.125W,TC=T0	07716	CEAD68100F
A13R725	321-0258-00			RES,FXD,FILM:4.75K OHM,1%,0.125W,TC=T0	19701	5033ED4K750F
A13R729	321-0273-00			RES,FXD,FILM:6.81K OHM,1%,0.125W,TC=T0	07716	CEAD68100F
A13R734	307-0730-00			RES NTWK,FXD,FI:7,47K OHM,2%,0.18W EA	11236	750-81-R47K
A13R735	307-0730-00			RES NTWK,FXD,FI:7,47K OHM,2%,0.18W EA	11236	750-81-R47K
A13R736	307-0730-00			RES NTWK,FXD,FI:7,47K OHM,2%,0.18W EA	11236	750-81-R47K
A13R791	315-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A13R794	315-0331-00	B010100	B010338	RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A13R794	315-0271-00	B010339		RES,FXD,FILM:270 OHM,5%,0.25W	57668	NTR25J-E270E
A13R795	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A13R798	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A13U780	156-2466-00			MICROCKT,LINEAR:QUAD DIFF VOLT COMP	01295	TLC374CP
A13U781	156-2466-00			MICROCKT,LINEAR:QUAD DIFF VOLT COMP	01295	TLC374CP
A13U782	156-2466-00			MICROCKT,LINEAR:QUAD DIFF VOLT COMP	01295	TLC374CP
A13U783	156-2467-00			MICROCKT,LINEAR:DUAL DIFF VOLT COMP	01295	TLC372CP
A14	670-8698-00			CIRCUIT BD ASSY:LOGIC CH1 & CH2 (CH 1 LOGIC BOARD)	80009	670-8698-00
A14C5301	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C5302	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14J6111	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 3)	22526	48283-029
A14R5301	321-0292-00			RES,FXD,FILM:10.7K OHM,1%,0.125W,TC=T0	07716	CEAD10701F
A14R5302	321-0318-00			RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A14R5303	321-1713-07			RES,FXD,FILM:36K OHM 0.1%,0.125W,TC=T9	19701	5033RE36K00B
A14R5304	321-0373-00			RES,FXD,FILM:75.0K OHM,1%,0.125W,TC=T0	19701	5033ED75K00F
A14R5305	321-0292-00			RES,FXD,FILM:10.7K OHM,1%,0.125W,TC=T0	07716	CEAD10701F
A14R5306	321-0318-00			RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A14R5307	321-1713-07			RES,FXD,FILM:36K OHM 0.1%,0.125W,TC=T9	19701	5033RE36K00B
A14W5311	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A14W5312	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A15	670-8698-00			CIRCUIT BD ASSY:LOGIC CH1 & CH2 (CH 2 LOGIC BOARD)	80009	670-8698-00
A15C5321	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A15C5322	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A15J6112	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 3)	22526	48283-029
A15R5321	321-0292-00			RES,FXD,FILM:10.7K OHM,1%,0.125W,TC=T0	07716	CEAD10701F
A15R5322	321-0318-00			RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A15R5323	321-1713-07			RES,FXD,FILM:36K OHM 0.1%,0.125W,TC=T9	19701	5033RE36K00B
A15R5324	321-0373-00			RES,FXD,FILM:75.0K OHM,1%,0.125W,TC=T0	19701	5033ED75K00F
A15R5325	321-0292-00			RES,FXD,FILM:10.7K OHM,1%,0.125W,TC=T0	07716	CEAD10701F
A15R5326	321-0318-00			RES,FXD,FILM:20.0K OHM,1%,0.125W,TC=T0	19701	5033ED20K00F
A15R5327	321-1713-07			RES,FXD,FILM:36K OHM 0.1%,0.125W,TC=T9	19701	5033RE36K00B
A15W5321	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A15W5322	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A16	670-8706-00			CIRCUIT BD ASSY:SWEEP REF	80009	670-8706-00
A16C7501	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A16C7502	281-0770-00	B020242		CAP,FXD,CER DI:1000PF,20%,100V	04222	MA101C102MAA
A16CR721	152-0141-02	B021785		SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A16J5201	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A16J9410	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 7)	22526	48283-036
A16Q7501	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A16Q7502	151-0736-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0736-00
A16R721	311-2219-00			RES,VAR,NONWW:PNL,500 OHM,20%,0.5W,SPDT	12697	(ADVISE)
A16R7501	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125W,TC=T0	19701	5033ED2K00F
A16R7502	321-0269-00			RES,FXD,FILM:6.19K OHM,1%,0.125W,TC=T0	07716	CEAD61900F
A16R7504	315-0120-00			RES,FXD,FILM:12 OHM,5%,0.25W	57668	NTR25J-R12
A16R7505	321-0099-00			RES,FXD,FILM:105 OHM,1%,0.125W,TC=T0	07716	CEAD105R0F
A16R7505	321-0085-00			RES,FXD,FILM:75 OHM,1%,0.125W,TC=T0	57668	CRB14FXE 75 OHM
A16R7506	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A16R7507	311-2229-00			RES,VAR,NONWW:TRMR,250 OHM,20%,0.5W LINEAR	TK1450	GF06UT 250
A16R7507	311-2231-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W LINEAR	TK1450	GF06UT 1K
A16S721	----- -----			(PART OF R721)		
A16W5201	175-9849-00			CA ASSY,SP,ELEC:3,22 AWG,2.5 L,RIBBON	80009	175-9849-00
A17	670-8780-00			CIRCUIT BD ASSY:POSITION INTERFACE	80009	670-8780-00
A17J6113	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 4)	22526	48283-036
A17R120	321-0123-00			RES,FXD,FILM:187 OHM,1%,0.125W, TC=T0	07716	CEAD187R0F
A17R121	321-0123-00			RES,FXD,FILM:187 OHM,1%,0.125W, TC=T0	07716	CEAD187R0F
A17R170	321-0123-00			RES,FXD,FILM:187 OHM,1%,0.125W, TC=T0	07716	CEAD187R0F
A17R171	321-0123-00			RES,FXD,FILM:187 OHM,1%,0.125W, TC=T0	07716	CEAD187R0F
A17R7320	307-0706-00			RES NTWK,FXD,FI:4,10K OHM,2%,0.2W EA	01121	208B103
A17R7325	311-2238-00			RES,VAR,NONWW:TRMR,50K OHM,20%,0.5W LINEAR	TK1450	GF06UT 50 K
A17R7330	307-0706-00			RES NTWK,FXD,FI:4,10K OHM,2%,0.2W EA	01121	208B103
A17R7335	311-2238-00			RES,VAR,NONWW:TRMR,50K OHM,20%,0.5W LINEAR	TK1450	GF06UT 50 K
A18	670-8998-00			CIRCUIT BD ASSY:THERMAL SHUTDOWN	80009	670-8998-00
A18CR950	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A18CR951	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A18J1	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18Q950	151-0503-00			SCR:SI,TO-92	04713	SCR5138
A18R956	315-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A18R957	315-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A18R958	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A18R959	301-0103-00			RES,FXD,FILM:10K OHM,5%,0.50W	19701	5053CX10K00J
A18RT950	307-0662-00			RES,THERMAL:1K OHM,40%	50157	180Q10216
A18W950	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 3)	22526	48283-029
A20	670-8898-00	B010100	B021412	CIRCUIT BD ASSY:X-Y PLOTTER	80009	670-8898-00
A20	670-8898-01	B021413		CIRCUIT BD ASSY:X-Y PLOTTER	80009	670-8898-01
A20C1001	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A20C1002	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A20C1003	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A20C1004	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A20C1005	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A20C1006	281-0773-00	B010100	B011136	CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A20C1006	281-0775-00	B011137		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A20C1006	281-0775-01			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A20C1007	290-0297-00			CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A20C1011	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A20C1012	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A20C1013	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A20C1014	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A20C1015	290-0246-00	B010100	B021412	CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A20CR1001	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20CR1002	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20CR1003	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20CR1011	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20CR1012	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20CR1014	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20CR1016	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20F1001	159-0090-00			FUSE,WIRE LEAD:0.25A,125V,0.085SEC	TK0946	SP1-0.25 A
A20J1011	131-3390-00			CONN,RCPT,ELEC:D SUBMIN,CKT BD,9 CONTACT	13556	DE-9SV
A20J4110	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	48283-029
A20J6423	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 4)	22526	48283-029
A20J9301	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 5)	22526	48283-029
A20K1001	148-0086-00			RELAY,REED:FORM C,100MA,100VDC,COIL 5VDC	15636	R8149-1
A20L1001	108-0443-00			COIL,RF:FIXED,23.5UH	80009	108-0443-00
A20L1002	108-0443-00			COIL,RF:FIXED,23.5UH	80009	108-0443-00
A20L1003	108-0422-00	B010100	B021412	COIL,RF:FIXED,80UH	80009	108-0422-00
A20Q1011	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A20Q1012	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A20R1001	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A20R1002	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A20R1005	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A20R1011	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A20R1012	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A20R1013	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A20R1014	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A20R1015	315-0134-00			RES,FXD,FILM:130K OHM,5%,0.25W	57668	NTR25J-E130K
A20R1016	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A20R1017	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W	19701	5043CX1K100J
A20U1001	156-2667-00			MICROCKT,LINEAR:QUAD LOW PWR,OP AMPL	80009	156-2667-00
A20VR1011	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A20VR1012	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A20W1001	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A20W1002	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A20W1003	131-0566-00	B021413		BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A21	670-8899-00	B010100	B021935	CIRCUIT BD ASSY:RS232	80009	670-8899-00
A21	670-8899-01	B021936		CIRCUIT BD ASSY:RS232 (OPTION 12 ONLY)	80009	670-8899-01
A21B1	146-0056-01			BATTERY,DRY:3.0V,1200 MAH,LITHIUM	TK0196	84313B1
A21C1001	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1002	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1003	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1004	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1005	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1006	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1007	290-0297-00			CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A21C1011	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A21C1012	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A21C1013	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A21C1014	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A21C1015	290-0246-00	B010100	B021935	CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A21C1221	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1222	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1223	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1224	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1225	283-0197-00			CAP,FXD,CER DI:470PF,5%,50V	04222	SR205A471JAA
A21C1226	283-0197-00			CAP,FXD,CER DI:470PF,5%,50V	04222	SR205A471JAA
A21C1227	283-0197-00			CAP,FXD,CER DI:470PF,5%,50V	04222	SR205A471JAA
A21C1228	283-0197-00			CAP,FXD,CER DI:470PF,5%,50V	04222	SR205A471JAA
A21C1229	283-0197-00			CAP,FXD,CER DI:470PF,5%,50V	04222	SR205A471JAA
A21C1232	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1233	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1234	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1235	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1236	283-0197-00			CAP,FXD,CER DI:470PF,5%,50V	04222	SR205A471JAA
A21C1237	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1238	283-0197-00			CAP,FXD,CER DI:470PF,5%,50V	04222	SR205A471JAA
A21C1239	283-0197-00			CAP,FXD,CER DI:470PF,5%,50V	04222	SR205A471JAA
A21C1240	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A21C1242	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1243	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1244	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1251	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A21C1252	283-0639-00			CAP,FXD,MICA DI:56PF,1%,100V	00853	D155E560F0
A21C1253	283-0639-00			CAP,FXD,MICA DI:56PF,1%,100V	00853	D155E560F0
A21CR1001	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21CR1002	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21CR1003	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21CR1011	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21CR1012	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21CR1014	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21CR1016	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21CR1221	152-0834-01			SEMICOND DVC,DI:16 DIODE ARRAY,COMMON ANODE	80009	152-0834-01
A21CR1222	152-0835-01			SEMICOND DVC,DI:16 DIODE ARRAY,COM CATHODE	80009	152-0835-01
A21CR1223	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21CR1224	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A21E1011	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A21F1001	159-0090-00			FUSE,WIRE LEAD:0.25A,125V,0.085SEC	TK0946	SP1-0.25 A
A21J1011	131-3390-00			CONN,RCPT,ELEC:D SUBMIN,CKT BD,9 CONTACT	13556	DE-9SV
A21J1212	131-0813-00			CONN,RCPT,ELEC:CKT BD MT,25 CONT,MALE	13511	777-DB-25P-T
A21J1214	131-0971-00			CONN,RCPT,ELEC:CKT BD MT,25 CONTACT,FEMALE	71468	DB25-SH
A21J1216	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A21J1217	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A21J1222	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 20)	22526	48283-029
A21J1231	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A21J1242	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A21J1251	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 20)	22526	48283-029
A21J4110	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	48283-029
A21J6423	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 4)	22526	48283-029
A21J9301	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029

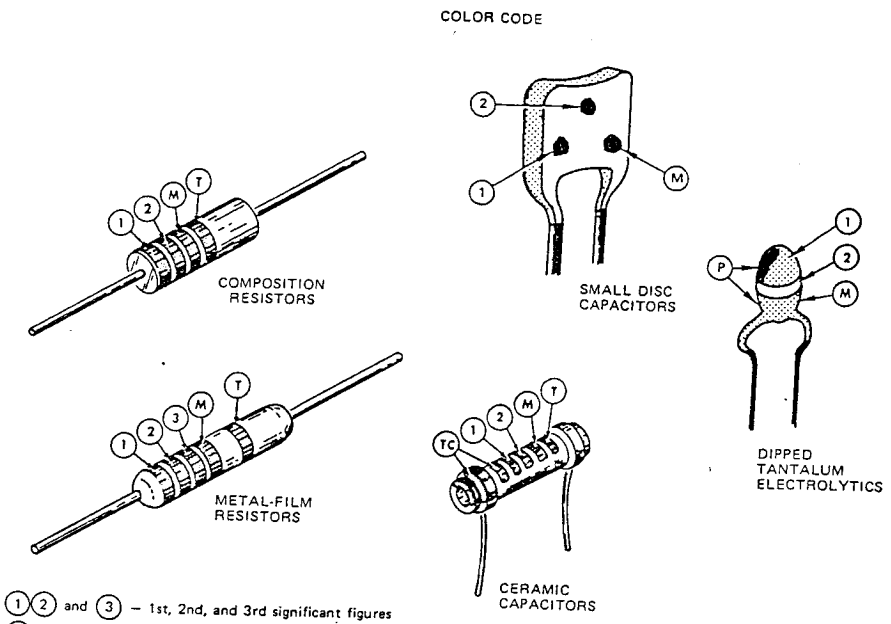
Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
				(QUANTITY OF 5)		
A21K1001	148-0086-00			RELAY,REED:FORM C,100MA,100VDC,COIL 5VDC	15636	R8149-1
A21L1001	108-0443-00			COIL,RF:FIXED,23.5UH	80009	108-0443-00
A21L1002	108-0443-00			COIL,RF:FIXED,23.5UH	80009	108-0443-00
A21L1003	108-0422-00	B010100	B021935	COIL,RF:FIXED,80UH	80009	108-0422-00
A21Q1011	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A21Q1012	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A21Q1221	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A21R1001	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A21R1002	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A21R1005	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A21R1011	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A21R1012	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A21R1013	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A21R1014	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A21R1015	315-0134-00			RES,FXD,FILM:130K OHM,5%,0.25W	57668	NTR25J-E130K
A21R1016	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A21R1017	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W	19701	5043CX1K100J
A21R1212	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A21R1213	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A21R1214	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A21R1221	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1222	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A21R1223	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1224	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A21R1234	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1235	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A21R1243	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1244	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1245	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1246	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1248	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1251	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1252	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1253	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A21R1255	315-0106-00			RES,FXD,FILM:10M OHM,5%,0.25W	01121	CB1065
A21S1221	260-2272-00			SWITCH,ROCKER:SPST,2.5A,28V	97525	240010GP
A21U1001	156-2667-00			MICROCKT,LINEAR:QUAD LOW PWR,OP AMPL	80009	156-2667-00
A21U1222	156-2391-00			MICROCKT,DGTL:OCT BUF/DRVR W/3 ST OUT	01295	SN74ALS541N3
A21U1223	156-2391-00			MICROCKT,DGTL:OCT BUF/DRVR W/3 ST OUT	01295	SN74ALS541N3
A21U1224	156-0878-01	B010100	B022299	MICROCKT,DGTL:QUAD LINE RCVR	04713	MC1489LDS
A21U1224	156-0878-00	B022300		MICROCKT,DGTL:QUAD LINE RECIEVER	04713	MC1489L
A21U1225	156-0879-01	B010100	B022299	MICROCKT,DGTL:QUAD LINE DRIVER	04713	MC1488LD
A21U1225	156-0879-00	B022300		MICROCKT,DGTL:QUAD LINE DRIVER	04713	MC1488
A21U1231	156-1748-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3-STATE OUT	01295	SN74ALS245AN3
A21U1232	156-0875-02	B010100	B022299	MICROCKT,DGTL:DUAL 2-W/2 INP AOI GATES	04713	SN74LS51NDS
A21U1232	156-0875-00	B022300		MICROCKT,DGTL:DUAL 2-WIDE 2-INP AOI GATES	01295	SN74LS51(N OR J)
A21U1233	156-2391-00			MICROCKT,DGTL:OCT BUF/DRVR W/3 ST OUT	01295	SN74ALS541N3
A21U1234	156-2093-00			MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3
A21U1235	156-1432-02	B010100	B022299	MICROCKT,DGTL:DUAL 2/4 LINE DECODER/DEMUX	01295	SN74LS156 NP3
A21U1235	156-1432-00	B022300		MICROCKT,DGTL:DUAL 2/4 LINE DECODER/DEMUX	18324	N74LS156 N
A21U1236	156-2603-00			MICROCKT,DGTL:CMOS,ADDRESSABLE LATCH,8 BIT	02735	CD74HCT259E
A21U1241	156-2391-00			MICROCKT,DGTL:OCT BUF/DRVR W/3 ST OUT	01295	SN74ALS541N3
A21U1242	156-2012-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM,SCREENED	80009	156-2012-00
A21U1243	160-2998-00	B010100	B021935	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-00
A21U1243	160-2998-07	B021936	B022326	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-07
A21U1243	160-2998-08	B022327	B023053	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-08
A21U1243	160-2998-09	B023054		MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-09

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A21U1244	156-2094-00			MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS04BN3/J4
A21U1245	156-2488-00			MICROCKT,DGTL:ASTTL,DECODE/DEMUX,OCTAL	07263	74F548 PCQR
A21U1251	156-2438-00			MICROCKT,DGTL:CMOS,SERIAL COMM INTERFACE	34371	CD82C52/B
A21U1343	160-2998-00	B010100	B021935	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-00
A21U1343	160-2998-07	B021936	B022326	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-07
A21U1343	160-2998-08	B022327	B023053	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-08
A21U1343	160-2998-09	B023054		MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-09
A21VR1011	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A21VR1012	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A21VR1221	152-0520-00			SEMICOND DVC,DI:ZEN,SI,12V,5%,1W,DO-41	80009	152-0520-00
A21VR1222	152-0520-00			SEMICOND DVC,DI:ZEN,SI,12V,5%,1W,DO-41	80009	152-0520-00
A21VR1223	152-0520-00			SEMICOND DVC,DI:ZEN,SI,12V,5%,1W,DO-41	80009	152-0520-00
A21VR1224	152-0520-00			SEMICOND DVC,DI:ZEN,SI,12V,5%,1W,DO-41	80009	152-0520-00
A21VR1232	152-0667-00			SEMICOND DVC,DI:ZEN,SI,3.0 V # 2% AT 2MA	04713	SZG30025RL
A21W1001	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A21W1002	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A21W1003	131-0566-00	B021936		BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A21W1216	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A21W1217	196-3137-00			LEAD,ELECTRICAL:26 AWG,5.6 L	80009	196-3137-00
A21W8101	175-9847-00			CA ASSY,SP,ELEC:50,28 AWG,2.5 L,RIBBON	80009	175-9847-00
A21Y1251	158-0124-00			XTAL UNIT,QTZ:2.4576 MHZ,0.05%,PARALLEL	01807	Z9W
A22	670-8900-00	B010100	B021759	CIRCUIT BD ASSY:GPIB	80009	670-8900-00
A22	670-8900-01	B021760		CIRCUIT BD ASSY:GPIB (OPTION 10 ONLY)	80009	670-8900-01
A22B1	146-0056-00			BATTERY,DRY:3.0V,1200 MAH,LITHIUM,ASSY,7 IN CH LEADS,5 PIN HARMONICA CONNECTOR	TK0196	8431381
A22C1001	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1002	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1003	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1004	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A22C1005	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A22C1006	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A22C1007	290-0297-00			CAP,FXD,ELCTLT:39UF,10%,10V	05397	T110B396K010AS
A22C1011	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A22C1012	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A22C1013	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A22C1014	290-0246-00			CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A22C1015	290-0246-00	B010100	B021759	CAP,FXD,ELCTLT:3.3UF,10%,15V	12954	D3R3EA15K1
A22C1321	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1322	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1323	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1331	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1332	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A22C1333	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A22C1334	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1335	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1342	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A22C1343	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A22C1351	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A22CR1001	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A22CR1002	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A22CR1003	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A22CR1011	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A22CR1012	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A22CR1014	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A22CR1016	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A22CR1321	152-0834-01			SEMICOND DVC,DI:16 DIODE ARRAY,COMMON ANODE	80009	152-0834-01
A22CR1322	152-0835-01			SEMICOND DVC,DI:16 DIODE ARRAY,COM CATHODE	80009	152-0835-01
A22F1001	159-0090-00			FUSE,WIRE LEAD:0.25A,125V,0.085SEC	TK0946	SP1-0.25 A
A22J1011	131-3390-00			CONN,RCPT,ELEC:D SUBMIN,CKT BD,9 CONTACT	13556	DE-9SV
A22J1314	131-2203-01			CONN,RCPT,ELEC:CKT BD,24 CONT,FEMALE	74868	57202401 4(398)
A22J1316	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A22J1317	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A22J1322	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 20)	22526	48283-029
A22J1331	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A22J1342	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A22J1351	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 20)	22526	48283-029
A22J4110	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	48283-029
A22J6423	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 4)	22526	48283-029
A22J9301	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 5)	22526	48283-029
A22K1001	148-0086-00			RELAY,REED:FORM C,100MA,100VDC,COIL 5VDC	15636	R8149-1
A22L1001	108-0443-00			COIL,RF:FIXED,23.5UH	80009	108-0443-00
A22L1002	108-0443-00			COIL,RF:FIXED,23.5UH	80009	108-0443-00
A22L1003	108-0422-00	B010100	B021759	COIL,RF:FIXED,80UH	80009	108-0422-00
A22Q1011	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A22Q1012	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A22R1001	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A22R1002	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A22R1005	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A22R1011	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A22R1012	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A22R1013	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A22R1014	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A22R1015	315-0134-00			RES,FXD,FILM:130K OHM,5%,0.25W	57668	NTR25J-E130K
A22R1016	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A22R1017	315-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.25W	19701	5043CX1K100J
A22R1321	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1322	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A22R1323	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1335	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A22R1341	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1342	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1343	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1344	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1345	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1346	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1348	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1351	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1352	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22R1353	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A22S1321	260-2272-00			SWITCH,ROCKER:SPST,2.5A,28V	97525	240010GP
A22U1001	156-2667-00			MICROCKT,LINEAR:QUAD LOW PWR,OP AMPL	80009	156-2667-00
A22U1243	160-2998-05			MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-05
A22U1322	156-2391-00			MICROCKT,DGTL:OCT BUF/DRVR W/3 ST OUT	01295	SN74ALS541N3
A22U1323	156-2391-00			MICROCKT,DGTL:OCT BUF/DRVR W/3 ST OUT	01295	SN74ALS541N3
A22U1324	156-1415-01	B010100	B022299	MICROCKT,DGTL:OCTAL GPIB XCVR-MANAGEMENT	27014	DS75161A NA+
A22U1324	156-1415-00	B022300		MICROCKT,DGTL:TTL,OCTAL GPIB XCVR MGT BUS	01295	SN75161A N
A22U1325	156-1414-02	B010100	B022299	MICROCKT,DGTL:OCTAL GPIB BUS XCVR,SCRN	27014	DS75160A N
A22U1325	156-1414-00	B022300		MICROCKT,DGTL:TTL,OCTAL GPIB XCVR DATA BUS	01295	SN75160 (N OR J)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A22U1331	156-1748-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3-STATE OUT	01295	SN74ALS245AN3
A22U1332	156-0875-02	B010100	B022299	MICROCKT,DGTL:DUAL 2-W/2 INP AOI GATES	04713	SN74LS51NDS
A22U1332	156-0875-00	B022300		MICROCKT,DGTL:DUAL 2-WIDE 2-INP AOI GATES	01295	SN74LS51(N OR J)
A22U1333	156-2391-00			MICROCKT,DGTL:OCT BUF/DRVR W/3 ST OUT	01295	SN74ALS541N3
A22U1334	156-2093-00			MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3
A22U1335	156-1919-00			MICROCKT,DGTL:DUAL POS EDGE TRIG FLIP-FLOP	04713	MC74F109 ND/JD
A22U1336	156-2095-00			MICROCKT,DGTL:QUAD 2-INP EXCLUSIVE OR GATES	01295	SN74ALS86N3/J4
A22U1341	156-2391-00			MICROCKT,DGTL:OCT BUF/DRVR W/3 ST OUT	01295	SN74ALS541N3
A22U1342	156-2012-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM,SCREENED	80009	156-2012-00
A22U1343	160-2998-00	B010100	B021935	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-00
A22U1343	160-2998-07	B021936	B022326	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-07
A22U1343	160-2998-08	B022327		MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-2998-08
A22U1344	156-2094-00			MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS04BN3/J4
A22U1345	156-2488-00			MICROCKT,DGTL:ASTTL,DECODE/DEMUX,OCTAL	07263	74F548 PCQR
A22U1351	156-1444-01			MICROCKT,DGTL:NMOS,GPIB INTFC CONTROLLER	01295	TMS9914A (NL
A22VR1011	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A22VR1012	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A22VR1321	152-0757-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,1W,DO-41	04713	1N4735A
A22W1001	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A22W1002	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A22W1003	131-0566-00	B021760		BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A22W1316	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A22W1324	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A22W1341	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A22W8101	175-9847-00			CA ASSY,SP,ELEC:50,28 AWG,2.5 L,RIBBON	80009	175-9847-00
A23	670-8952-00	B010100	B021935	CIRCUIT BD ASSY:OPT MEMORY	80009	670-8952-00
A23	670-8952-01	B021936		CIRCUIT BD ASSY:A23 OPTION MEMORY (OPTION 12,10 ONLY)	80009	670-8952-01
A23C1106	290-0983-00			CAP,FXD,ELCTLT:4.7UF,5%,10VDC	56289	150D475X5010A2
A23C1112	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A23C1118	285-0674-00			CAP,FXD,PLASTIC:0.01UF,10%,100V	84411	TEK270-10391
A23C1120	290-0920-00			CAP,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TAAANA
A23C1128	285-0808-00			CAP,FXD,PLASTIC:0.1UF,10%,50V	04099	EK13-16
A23C1132	283-0108-02			CAP,FXD,CER DI:220PF,10%,200V	56289	ORDER BY DESCR
A23C1134	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A23C1138	285-0674-00			CAP,FXD,PLASTIC:0.01UF,10%,100V	84411	TEK270-10391
A23C1142	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A23C1143	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A23C1148	285-0808-00			CAP,FXD,PLASTIC:0.1UF,10%,50V	04099	EK13-16
A23C1154	283-0341-00			CAP,FXD,CER DI:0.047UF,10%,100V	04222	SR301C473KAA
A23C1156	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A23CR1102	152-0664-00			SEMICOND DVC,DI:SCHOTTKY,SW,SI,70V,DO-35	80009	152-0664-00
A23CR1104	152-0664-00			SEMICOND DVC,DI:SCHOTTKY,SW,SI,70V,DO-35	80009	152-0664-00
A23J1152	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 3)	22526	48283-029
A23L1104	108-0109-00			COIL,RF:FIXED,63UH	TK2042	ORDER BY DESCR
A23P1122	131-2515-00			CONN,RCPT,ELEC:CKT BD,2 X 10,FEMALE	00779	86418-1
A23P1151	131-2515-00			CONN,RCPT,ELEC:CKT BD,2 X 10,FEMALE	00779	86418-1
A23R1112	321-0277-03			RES,FXD,FILM:7.50K OHM,0.25%,0.125W,T=T2	01121	ORDER BY DESCR
A23R1114	321-0652-00			RES,FXD,FILM:145K OHM,0.25%,0.125W,TC=T9	07716	CEAE14502C
A23R1116	321-1693-07			RES,FXD,FILM:46.67K OHM,0.1%,0.125W,T-9	07716	CEAE46671B
A23R1132	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A23R1134	321-0983-00			RES,FXD,FILM:4.5 MEG OHM,1%,0.125W,TC=T0	91637	CMF55116-G45003F
A23R1144	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A23R1150	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A23R1152	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A23R1154	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A23R1156	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A23RT1102	307-1211-00			RES,THERMAL:400 OHM,30%,28VDC	50157	P-58188
A23U1118	156-2483-00			MICROCKT,DGTL:CMOS,8192 X 8,150NS	TK0961	uPD4464C-15
A23U1122	156-2445-00			MICROCKT,LINEAR:PROGRAMMABLE VOLTAGE REF	32293	ICL8212CPA
A23U1128	156-2483-00			MICROCKT,DGTL:CMOS,8192 X 8,150NS	TK0961	uPD4464C-15
A23U1132	156-2392-00			MICROCKT,DGTL:CMOS,HEX SCHMITT TRIG INV	04713	MC74HC14ND
A23U1138	156-2483-00			MICROCKT,DGTL:CMOS,8192 X 8,150NS	TK0961	uPD4464C-15
A23U1142	156-0411-02			MICROCKT,LINEAR:QUAD COMPARATOR,SCREENED	04713	LM339JDS
A23U1148	156-2483-00			MICROCKT,DGTL:CMOS,8192 X 8,150NS	TK0961	uPD4464C-15
A23U1162	156-2293-00			MICROCKT,DGTL:DUAL 2 TO 4-LINE DECODER/MUX	01295	SN74ALS139N3
A23W101	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 X 0.225	24546	OMA 07
A24	670-9701-00	B020000		CIRCUIT BD ASSY:CURSOR CONTROL	80009	670-9701-00
A24J9430	131-3058-00	B020000		CONN,RCPT,ELEC:HEADER,RTANG,2 X 3,0.1 CTR	00779	1-86479-5
A24R9412	311-2285-01	B020000		RES,VAR,NONWW:CKT BD,10K OHM,20%,0.25W	12697	MODEL388(ADVISE)
A24S9412	----- -----	B020080		(PART OF R9412)		
A24W9430	174-0260-00	B020000		CA ASSY,SP,ELEC:6,26 AWG,3.0 L,RIBBON	80009	174-0260-00
B9965	119-0830-07			FAN,TUBEAXIAL:12VDC,2.4W,6500 RPM,31 CFM	TK0146	69.11.56 W/6"LEA
C7401	283-0003-00			CAP,FXD,CER DI:0.01UF,+80-20%,150V	59821	D103Z40Z5UJDCEX
C7402	283-0003-00			CAP,FXD,CER DI:0.01UF,+80-20%,150V	59821	D103Z40Z5UJDCEX
C9272	281-0534-00			CAP,FXD,CER DI:3.3PF,+/-0.25PF,500V	52763	2RDPLZ007 3P3OCC
C9273	281-0534-00			CAP,FXD,CER DI:3.3PF,+/-0.25PF,500V	52763	2RDPLZ007 3P3OCC
CR970	152-0600-00			SEMICOND DVC,DI:SCHOTTKY,RECT,SI,35V,15A	04713	MBR1535CT
DL9210	119-1515-00			DELAY LINE,ELEC:93NS,150 OHM,ASSEMBLY	80009	119-1515-00
DS518	150-1029-00			LT EMITTING DIO:GREEN,565NM,35MA	58361	Q6480/MV5274C
DS9150	150-1071-00			LT EMITTING DIO:GREEN,565NM,20MA MAX	50434	HLMP3910
F1001	159-0253-00			FUSE,CARTRIDGE:0.250A,125V,FAST,SUBMINI	75915	251.250 T & R T1
F9001	159-0023-00			FUSE,CARTRIDGE:3AG,2A,250V,SLOW BLOW	71400	MDX2
FL9001	119-1788-00			LINE FLTR ASSY:	80009	119-1788-00
J9100	131-0679-02			CONN,RCPT,ELEC:BNC,MALE,3 CONTACT	24931	28JR270-1
J9376	131-0955-00			CONN,RCPT,ELEC:BNC,FEMALE	13511	31-279
J9510	131-0679-02			CONN,RCPT,ELEC:BNC,MALE,3 CONTACT	24931	28JR270-1
J9800	131-0955-00			CONN,RCPT,ELEC:BNC,FEMALE	13511	31-279
P9900	136-0628-00			JACK,TIP:W/WIRE	80009	136-0628-00
Q9070	151-1141-00			TRANSISTOR:FE,N-CHANNEL,SI,TO-220	04713	STP3000
R5202	315-0300-00			RES,FXD,FILM:30 OHM,5%,0.25W	19701	5043CX30R00J
R5203	315-0300-00			RES,FXD,FILM:30 OHM,5%,0.25W	19701	5043CX30R00J
R9272	301-0121-00			RES,FXD,FILM:120 OHM,5%,0.5W	19701	5053CX120K0
R9273	301-0121-00			RES,FXD,FILM:120 OHM,5%,0.5W	19701	5053CX120K0
R9376	315-0430-00			RES,FXD,FILM:43 OHM,5%,0.25W	19701	5043CX43R00J
R9521	311-2146-00			RES,VAR,NONWW:CKT BD,50 OHM,20%,0.5W	01121	WA1G040S503MZ
R9644	311-2158-01			RES,VAR,WW:PNL,5K OHM,5%,1W,W/RIBBON	80009	311-2158-01
R9802	311-2177-02	B010100	B022529	RES,VAR,NONWW:W/PLATE & CABLE	80009	311-2177-02
R9802	311-2177-03	B022530		RES,VAR,NONWW:PNL,10K OHM,20%,0.5W	80009	311-2177-03
V9870	154-0861-00			ELECTRON TUBE:	80009	154-0861-00
W9150	175-2546-01			CA ASSY,SP,ELEC:2,26 AWG,3.0 L,RIBBON	80009	175-2546-01
W9272	119-1505-01			DEFL LEAD ASSY:CAP/RES/ELEC LEAD,2.0 L	80009	119-1505-01
W9273	119-1506-01			DEFL LEAD ASSY:CAP/RES/ELEC LEAD,2.5 L	80009	119-1506-01



COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER	TOLERANCE	MULTIPLIER	TOLERANCE over 10 pF	TOLERANCE under 10 pF	
BLACK	0	1	–––	1	±20%	±2 pF	4 VDC
BROWN	1	10	±1%	10	±1%	±0.1 pF	6 VDC
RED	2	10^2 or 100	±2%	10^2 or 100	±2%	–––	10 VDC
ORANGE	3	10^3 or 1 K	±3%	10^3 or 1000	±3%	–––	15 VDC
YELLOW	4	10^4 or 10 K	±4%	10^4 or 10,000	+100% –9%	–––	20 VDC
GREEN	5	10^5 or 100 K	±½%	10^5 or 100,000	±5%	±0.5 pF	25 VDC
BLUE	6	10^6 or 1 M	±¼%	10^6 or 1,000,000	–––	–––	35 VDC
VIOLET	7	–––	±1/10%	–––	–––	–––	50 VDC
GRAY	8	–––	–––	10^{-2} or 0.01	+80% –20%	±0.25 pF	–––
WHITE	9	–––	–––	10^{-1} or 0.1	±10%	±1 pF	3 VDC
GOLD	–	10^{-1} or 0.1	±5%	–––	–––	–––	–––
SILVER	–	10^{-2} or 0.01	±10%	–––	–––	–––	–––
NONE	–	–––	±20%	–––	±10%	±1 pF	–––

(1861-20A) 2662-48

Figure 9-1. Color codes for resistors and capacitors.

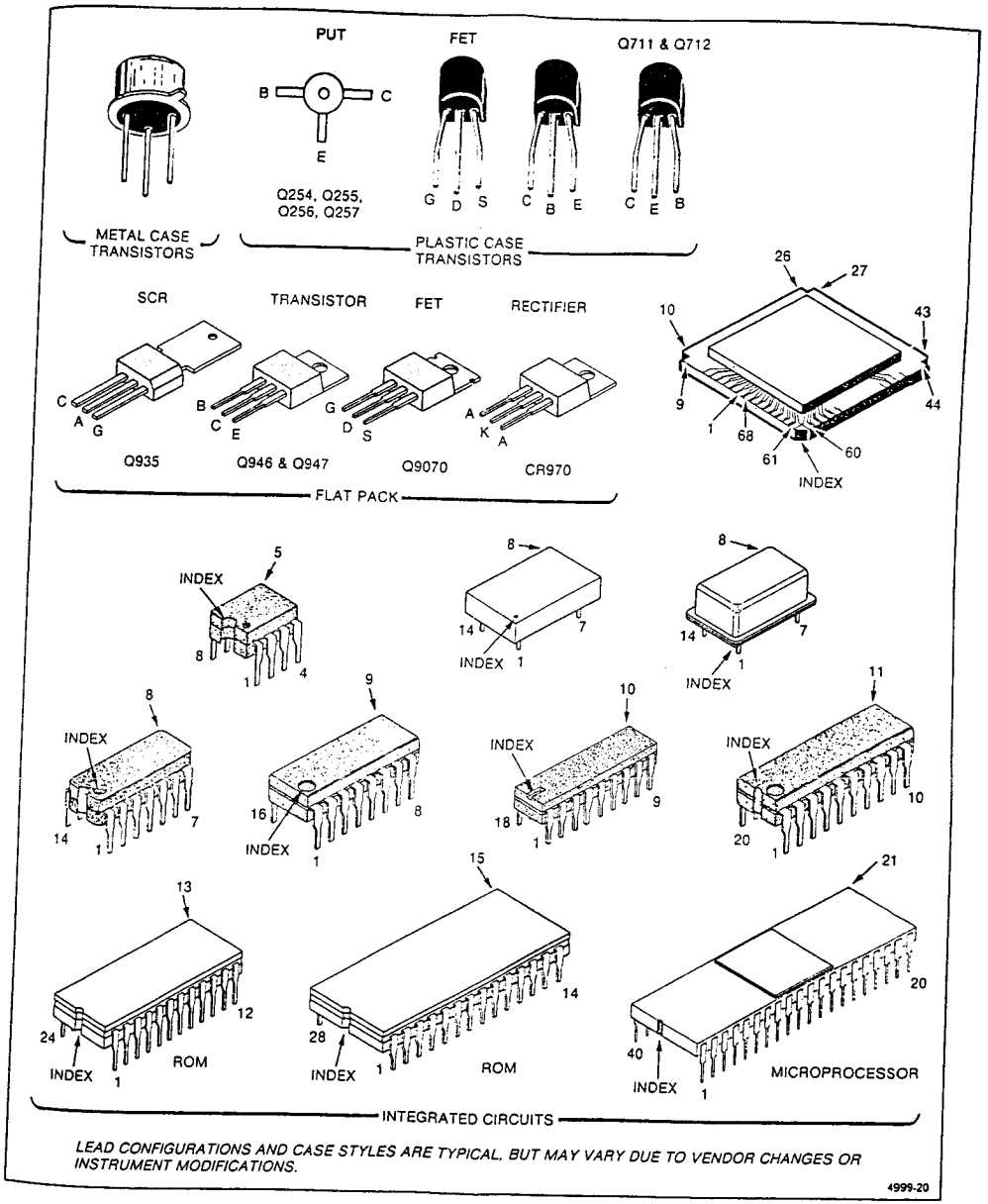


Figure 9-2. Semiconductor lead configurations.

TEST WAVEFORM AND VOLTAGE SETUPS

WAVEFORM MEASUREMENTS

On the left-hand pages preceding the schematic diagrams are test waveform illustrations that are intended to aid in troubleshooting the instrument. To test the instrument for these waveforms, make the initial control settings as follows:

Vertical (Both Channels)

POSITION	Midrange
VERTICAL MODE	CH 1
X-Y	Off (button out)
BW LIMIT	On (button in)
VOLTS/DIV	1 V
VOLTS/DIV Variable	CAL detent
INVERT	Off (button out)
AC-GND-DC	DC

Horizontal

POSITION	(Midrange)
HORIZONTAL MODE	A
A SEC/DIV	0.5 ms
SEC/DIV Variable	CAL detent
X10 Magnifier	Off (knob in)

A TRIGGER

VAR HOLDOFF	NORM
Mode	P-P AUTO
SLOPE	OUT
LEVEL	Midrange
HF REJECT	OFF
A&B INT	VERT MODE
A SOURCE	INT
A EXT COUPLING	AC

Storage

STORE/NON STORE	NON STORE (button out)
SAVE/CONTINUE	CONTINUE (button out)
PRETRIG/POST TRIG	POST TRIG (button out)
ROLL/SCAN	SCAN (button out)
1K/4K	4K (button out)
POSITION CURS/ SELECT WAVEFORM	POSITION CURS (button in)
WAVEFORM REFERENCE	WAVEFORM REFERENCE (button in)

Changes to the control settings for specific waveforms are noted at the beginning of each set of waveforms. Input signals and hookups required are also indicated, if needed, for each set of waveforms. Voltage measurements are made with a 1X probe unless otherwise noted.

DC VOLTAGE MEASUREMENTS

Typical voltage measurements, located on the schematic diagram, were obtained with the instrument operating under the conditions specified in the Waveforms Measurements setup. Control-setting changes required for specific voltages are indicated on each waveforms page. Measurements are referenced to chassis ground with the exception of the Preregulator and Inverter voltages on Diagram 8. These voltages are referenced as indicated on the schematic diagram.

RECOMMENDED TEST EQUIPMENT

Test equipment in Table 4-1 meets the required specifications for testing this instrument.

POWER SUPPLY ISOLATION PROCEDURE

Each regulated supply has numerous feed points to external loads throughout the instrument. The power distribution diagrams are used in conjunction with the schematic diagrams to determine those loads that can be isolated by removing service jumpers and those that cannot.

The power distribution and circuit board interconnections diagrams are divided into circuit boards. Each power supply feed to a circuit board is indicated by the schematic diagram number on which the voltage appears. The schematic diagram grid location of a service jumper or component is given adjacent to the component number on the power distribution and circuit board interconnect diagrams.

If a power supply comes up after lifting one of the main jumpers from the power supply to isolate that supply, it is very probable that a short exists in the circuitry on that supply line. By lifting jumpers farther down the line, the circuit in which a short exists may be located.

Always set the POWER switch to OFF before soldering or unsoldering service jumpers or other components and before attempting to measure component resistance values.

AC Waveforms

WARNING

Instrument must be connected to the ac-power source using a 1:1 isolation transformer. Do not connect the test oscilloscope probe ground lead to the inverter circuit test points if the instrument is not isolated. AC-source voltage exists on reference points TP950 and T906 pin 5.

DC Voltages

Preregulator and Inverter voltages are referenced to test point noted adjacent to the voltage. Power supply output voltages are referenced to chassis ground.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
B9965	9	P7393	2
BT1101	25	P8100	23
		P8100	24
C7401	1	P9010	12
C7402	1	P9050	12
		P9060	12
DS9150	8	P9070	8
		P9105C	14
F9001	8	P9200	1
		P9210	12
FL9001	8	P9250	4
		P9250	7
J9100	1	P9272	3
J9376	4	P9273	3
J9510	1	P9320	12
J9800	9	P9410	12
		P9430	14
P1152	25	P9700	5
P4104	18	P9700	6
P4110	12	P9700	7
P4210	12	P9705	10
P4220	12	P9705	7
P6100	19	P9778	7
P6100	20	P9788	7
P6100	21	P9802	9
P6110	13	P9965	9
P6111	13	P9991	10
P6112	13		
P6113	13	R5202	7
P6120	13	R5203	7
P6130	13	R9521	5
P6410	13		
P6420	13	V9870	9
P6421	13		
P6423	13	W9272	3
P7390	2		
P7391	2		
P7392	2		

A2—ATTENUATOR BOARD

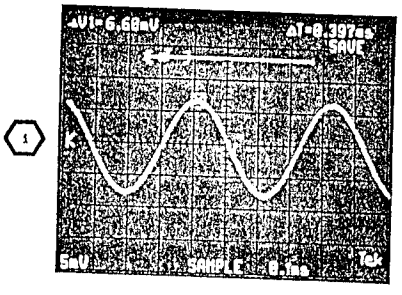
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
AT1	1	L91	10	R52	1	C56	1	R17	1	R84	1
AT2	1	L93	10	R53	1	C57	1	R18	1	R85	1
AT51	1	L96	10	R54	1	C59	1	R19	1	R87	1
AT52	1	P9200	1	R55	1	C60	1	R21	1	R88	1
C2	1	Q13	1	R56	1	C61	1	R22	1	R91	1
C3	1	Q15	1	R57	1	C63	1	R23	1	R93	1
C4	1	Q18	1	R58	1	C67	1	R25	1	R96	1
C5	1	Q63	1	R59	1	C71	1	R26	1	R97	1
C6	1	Q65	1	R60	1	C76	1	R27	1	R98	1
C6	1	Q68	1	R61	1	C77	1	R29	1	S1	1
C7	1	R1	1	R62	1	C80	1	R30	1	S10	1
C9	1	R1	1	R63	1	C85	1	R30	1	S43	1
C9	1	R2	1	R64	1	C88	1	R31	1	S51	1
C10	1	R3	1	R65	1	C90	10	R33	1	S80	1
C11	1	R4	1	R66	1	C91	10	R34	1	S93	1
C13	1	R5	1	R67	1	C93	10	R35	1	U10	1
C17	1	R6	1	R68	1	C94	10	R37	1	U10	10
C21	1	R6	1	R69	1	C96	10	R38	1	U30	1
C26	1	R7	1	R71	1	C97	10	R39	1	U60	1
C27	1	R8	1	R72	1	CR7	1	R41	1	U60	10
C30	1	R9	1	R73	1	CR18	1	R42	1	U80	1
C30	1	R10	1	R75	1	CR57	1	R43	1	VR10	10
C35	1	R11	1	R76	1	CR68	1	R46	1	VR60	10
C38	1	R12	1	R77	1	J9103	1	R47	1	W43	1
C52	1	R13	1	R79	1	J9108	1	R48	1	W93	1
C53	1	R14	1	R80	1	J9991	10	R51	1	W94	10
C54	1	R15	1	R81	1	L90	10	R51	1	W96	10
C55	1	R16	1	R83	1						

A14—CH 1 LOGIC BOARD

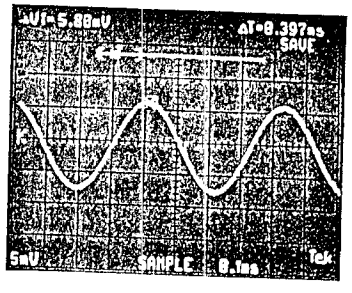
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C5301	1	R5302	1	R5306	1
C5302	1	R5303	1	R5307	1
J6111	1	R5304	1	W5311	1
R5301	1	R5305	1	W5312	1

A15—CH 2 LOGIC BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C5321	1	R5322	1	R5326	1
C5322	1	R5323	1	R5327	1
J6112	1	R5324	1	W5321	1
R5321	1	R5325	1	W5322	1

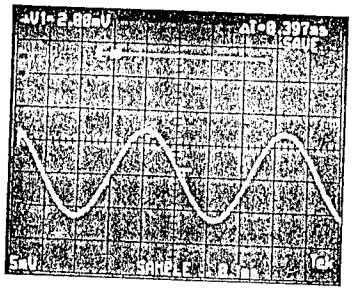


1



2

WAVEFORMS FOR DIAGRAM 1



3

4999-81

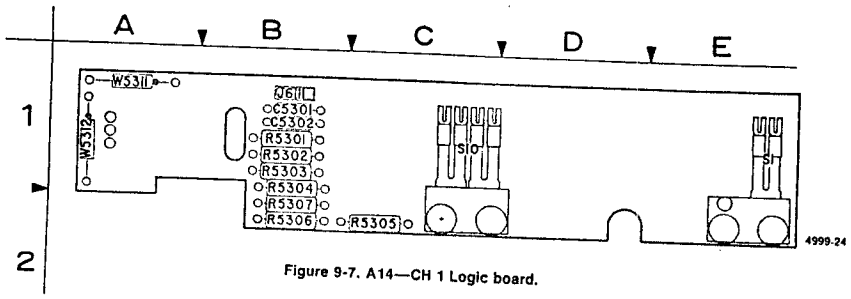


Figure 9-7. A14—CH 1 Logic board.

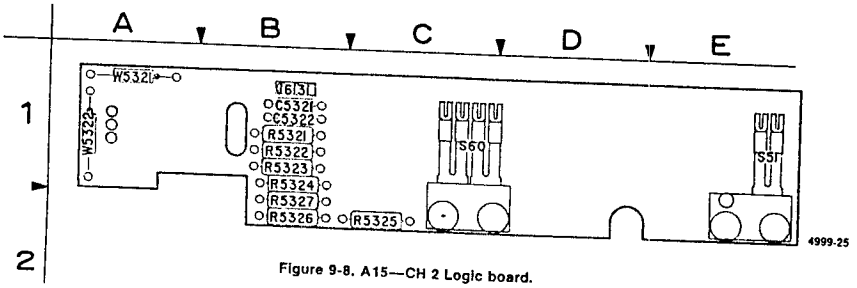
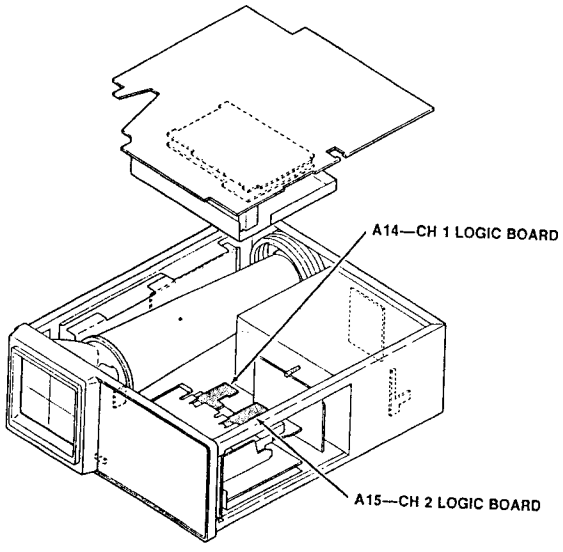


Figure 9-8. A15—CH 2 Logic board.



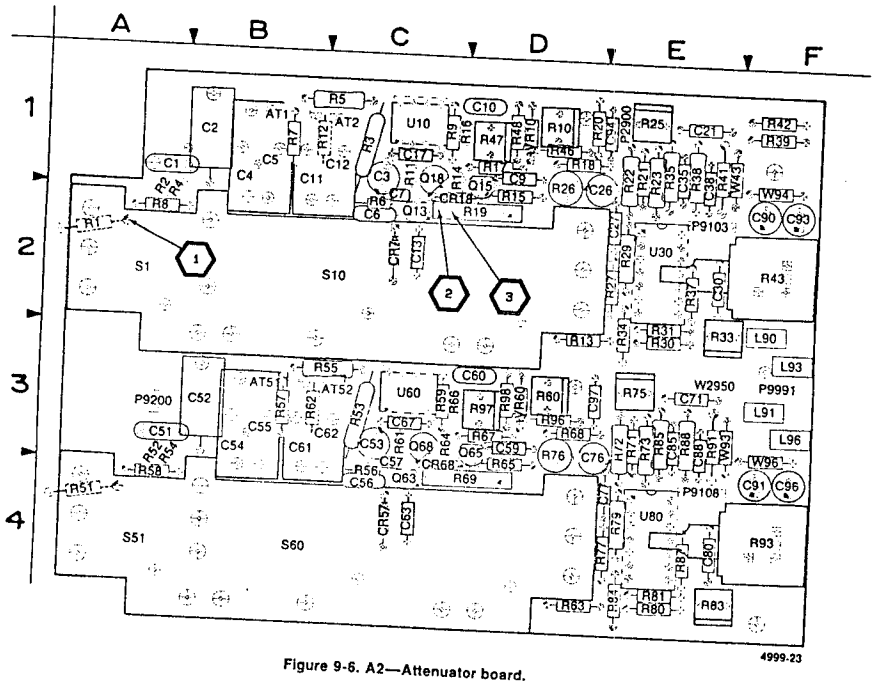
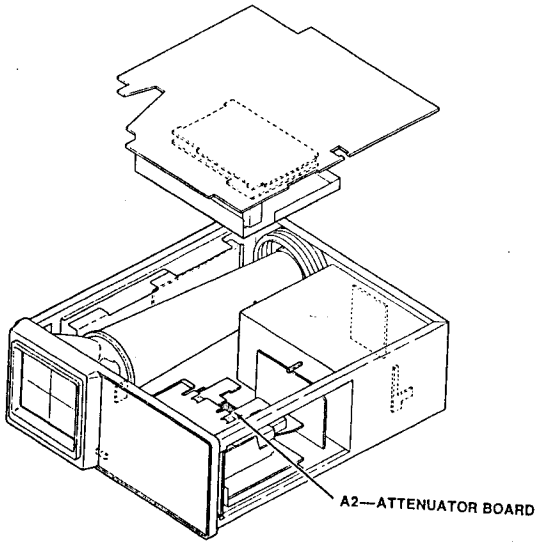
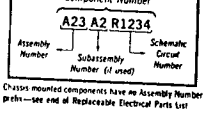


Figure 9-6. A2—Attenuator board.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

A2—ATTN, A14—CH 1 & A15—CH 2 LOGIC FIG. 9-6,-7,-8

CH1 AND CH2 ATTENUATORS DIAGRAM 1

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
AT00001	2C	1B	C85	7L	3E	R19	2H	2D	R67	5G	3D
AT2	2D	1C	C88	7M	3E	R21	3J	1E	R68	5G	3D
AT51	5C	3B				R22	3K	1E	R69	5H	4D
AT52	5D	3C	CR7	2F	2C	R23	3K	1E	R71	6J	3E
			CR18	2G	1C	R25	3K	1E	R72	6K	3E
C2	2B	1B	CR57	5F	4C	R26	3K	1D	R73	5K	3E
C3	2F	1C	CR68	5G	3C	R27	2L	2E	R75	6K	3E
C4	2C	1B				R29	3L	2E	R76	6K	3D
C5	2C	1B	J9103	2M	2E	R30	3K	2E	R77	5L	4E
C6	2E	1C	J9108	5L	4E	R30	3K	2E	R79	6L	4E
C7	2E	1C				R31	3L	2E	R80	6K	4E
C9	2F	1C	P9200	6B	3A	R33	3K	2E	R81	6L	4E
C9	3F	1D				R34	4L	2E	R83	6K	4E
C10	3F	1D	Q13	2F	2C	R35	4L	1E	R84	6L	4E
C11	2D	1B	Q15	3F	1D	R37	4L	2E	R85	7L	3E
C13	2F	2C	Q18	2G	1C	R38	4M	1E	R87	6L	4E
C17	2G	1C	Q63	5F	4C	R39	4M	1F	R88	7M	3E
C21	3J	1E	Q65	6F	3D	R41	4M	1E	R91	7K	3E
C26	3K	1D	Q68	5G	3C	R42	4M	1F	R93	7K	4F
C27	3L	2E				R43	4M	2F	R96	6G	3D
C30	3K	2E	R1	2A	2A	R46	3G	1D	R97	6G	3D
C30	3K	2E	R1	2A	2A	R47	3G	1D	R98	6G	3D
C35	4L	1E	R2	2A	2A	R48	3G	1D			
C36	4M	1E	R3	2E	1C	R51	5A	4A	S1	4A	2A
C52	5B	3B	R4	2B	2A	R51	5A	4A	S10	4K	2C
C53	5F	3C	R5	3E	1B	R52	5A	3A	S43	2F	2F
C54	5C	3B	R6	2E	2C	R53	5E	3C	S51	4A	4A
C55	5C	3B	R6	2E	2C	R54	5B	3A	S60	4C	4B
C56	5E	4C	R7	3C	1B	R55	6E	3C	S93	8L	4F
C57	5F	3C	R8	2B	2A	R56	5E	4C			
C59	6F	3D	R9	3F	1C	R57	5C	3B	U10	3E	1C
C60	6F	3D	R10	3E	1D	R58	5B	4A	U30	2L	2E
C61	5D	3B	R11	2F	1C	R59	5F	3C	U60	5E	3C
C63	5F	4C	R12	3D	1B	R60	6E	3D	U80	5L	4E
C67	5G	3C	R13	2F	2D	R61	5F	3C			
C71	5J	3E	R14	2F	1C	R62	5D	3B			
C76	6K	3D	R15	3F	1D	R63	5F	4D	W43	4M	1E
C77	6L	4E	R16	3F	1C	R64	5F	3C	W93	7K	3E
C80	6K	4E	R17	2G	1D	R65	6F	3D			
			R18	2G	1D	R66	6F	3C			

Partial A2 also shown on diagram 10.

ASSEMBLY A3

J9200	7B	3C	R89	7B	2C	R7401	6B	3C	S90	7A	2C
Q7410	6A	2D	R92	7B	3C	R7402	6A	2D			
			R951	6A	4B	R7403	6A	2D	W7457	7B	2C
			R952	6A	4D						

Partial A3 also shown on diagrams 2, 3, 4, 5, 6, 7, 9, 10 and 13.

ASSEMBLY A14

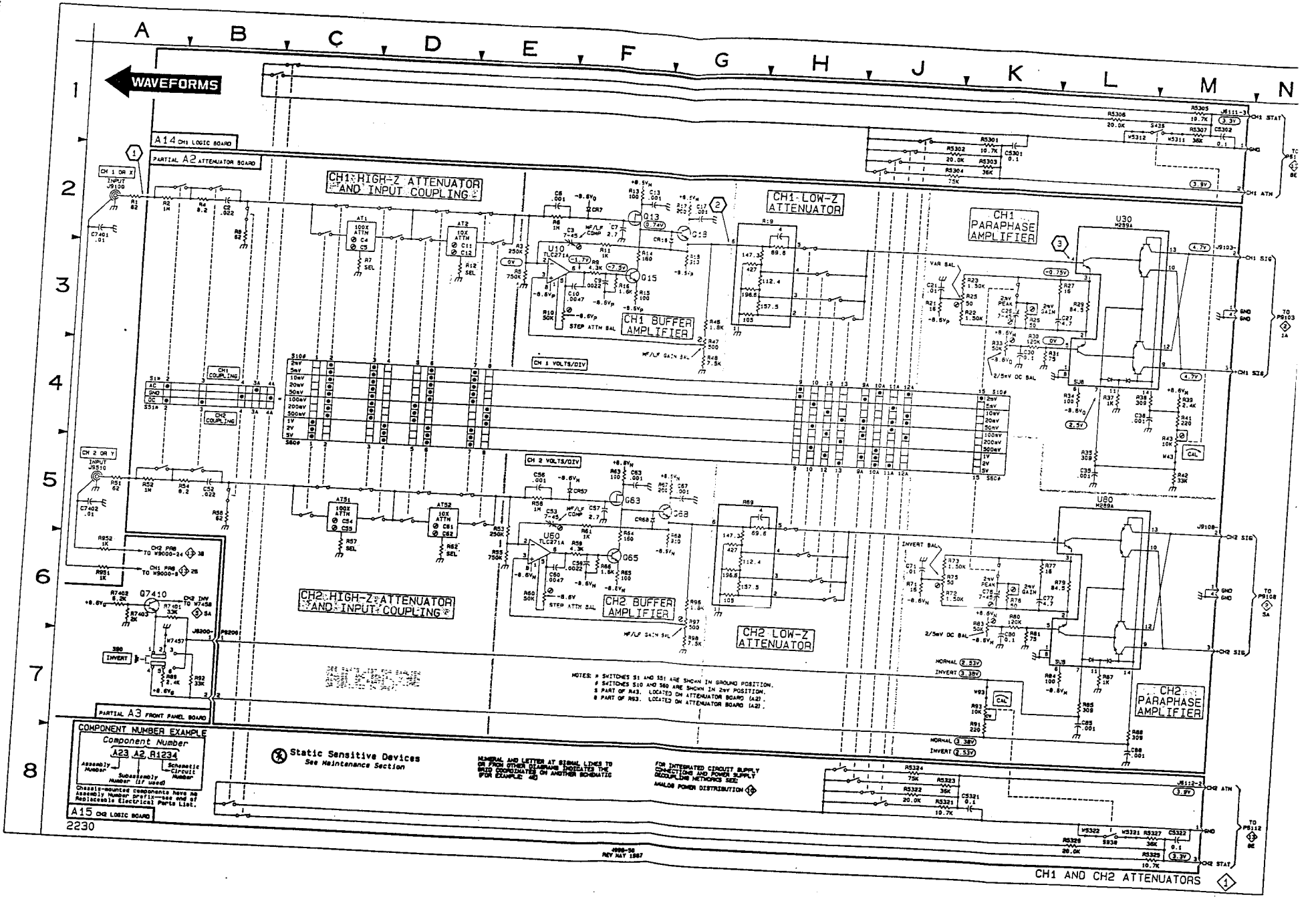
C5301	1K	1B	R5301	1K	1B	R5305	1M	1C	W5311	1M	1A
C5302	1M	1B	R5302	1J	1B	R5306	1L	1B	W5312	1L	1A
			R5303	1K	1B	R5307	1M	1B			
J6111	1M	1B	R5304	1J	1B						

ASSEMBLY A15

C5321	8K	1B	R5321	8K	1B	R5325	8M	1C	W5321	8M	1A
C5322	8M	1B	R5322	8J	1B	R5326	8L	1B	W5322	8L	1A
			R5323	8K	1B	R5327	8M	1B			
J6112	8M	1B	R5324	8J	1B						

CHASSIS MOUNTED PARTS

C7401	2A	CHASSIS	J9100	2A	CHASSIS	P9200	6B	CHASSIS			
C7402	5A	CHASSIS	J9510	5A	CHASSIS						


WAVEFORMS
A14 CH1 LOGIC BOARD
PARTIAL A2 ATTENUATOR BOARD
CH1 HIGH-Z ATTENUATOR AND INPUT COUPLING
CH1 LOW-Z ATTENUATOR
CH1 PARAPHASE AMPLIFIER
CH1 BUFFER AMPLIFIER
CH1 COUPLING
CH2 COUPLING
CH 1 VOLTS/DIV
CH 2 VOLTS/DIV
CH2 HIGH-Z ATTENUATOR AND INPUT COUPLING
CH2 BUFFER AMPLIFIER
CH2 LOW-Z ATTENUATOR
CH2 PARAPHASE AMPLIFIER
PARTIAL A3 FRONT PANEL BOARD
A15 CH2 LOGIC BOARD
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no assembly number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NOTES: # SWITCHES S1 AND S51 ARE SHOWN IN GROUND POSITION.
SWITCHES S10 AND S60 ARE SHOWN IN 2mV POSITION.
$ PART OF R43. LOCATED ON ATTENUATOR BOARD (A2).
$ PART OF R93. LOCATED ON ATTENUATOR BOARD (A2).
FOR INTEGRATED CIRCUIT SUPPLY CONNECTIONS AND POWER SUPPLY DECOUPLING NETWORKS SEE:
ANALOG POWER DISTRIBUTION
CH1 AND CH2 ATTENUATORS
2230

A1—MAIN BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C100	2										
C114	2	C528	5	C6121	5	CR957	9	Q303	4	R125	2
C115	2	C531	10	C6122	5	CR960	9	Q327	4	R126	2
C116	10	C537	10	C6123	5	CR961	9	Q328	4	R130	2
C125	2	C538	2	C6131	2	CR962	9	Q382	4	R131	2
C126	2	C539	2	C7101	6	CR963	9	Q384	4	R132	2
C130	2	C540	10	C7201	9	CR965	9	Q397	4	R133	2
C133	2	C544	4	C7203	10	CR967	9	Q413	4	R135	2
C150	2	C545	2	C7260	10	CR980	9	Q419	4	R136	2
C164	2	C547	9	C7320	7	CR981	9	Q420	4	R138	2
C165	2	C553	10	C7361	4	CR7201	9	Q421	4	R139	2
C175	2	C561	4	C7362	4	CR7202	9	Q422	4	R142	2
C176	2	C562	10	C9272	3	CR7203	9	Q423	4	R143	2
C180	2	C563	5	C9273	3	CR7301	7	Q428	4	R144	2
C200	10	C565	4			CR7302	7	Q429	4	R145	2
C201	10	C590	10	CR133	2	CR7303	7	Q473	4	R150	2
C202	3	C603	6	CR183	2	CR7304	7	Q474	4	R151	2
C210	3	C635	6	CR200	2	CR7305	7	Q487	4	R152	2
C215	10	C647	6	CR201	2	CR7306	7	Q509	5	R153	2
C220	10	C648	6	CR202	2	CR7307	7	Q511	5	R154	2
C225	3	C649	6	CR203	2	CR7308	7	Q521	5	R155	2
C226	3	C764	7	CR224	3			Q522	5	R156	2
C228	3	C770	7	CR225	3	DL9210	3	Q523	5	R158	2
C229	3	C775	7	CR226	3			Q524	4	R159	2
C237	3	C777	7	CR227	3	DS856	9	Q525	5	R164	2
C239	3	C779	7	CR228	3	DS858	9	Q527	5	R165	2
C240	3	C780	7	CR229	3	DS870	9	Q541	4	R172	2
C241	3	C782	7	CR372	4			Q542	4	R175	2
C242	3	C785	7	CR381	4	E200	10	Q543	4	R176	2
C250	3	C787	7	CR393	4	E201	10	Q544	4	R180	2
C251	3	C789	7	CR399	4	E272	10	Q576	5	R181	2
C255	10	C796	10	CR414	4	E590	10	Q578	5	R182	2
C262	3	C797	10	CR415	4	E907	8	Q583	9	R183	2
C274	10	C799	10	CR467	4			Q586	9	R185	2
C281	3	C824	9	CR476	4	J4210	5	Q756	7	R186	2
C282	3	C825	9	CR477	4	J9010	6	Q770	7	R188	2
C292	3	C828	9	CR501	5	J9010	10	Q775	7	R189	2
C312	4	C832	10	CR504	5	J9050	10	Q779	7	R192	2
C337	4	C835	9	CR505	5	J9060	10	Q780	7	R193	2
C350	4	C845	9	CR508	5	J9210	2	Q785	7	R194	2
C351	4	C847	9	CR509	5	J9210	9	Q789	7	R195	2
C363	4	C849	10	CR514	5	J9300	10	Q804	9	R200	2
C369	4	C851	9	CR527	5	J9320	4	Q814	9	R202	3
C381	4	C853	9	CR531	4	J9644	6	Q825	9	R203	3
C389	4	C854	9	CR532	4	J9802	9	Q829	9	R204	3
C390	4	C855	9	CR541	4	J9965	9	Q835	9	R206	3
C392	4	C871	9	CR551	9			Q840	9	R207	3
C396	8	C873	9	CR556	4	L142	2	Q845	9	R210	3
C397	4	C875	9	CR590	9	L143	2	Q908	8	R212	3
C400	4	C877	9	CR712	6	L192	2	Q928	8	R213	3
C414	4	C893	9	CR764	7	L193	2	Q930	8	R215	3
C415	4	C904	8	CR765	7	L960	9	Q935	8	R216	3
C418	4	C906	8	CR768	7	L961	9	Q938	8	R217	3
C419	4	C907	8	CR770	7	L962	9	Q939	8	R218	3
C420	10	C908	8	CR780	7	L968	9	Q944	8	R219	3
C421	10	C917	8	CR805	9			Q946	8	R220	10
C440	2	C919	8	CR818	9	P9070	8	Q947	8	R222	3
C453	4	C922	8	CR820	9			Q7201	9	R223	3
C454	4	C925	8	CR823	9	Q102	2	Q7202	9	R225	3
C459	4	C940	8	CR824	9	Q103	2	Q7203	9	R226	3
C460	10	C941	8	CR825	9	Q114	2	Q7204	9	R227	3
C467	4	C942	8	CR829	9	Q115	2	Q7362	4	R230	3
C469	4	C943	8	CR840	9	Q152	2	Q7420	5	R231	3
C473	4	C944	8	CR845	9	Q153	2	Q7440	5	R233	3
C480	10	C945	8	CR851	9	Q164	2	Q7470	5	R234	3
C487	4	C951	13	CR853	9	Q165	2	Q7471	5	R235	3
C494	10	C954	9	CR854	9	Q202	3	Q7472	5	R236	3
C499	10	C956	9	CR855	9	Q203	3	Q9070	8	R239	3
C500	5	C958	9	CR901	8	Q206	3			R240	3
C501	5	C959	9	CR902	8	Q207	3	R100	2	R241	3
C502	10	C960	9	CR903	8	Q230	3	R101	2	R242	3
C503	10	C961	9	CR904	8	Q231	3	R102	2	R244	3
C504	5	C962	9	CR907	8	Q254	3	R103	2	R245	3
C505	5	C963	9	CR908	8	Q255	3	R104	2	R250	3
C506	10	C964	9	CR920	8	Q256	3	R105	2	R251	3
C507	10	C965	9	CR946	8	Q257	3	R106	2	R254	3
C518	5	C968	9	CR947	8	Q282	3	R108	2	R255	3
C519	5	C970	9	CR948	8	Q283	3	R109	2	R256	3
C520	5	C975	9	CR954	9	Q284	3	R114	2	R257	3
C521	5	C976	9	CR955	9	Q285	3	R115	2	R258	3
C525	5	C979	9	CR956	9	Q302	4	R122	2	R259	3
C527	5										

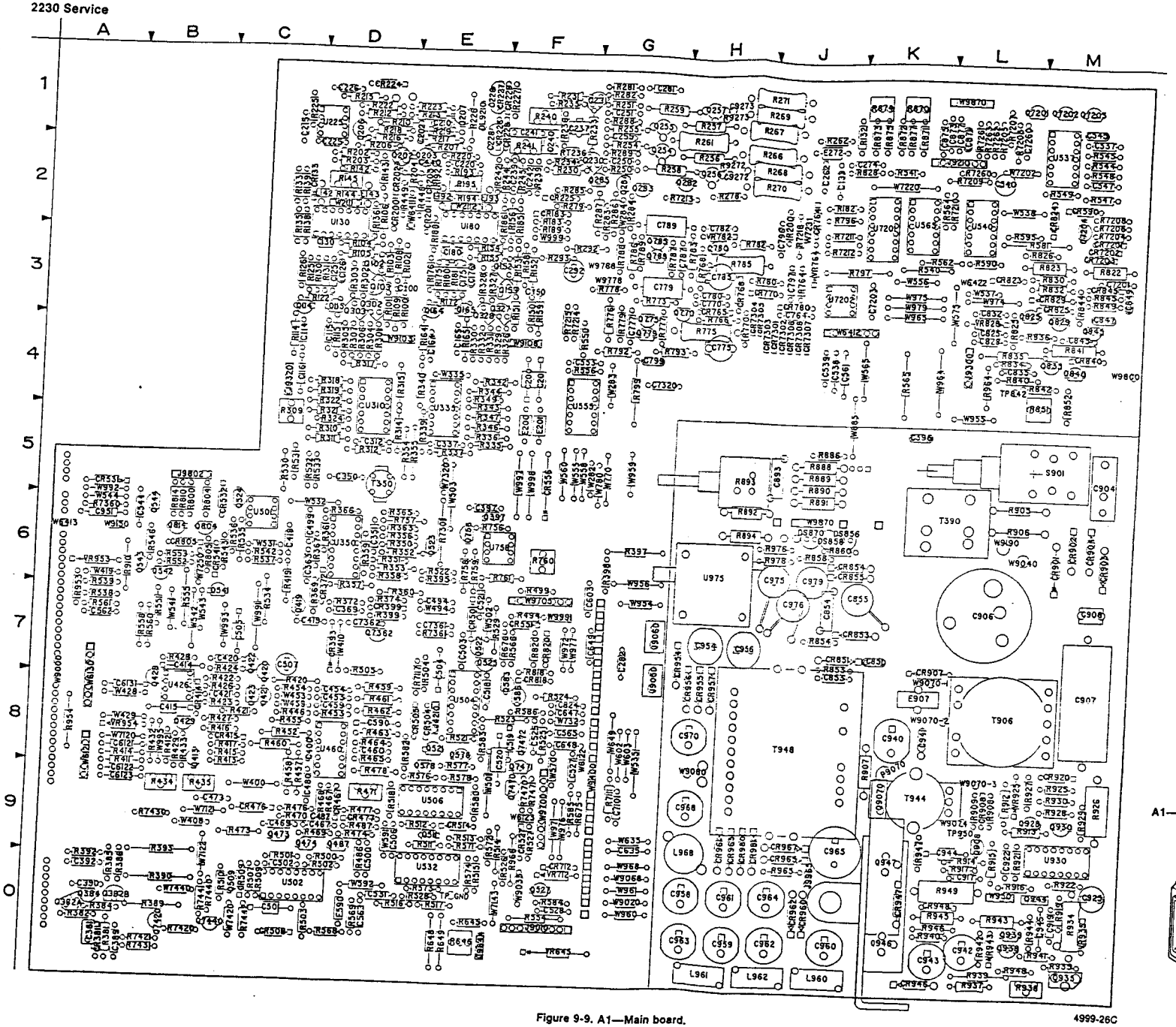
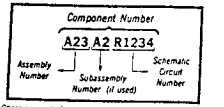


Figure 9-9. A1—Main board.

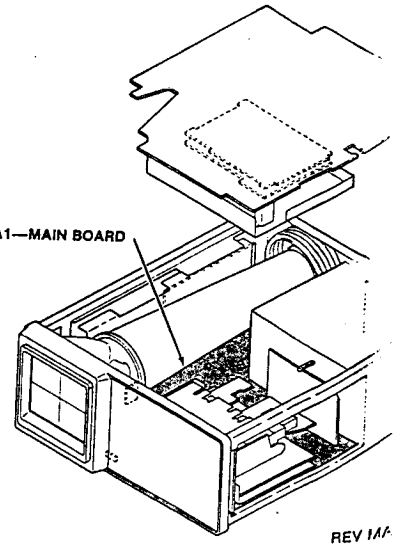
4999-26C

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

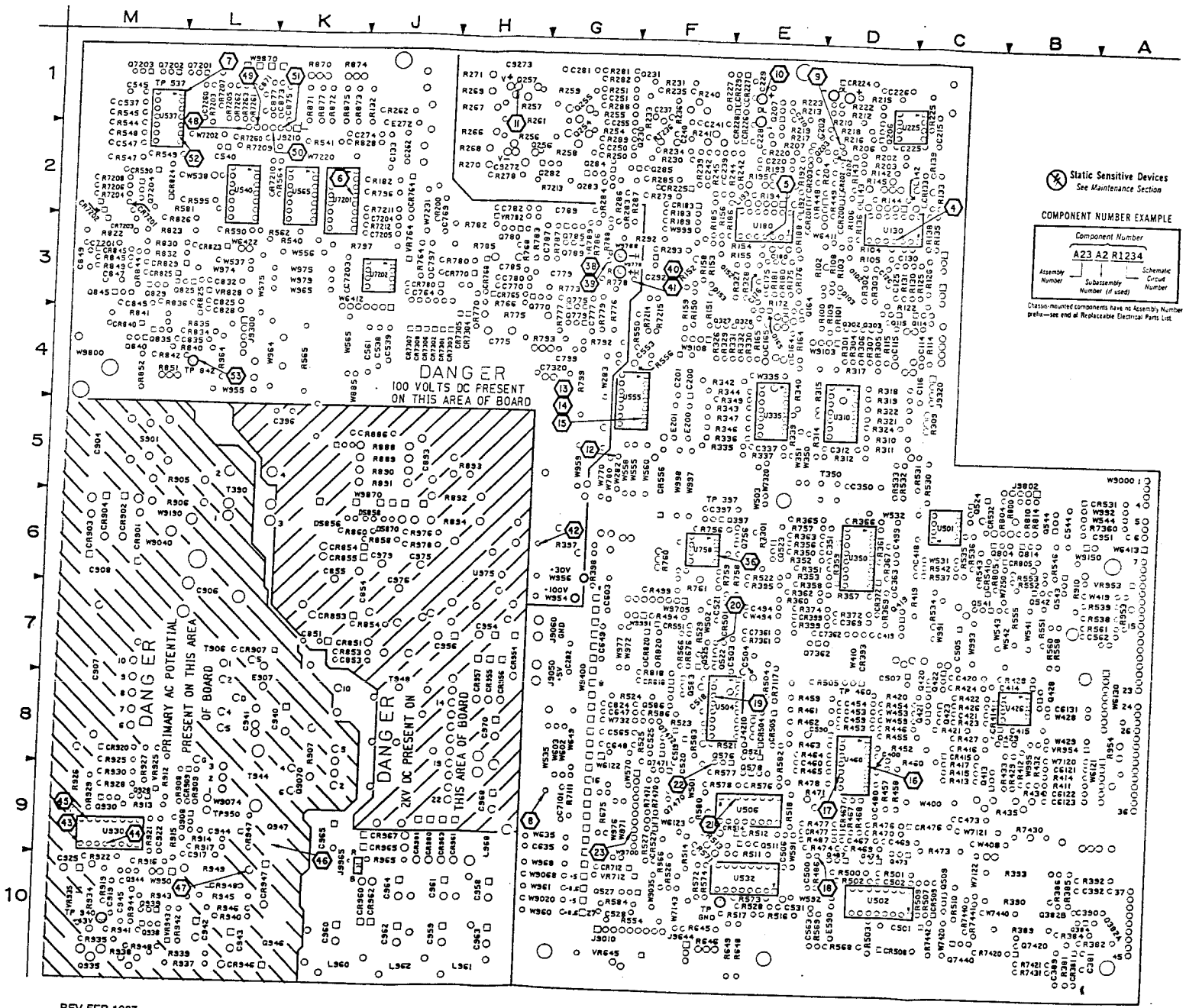


A1—MAIN BOARD (cont)

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
R261	3	R385	4	R523	5	R779	7	R935	8	U426	4
R262	3	R386	4	R524	5	R780	7	R937	8	U426	10
R266	3	R389	4	R525	5	R782	7	R938	8	U460	4
R267	3	R390	4	R526	5	R783	7	R939	8	U460	10
R268	3	R392	4	R527	5	R785	7	R940	8	U501	4
R269	3	R393	4	R528	5	R786	7	R941	8	U501	10
R270	3	R395	4	R529	5	R787	7	R942	8	U502	5
R271	3	R397	8	R530	4	R788	7	R943	8	U502	10
R278	3	R398	8	R531	4	R789	7	R944	8	U504	5
R279	3	R399	4	R532	4	R792	7	R945	8	U504	10
R281	3	R411	4	R533	4	R793	7	R946	8	U506	5
R282	3	R412	4	R534	4	R796	10	R947	8	U506	10
R283	3	R413	4	R535	4	R797	10	R948	8	U532	5
R284	3	R414	4	R536	4	R799	10	R949	8	U532	10
R285	3	R415	4	R537	4	R800	9	R953	13	U537	2
R286	3	R416	4	R538	2	R804	9	R954	13	U537	9
R287	3	R417	4	R539	2	R805	9	R964	10	U537	10
R288	3	R419	4	R540	2	R810	9	R965	9	U540	2
R289	3	R420	4	R541	2	R814	9	R966	10	U540	10
R292	3	R421	4	R542	4	R818	9	R976	9	U555	4
R293	3	R422	4	R543	4	R820	9	R978	9	U555	10
R301	4	R423	4	R544	2	R822	9	R7111	6	U565	4
R302	4	R424	4	R545	2	R823	9	R7117	5	U565	10
R303	4	R426	4	R546	4	R825	9	R7203	9	U758	7
R304	4	R427	4	R547	9	R826	9	R7204	9	U758	10
R305	4	R428	4	R548	9	R828	9	R7205	9	U930	8
R306	4	R429	4	R549	9	R830	9	R7206	9	U975	9
R307	4	R432	4	R550	4	R832	9	R7207	9	U7201	2
R309	4	R433	4	R551	4	R834	9	R7208	9	U7201	10
R310	4	R434	4	R552	4	R835	9	R7209	9	U7202	2
R311	4	R435	4	R553	4	R836	9	R7210	2	U7202	10
R312	4	R446	4	R554	6	R840	9	R7211	2		
R314	4	R448	2	R555	4	R841	9	R7212	2	VR645	6
R315	4	R449	2	R556	4	R842	9	R7213	3	VR712	6
R317	4	R452	4	R558	4	R844	9	R7214	2	VR764	7
R318	4	R453	4	R560	4	R845	9	R7215	2	VR782	7
R319	4	R454	4	R561	4	R849	9	R7216	2	VR828	9
R321	4	R455	4	R562	4	R851	9	R7260	9	VR925	8
R322	4	R457	4	R564	4	R852	9	R7261	9	VR935	8
R324	4	R458	4	R565	4	R853	9	R7262	9	VR943	8
R326	4	R459	4	R566	7	R854	9	R7263	9	VR953	13
R327	4	R460	4	R568	5	R858	9	R7301	7	VR954	13
R328	4	R461	4	R569	5	R860	9	R7360	4		
R329	4	R462	4	R571	5	R870	9	R7361	4	W282	3
R330	4	R463	4	R572	5	R871	9	R7420	5	W283	3
R331	4	R464	4	R573	5	R872	9	R7421	5	W284	3
R332	4	R465	4	R574	5	R873	9	R7430	5	W335	4
R335	4	R467	4	R576	5	R874	9	R7431	5	W400	10
R336	4	R468	4	R577	5	R875	9	R7440	5	W408	10
R337	4	R469	4	R578	5	R877	9	R7441	5	W410	4
R339	4	R470	4	R580	5	R886	9	R7442	5	W419	4
R340	4	R471	4	R581	9	R888	9	R7470	5	W428	4
R342	4	R473	4	R582	5	R889	9	R7471	5	W429	4
R343	4	R474	4	R583	9	R890	9	R9272	3	W453	4
R344	4	R476	4	R584	5	R891	9	R9273	3	W459	4
R346	4	R477	4	R585	5	R892	9			W494	10
R347	4	R478	4	R586	9	R893	9	RT236	3	W501	6
R349	4	R486	4	R590	9	R894	9			W502	5
R350	4	R487	4	R595	9	R905	8	S901	8	W503	5
R351	4	R494	10	R645	6	R906	8			W531	4
R352	4	R499	10	R646	6	R907	8	T350	4	W532	4
R353	4	R500	5	R648	6	R908	8	T390	8	W535	2
R354	4	R501	5	R649	6	R909	8	T906	8	W537	2
R355	4	R502	5	R675	6	R910	8	T944	8	W538	2
R356	4	R503	5	R676	7	R912	8	T948	9	W541	4
R357	4	R504	5	R756	7	R913	8			W542	10
R358	4	R505	5	R757	7	R914	8	TP397	4	W543	4
R359	4	R507	5	R758	7	R915	8	TP460	4	W544	10
R360	4	R509	5	R759	7	R916	8	TP537	2	W555	4
R361	4	R510	5	R760	7	R917	8	TP842	9	W556	10
R363	4	R511	5	R761	7	R919	8	TP940	8	W558	4
R365	4	R512	5	R764	7	R921	8	TP950	8	W560	4
R366	4	R513	5	R766	7	R922	8			W565	9
R367	4	R514	5	R768	7	R925	8	U130	2	W570	7
R369	4	R515	5	R770	7	R926	8	U180	2	W575	9
R372	4	R516	5	R773	7	R927	8	U225	3	W591	10
R374	4	R517	5	R775	7	R928	8	U225	10	W592	10
R381	4	R518	5	R776	7	R929	8	U310	4	W602	6
R382	4	R521	5	R777	7	R930	8	U335	4	W603	6
R384	4	R522	5	R778	7	R934	8	U350	4	W635	6

A1—MAIN BOARD (cont)

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
W649	6	W9705	10
W732	7	W9778	7
W770	7	W9788	7
W780	7	W9800	9
W885	10	W9870	9
W950	8	W9991	10
W954	10		
W955	10		
W956	10		
W959	10		
W960	10		
W961	10		
W964	10		
W965	10		
W968	10		
W971	10		
W972	10		
W974	10		
W975	10		
W976	10		
W977	10		
W979	10		
W991	10		
W992	4		
W993	10		
W995	10		
W997	10		
W998	10		
W999	10		
W2111	2		
W2112	2		
W6121	13		
W6122	13		
W6123	13		
W6130	13		
W6411	13		
W6412	13		
W6413	13		
W6422	13		
W7120	6		
W7121	4		
W7122	5		
W7143	6		
W7202	9		
W7220	2		
W7231	2		
W7250	9		
W7320	7		
W7420	5		
W7440	5		
W9000	2		
W9000	3		
W9000	4		
W9000	5		
W9000	6		
W9000	7		
W9000	9		
W9000	10		
W9000	13		
W9020	10		
W9035	10		
W9040	8		
W9068	10		
W9070	8		
W9080	9		
W9103	2		
W9108	2		
W9150	8		
W9190	8		
W9400	3		
W9400	6		
W9400	7		
W9400	9		
W9400	10		
W9700	5		
W9700	6		
W9700	7		
W9705	7		



REV FEB 1987

Figure 9-10. Circuit view of A1—Main board.

4999-27 A

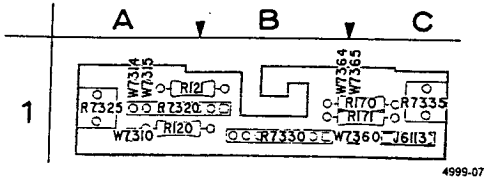
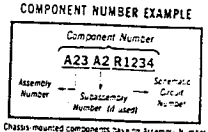


Figure 9-11. A17—Position interface board.

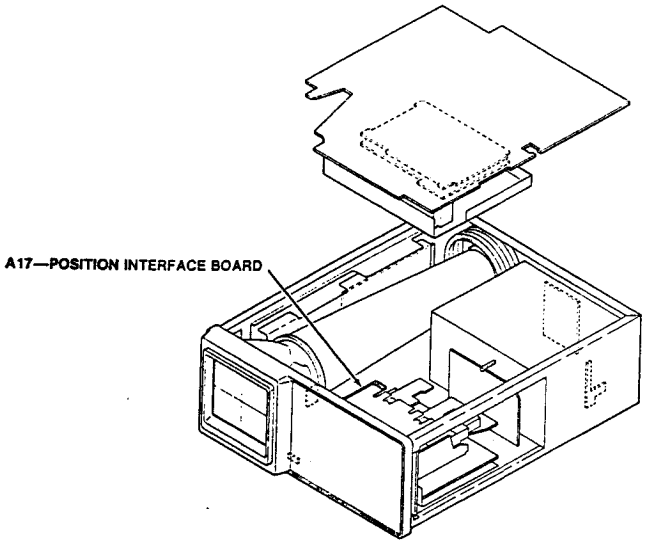
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

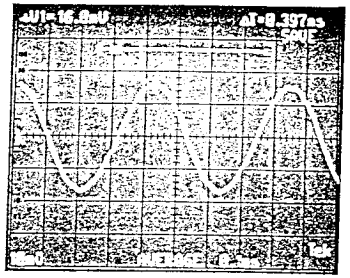


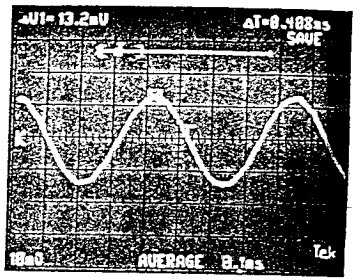
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
J6113	2	R7320	2	W7310	2
R120	2	R7325	2	W7314	2
R121	2	R7330	2	W7315	2
R170	2	R7330	2	W7360	2
R171	2	R7330	2	W7364	2
R7320	2	R7330	2	W7365	2
R7320	2	R7335	2		

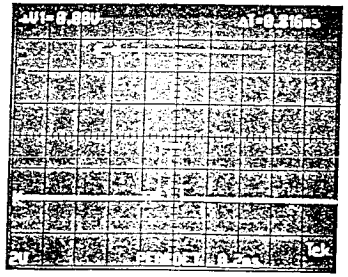


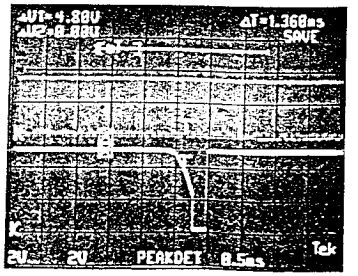
WAVEFORMS FOR DIAGRAM 2

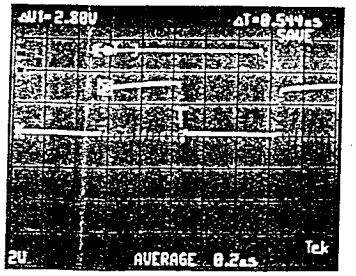




SET VERTICAL MODE SWITCH TO BOTH-CHOP.







4999-80

VERTICAL PREAMPLIFIERS AND CHANNEL SWITCHING DIAGRAM 2

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100*	1B	3D						
C114	1D	4C	R105	2C	3D	R194	5M	2E
C115	2D	4D	R106	2C	2D	R195	5M	2E
C125	2J	3D	R108	2B	3D	R200	4L	2J
C126	2J	3D	R109	2B	3D	R448	4M	2E
C130	2K	3D	R114	1E	4C	R449	3M	2D
C133	7J	2J	R115	2E	4D	R538	8F	7A
C150*	5B	3F	R122	2E	3D	R539	8F	7A
C164	5D	4E	R125	2J	3C	R540	8H	3K
C165	5D	4E	R126	1J	3C	R541	7H	2K
C175	5J	3E	R130	1K	3C	R544	7F	2M
C176	5J	3E	R131	2K	3D	R545	7F	1M
C180	5K	3E	R132	7H	1J	R7210	6G	2L
C440	3M	2E	R133	7J	2C	R7211	4H	2J
C538	8F	4J	R135	3K	2C	R7212	6H	3J
C539	8F	4J	R136	3K	2D	R7214	3K	3F
C545	7F	1M	R138	3L	2C	R7215	6K	3F
C6131	7E	8B	R139	3L	2C	R7216*	6J	2J
			R142	1M	2D			
CR133	3K	2C	R143	2M	2D	TP537	6F	1M
CR183	8K	2F	R144	1M	2D			
CR200	3L	2D	R145	2M	2D	U130	1K	3D
CR201	4L	2E	R150	5A	3F	U180	4K	3E
CR202	3M	2D	R151	6A	3F	U537A	7G	1M
CR203	4M	2E	R152	4B	3F	U537C	7F	1M
			R153	6A	3F	U537D	7F	1M
J9210	6F	2K	R154	5C	3E	U540A	8G	2L
			R155	5C	3E	U540B	7E	2L
L142	1L	2D	R156	5C	2F	U7201	7H	2J
L143	2L	2D	R158	5B	3F	U7202A	4H	3J
L192	4L	2E	R159	5B	3F	U7202B	6H	3J
L193	6L	2E	R164	5E	4E			
			R165	5E	4E	W535	7F	8G
Q102	1B	3D	R172	5E	3E	W537	7F	3L
Q103	2B	3D	R175	5J	3E	W538	7G	2L
Q114	1E	3C	R176	5J	3E	W2111	1L	2D
Q115	2E	3D	R180	5K	3E	W2112	4L	2E
Q152	5B	3F	R181	5K	3E	W7220	6G	2K
Q153	6A	3F	R182	8H	2J	W7231*	6J	2J
Q164	5E	3E	R183	8J	2F	W9000	1D	8A
Q165	5E	3E	R185	6K	2F	W9000	2D	8A
			R186	6K	2E	W9000	5D	8A
R100	1A	3D	R188	8L	3E	W9000	7D	8A
R101	2A	3D	R189	8L	2F	W9000	8D	8A
R102	1B	3D	R192	4M	2E	W9103	2A	4D
R103	2B	3D	R193	6M	2E	W9108	6A	4F
R104	1C	3D						

Partial A1 also shown on diagrams 3, 4, 5, 6, 7, 8, 9, 10 and 13.

ASSEMBLY A3

C901	7D	4C	R111	2C	1B	S545	7B	2D
			R112	2D	1B	S550	8B	2B
CR534	7B	2B	R161	5C	1C			
CR537	7C	2B	R162	5D	1D	W534	8D	3C
CR538	8C	2A						

Partial A3 also shown on diagrams 1, 3, 4, 5, 6, 7, 9, 10 and 13.

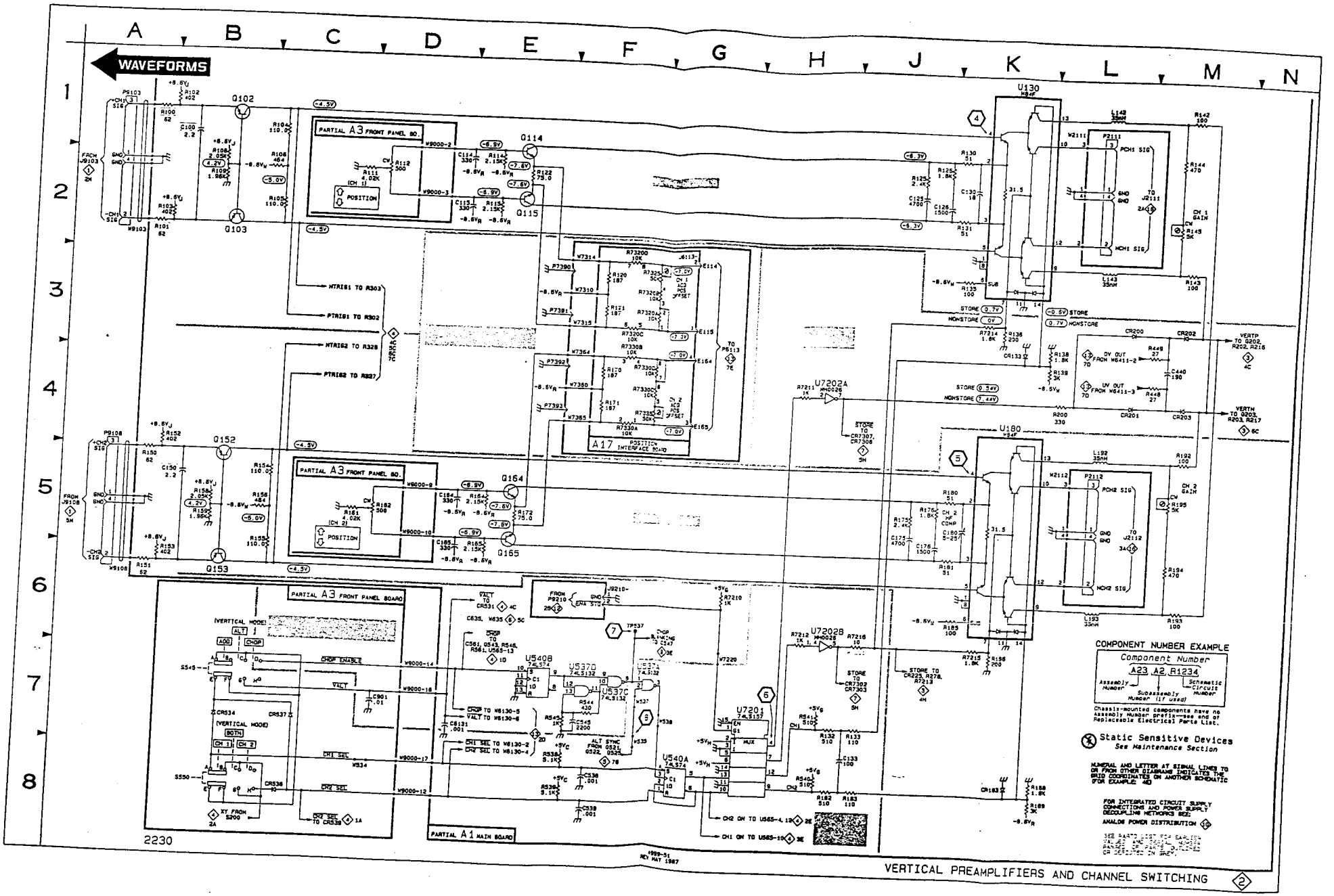
ASSEMBLY A17

J6113	2G	1C	R7320D	3F	1B	W7310	3F	1A
			R7325	3F	1A	W7314	2F	1A
R120	3F	1A	R7330A	4F	1B	W7315	3F	1A
R121	3F	1A	R7330B	3F	1B	W7360	4F	1C
R170	4F	1C	R7330C	4F	1B	W7364	3F	1B
R171	4F	1C	R7330D	4F	1B	W7365	4F	1C
R7320B	3F	1B	R7335	4F	1C			
R7320C	3F	1B						

CHASSIS MOUNTED PARTS

P7390	3F	CHASSIS	P7392	4F	CHASSIS			
P7391	3F	CHASSIS	P7393	4F	CHASSIS			

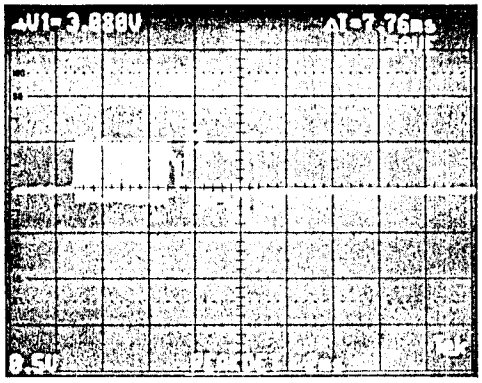
*See Parts List for serial number ranges.


WAVEFORMS
A3 FRONT PANEL BD.
A17 POSITION INTERFACE BOARD
A1 MAIN BOARD
Q102
Q103
Q114
Q115
Q152
Q153
Q164
Q165
U130
U180
U5408
U5370
U5371
U5372
U540A
U7202A
U7202B
U7203
COMPONENT NUMBER EXAMPLE
Component Number
A23, A2, R1234
Static Sensitive Devices
See Maintenance Section
2230
VERTICAL PREAMPLIFIERS AND CHANNEL SWITCHING

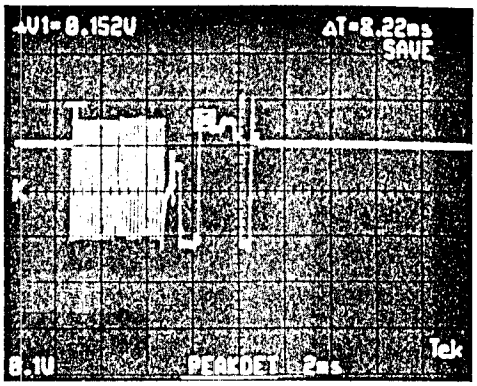
WAVEFORMS FOR DIAGRAM 3

SET THE STORE/NON STORE SWITCH TO STORE FOR WAVEFORMS 9 THROUGH 11.

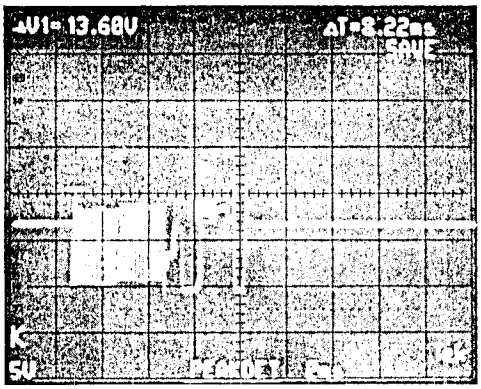
9



10

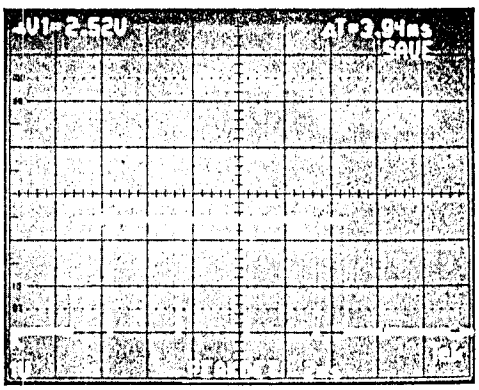


11



SET HORIZONTAL MODE SWITCH TO BOTH AND STORE/NON STORE SWITCH TO STORE.

12



VERTICAL OUTPUT AMPLIFIER DIAGRAM 3

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C202*	5D	1D	Q283	3J	2G	R258	6K	2G
C210	5D	1E	Q284	2K	2G	R259	4K	1G
C225	7D	2D	Q285	2K	2G	R261	5L	1H
C226	3F	1D				R262	5L	1J
C228	6G	2E	R202	5C	2D	R266	7K	2H
C229	5G	1E	R203	5C	2D	R267	3L	1H
C237	5J	1F	R204	5C	2D	R268	7K	2J
C239	5H	2F	R206	4C	2D	R269	3L	1J
C240	5J	1F	R207	6C	2E	R270	7K	2J
C241	5H	1F	R210	5D	1D	R271	3L	1J
C242	5H	2F	R212	5D	1D	R278	4H	2H
C250	6J	2G	R213	5D	1E	R279	3J	2F
C251	4J	1G	R215	5D	1D	R281	2F	1G
C262	5L	2J	R216	4D	2D	R282	2F	1G
C281	2F	1G	R217	6D	2E	R283	3H	2G
C282	3H	7G	R218	4D	1D	R284	2J	2G
C292	2K	3F	R219	6D	1E	R285	2K	2F
C9272	3L	2H	R222	5E	1D	R286	2K	2G
C9273	7L	1H	R223	5E	1E	R287	2K	2G
			R225	7D	1C	R288	3K	1G
CR224	4F	1D	R226	5F	1E	R289	3K	2G
CR225	4G	2F	R227	5G	1F	R292	2K	3F
CR226	5F	1E	R230	6J	2F	R293	2K	3F
CR227	5F	1E	R231	4J	1F	R7213	4H	2G
CR228	5G	1E	R233	5J	1F	R9272	7L	2H
CR229	5G	1E	R234	6J	2F	R9273	3L	1H
			R235	5J	1F			
DL9210	5E	1E	R236	5J	1F	RT236	5J	2F
			R239	5H	2F			
Q202	4C	2D	R240	5J	1F	U225	7D	1D
Q203	6C	2E	R241	5H	2F			
Q206	4D	1D	R242	5H	2E	W282	3H	5G
Q207	6D	1E	R244	5H	2F	W283	3H	4G
Q230	6J	2F	R245	5H	2F	W284	3H	2G
Q231	4J	1F	R250	6J	2G	W9000-4	2F	8A
Q254	6L	2G	R251	4J	1G	W9000-13	3F	8A
Q255	4L	1G	R254	6J	2G	W9400	3G	9G
Q265	7K	2H	R255	4J	1G			
Q257	4L	1H	R256	7K	2H			
Q282	4H	2G	R257	3K	1H			

Partial A1 also shown on diagrams 2, 4, 5, 6, 7, 8, 9, 10 and 13.

ASSEMBLY A3

R224 R280	3E 2E	2B 1C	S226	3E	2C			

Partial A3 also shown on diagrams 1, 2, 4, 5, 6, 7, 9, 10 and 13.

CHASSIS MOUNTED PARTS

P9272 P9273	7M 3M	CHASSIS CHASSIS	W9272 W9273	7M 3M	CHASSIS CHASSIS			

***See Parts List for serial number ranges.**

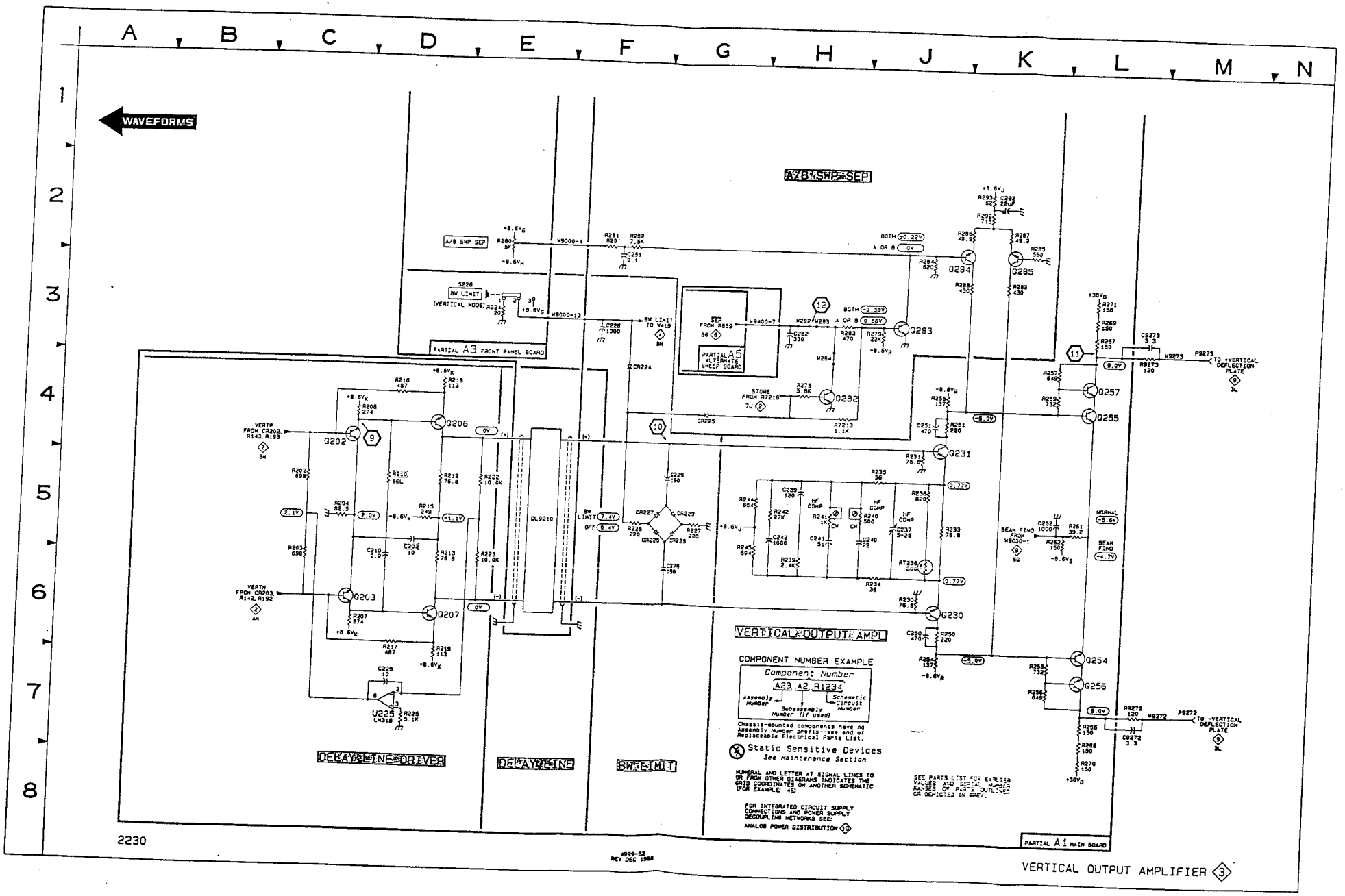


FIG. 9-9

A1—MAIN BOARD

A17—POSITION INTERFACE

WAVEFORMS FOR DIAGRAM 3

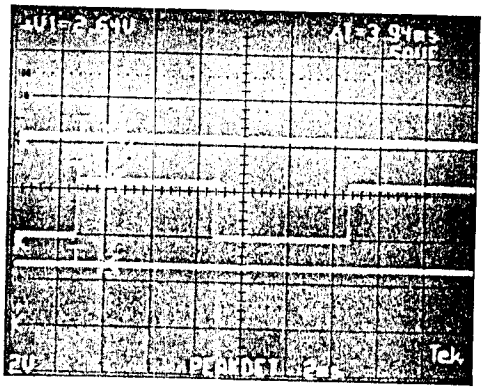
A2—ATTN. A14—CH 1 &

WAVEFORMS FOR DIAGRAM 4

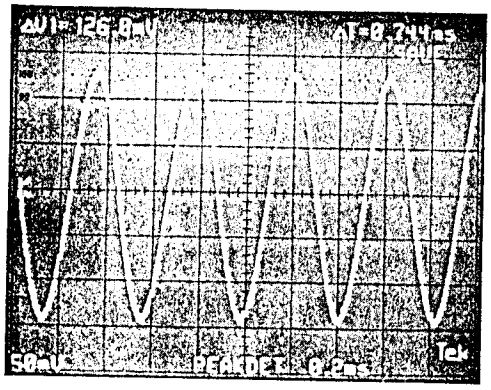
SET A&B INT SWITCH TO CH 1. (13)

SET VERTICAL MODE SWITCH TO BOTH-ALT. (14)

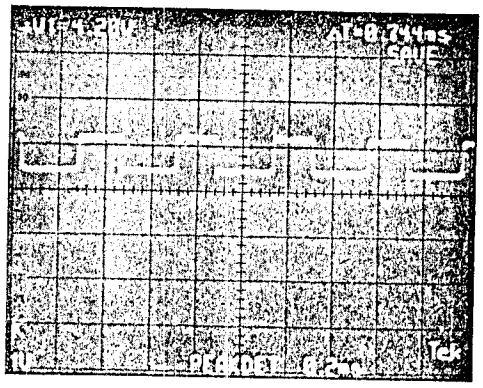
SET VERTICAL MODE SWITCH TO CH 2 AND A&B INT SWITCH TO CH 2. (15)



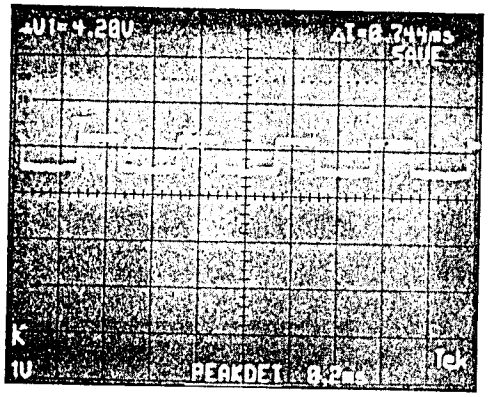
(16)



(17)

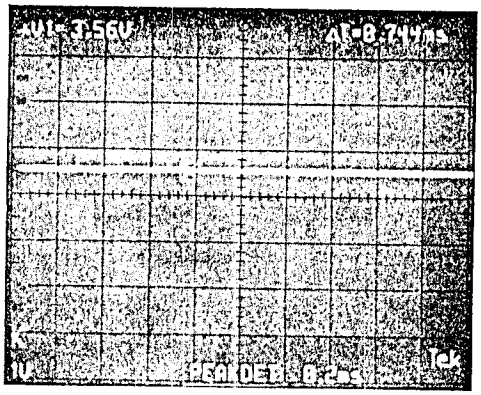


(18)



SET HORIZONTAL MODE SWITCH TO B AND A TRIGGER SWITCH TO SGL SWP.

(18)



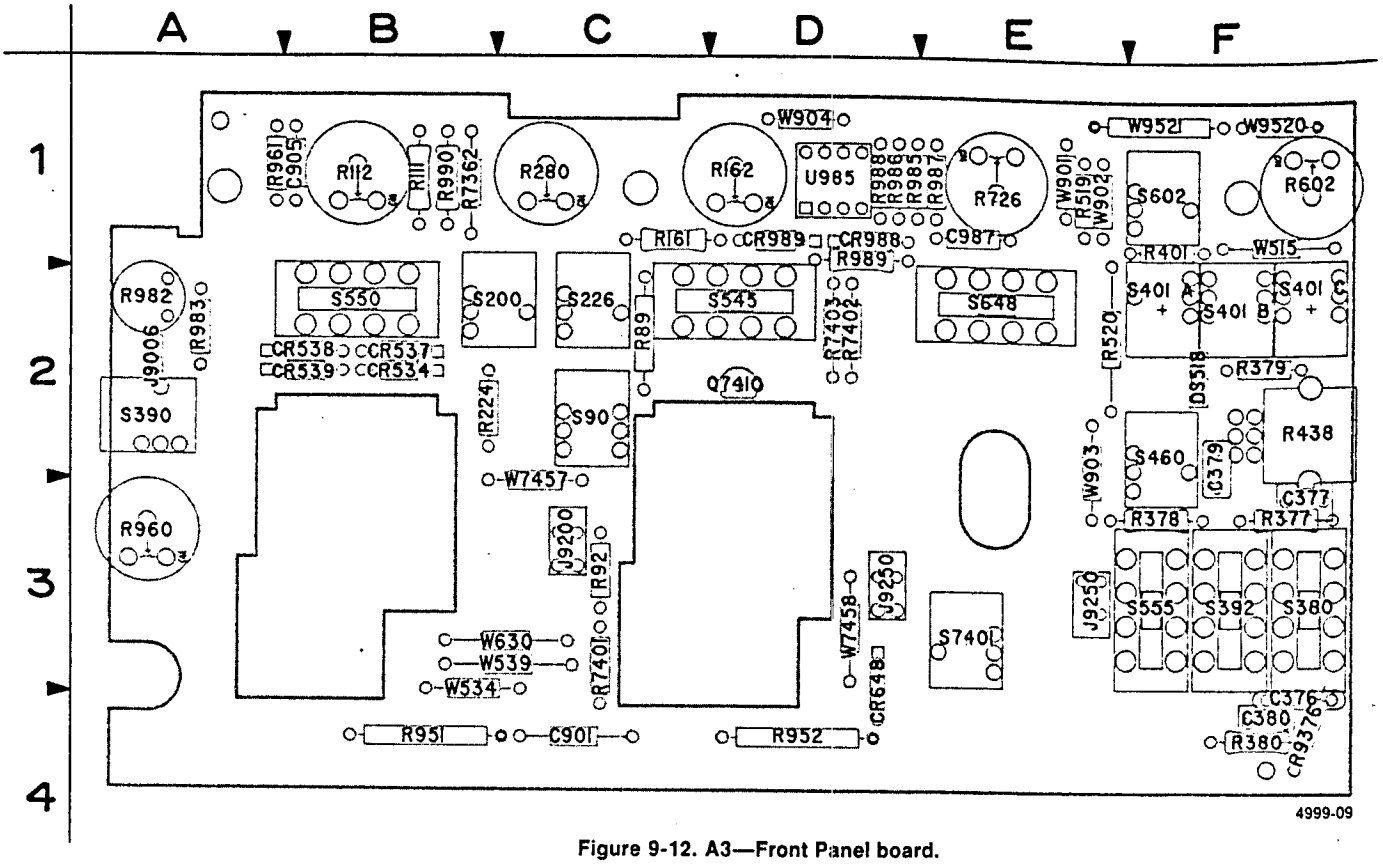
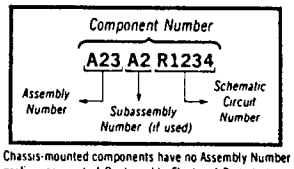


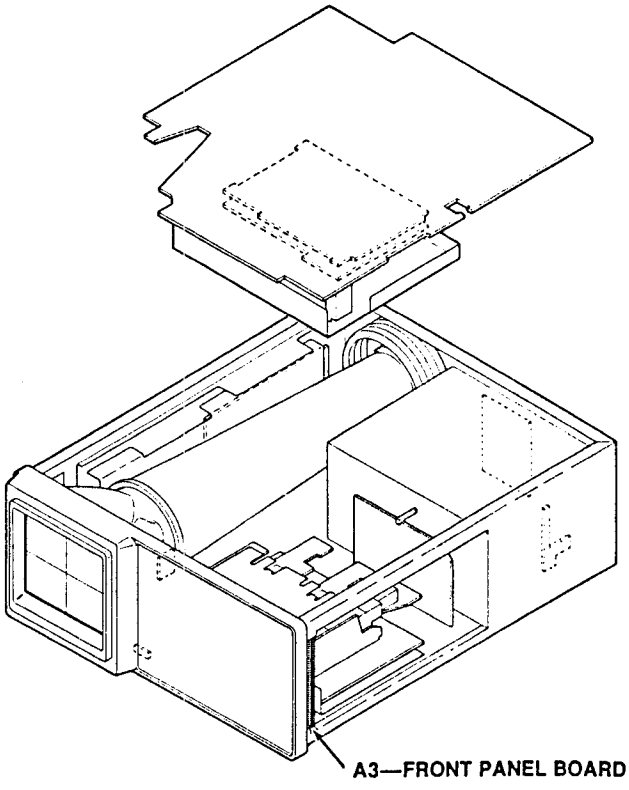
Figure 9-12. A3—Front Panel board.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List



A3—FRONT PANEL BOARD

A3—FRONT PANEL BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C376	4	R377	4	S380	4
C377	4	R378	4	S390	9
C379	4	R379	4	S392	4
C380	4	R380	4	S401	5
C901	2	R401	5	S401	5
C905	10	R438	4	S401	5
C987	7	R519	5	S438	4
CR534	2	R520	5	S460	4
CR537	2	R602	6	S545	2
CR538	2	R726	7	S550	2
CR539	4	R951	1	S555	4
CR648	4	R952	1	S602	6
CR988	7	R960	13	S648	6
CR989	7	R961	13	S7401	5
DS518	5	R982	9	U985	7
J9006	9	R983	9	U985	10
J9200	1	R985	7	W515	5
J9250	4	R986	7	W534	2
J9250	5	R987	7	W539	4
J9250	7	R988	7	W630	4
J9900	7	R989	7	W901	6
Q7410	1	R990	7	W902	5
R89	1	R7362	4	W903	5
R92	1	R7401	1	W904	6
R111	2	R7402	1	W7457	1
R112	2	R7403	1	W7458	5
R161	2	R9376	4	W9520	5
R162	2	S90	1	W9521	5
R224	3	S200	4	W9900	7
R280	3	S226	3		

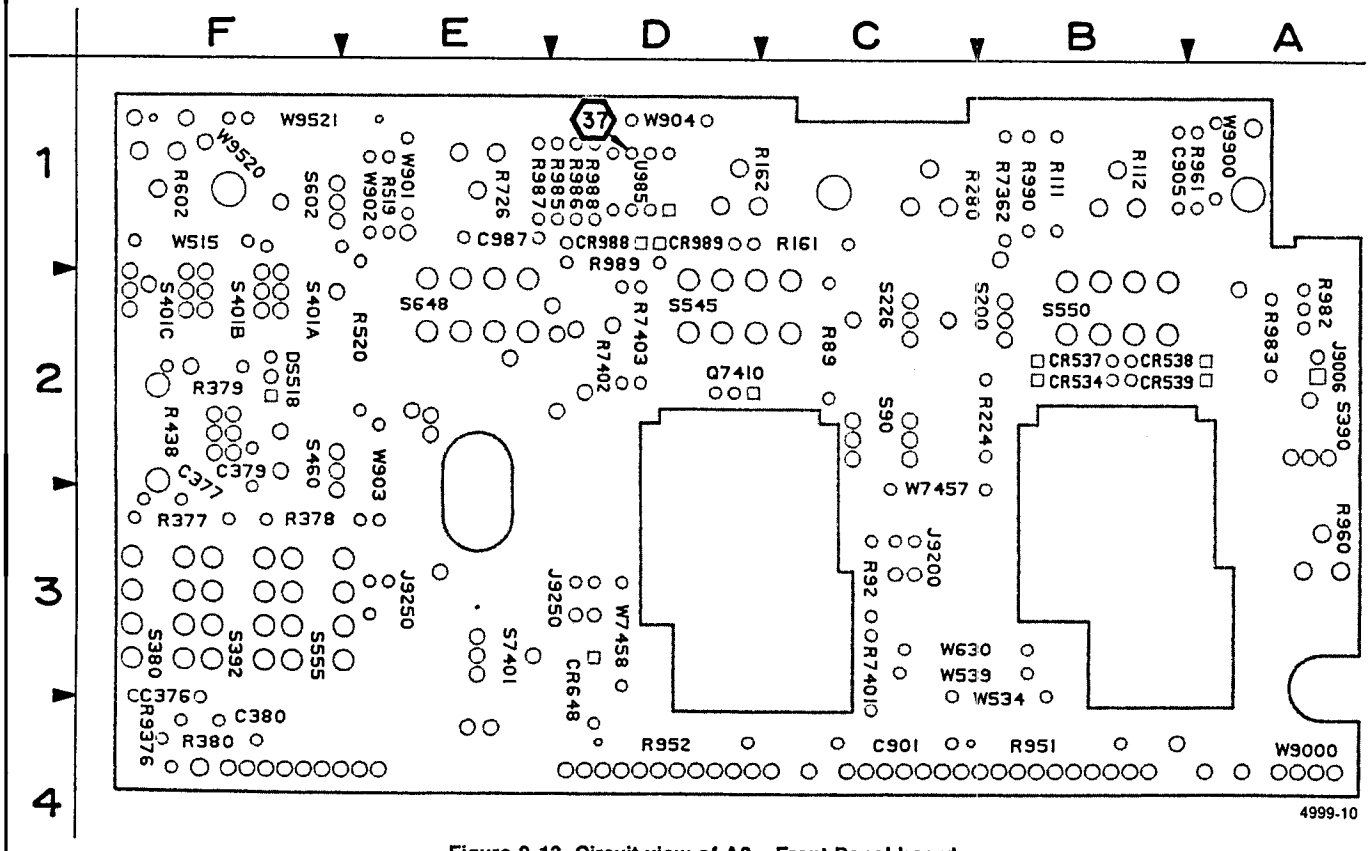


Figure 9-13. Circuit view of A3—Front Panel board.

TRIGGERING DIAGRAM 4

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C312	4E	5D
C337	7E	5E
C350	4F	5D
C351*	4G	6D
C363*	4H	6D
C369	5H	7D
C381	6G	10A
C389	6G	10B
C390	5H	10A
C392	7H	10A
C397	7G	6E
C400	5K	8D
C414	1L	7B
C415	3L	8B
C418	8J	6C
C419	8J	7D
C453	4L	8D
C454	4M	8D
C459	5L	8D
C467	7L	9D
C469	7M	9C
C473	6M	9C
C487*	7M	9D
C544	1D	6B
C561	2D	4J
C565	2F	8F
C7361	8H	7E
C7362	8J	7D
CR372	4J	6D
CR381	6G	10A
CR393	6J	7D
CR399	7J	7D
CR414	1K	8B
CR415	3K	8C
CR467	6L	9D
CR476	6M	9C
CR477	6M	9D
CR531	4C	5A
CR532	3C	6C
CR541	3C	6C
CR556	1E	5F
J9320	2H	4C
Q302	5D	3D
Q303	4D	3D
Q327	7D	3E
Q328	6D	3E
Q382A	6H	10A
Q382B	6H	10B
Q384	6H	10A
Q397	7H	6F
Q413	3K	8B
Q419	8J	7C
Q420	1L	7C
Q421	3L	8C
Q422	1L	7C
Q423	4L	8C
Q428	2M	8B
Q429	3M	8B
Q473	7M	9C
Q474	7M	9D
Q487	8N	9D
Q524	3G	6C
Q541	3D	7C
Q542	2C	6B
Q543	2D	6B
Q544	2D	6B
Q7362	8J	7D
R301	4C	4D
R302	5C	3D
R303	4C	3D
R304	5D	4D
R305	4D	4D
R306	5D	4D
R307	4D	4D
R309	4D	5C
R310	5D	5D
R311	4D	5D
R312	4E	5D
R314	5E	5D
R315	4E	4D
R317	3F	4D
R318	4F	4D
R319	5F	4D
R321	5F	5D
R322	5F	4D
R324	5E	5D
R326	6C	4F
R327	7C	3E
R328	6C	3E
R329	7D	4E
R330	6D	4E
R331	7D	4E
R332	6D	4E
R335	7D	5E
R336	6D	5E
R337	7E	5E
R339	7F	5E
R340	6F	4E
R342	2F	4F
R343	6F	4E
R344	7F	4E
R346	7F	5E
R347	8F	5E
R349	7E	4E
R350	4G	6E
R351	5G	6D
R352	4G	6E
R353	5G	6D
R354	4F	5E
R355	5F	5E
R356	4G	6E
R357	5G	7D
R358	4G	6D
R359	4H	6D
R360	5H	7E
R361	4G	6D
R363	4H	6E
R365	3J	6E
R366	4H	6D
R367	4H	6D
R369	5J	7D
R372	4J	7D
R374	4J	7D
R381	6G	10A
R382	6G	10A
R384	6G	10A
R385	6H	10A
R386	6H	10B
R389	6G	10B
R390	5G	10B
R392	7H	10A
R393	6H	10B
R395	7H	6E
R399	7H	7D
R411	3J	9B
R412	3J	8B
R413	3K	9C
R414	1K	8B
R415	3K	8C
R416	1K	8C
R417	3K	8C
R419	8J	6C
R420	4K	8C
R421	4L	8C
R422	1L	8C
R423	3L	8C
R424	1L	7C
R426	1L	8C
R427	3L	8C
R428	1M	7B
R429	3M	8B
R432	2M	8B
R433	3M	8B
R434	2M	9B
R435	2M	9B
R446	4L	8C
R452	6K	8C
R453	4L	8D
R454	4M	8C
R455	8J	8C
R457	5K	9D
R458	5K	9C
R459	4L	8D
R460	5K	8C
R461	4K	8D
R462	5K	8D
R463	7K	8D
R464	7L	8D
R465	6L	8D
R467	6L	9D
R468	7L	9D
R469	6L	9D
R470	7L	9D
R471	7K	9D
R473	7M	9C
R474	8M	9D
R476	6M	9D
R477	6M	9D
R478	7K	9D
R486	6M	10D
R487	7N	9D
R530	2H	5C
R531	3H	5C
R532	3F	5C
R533	2F	5D
R534	2H	7C
R535	3G	6C
R536	3G	6C
R537	3G	6C
R542	4G	6C
R543	3D	6C
R546	3D	6B
R550	2D	4F
R551	2C	7B
R552	2C	6B
R553	2C	6B
R555	1E	7B
R556	3C	4F
R558	2D	7B
R560	3C	7B
R561	2D	7A
R562	2E	3K
R564	2F	2K
R565	2F	4K
R7360	8H	6A
R7361	8H	7E
T350	4G	5D
TP397	7G	5E
TP460	6K	8D
U310	4E	5D
U335	6E	5E
U350A	4H	6D
U350B	4H	6D
U350C	5H	6D
U350D	5G	6D
U350E	4G	6D
U426A	1L	8B
U426B	3L	8B
U460	5K	8D
U501A	3H	6C
U501B	2H	6C
U555A	3C	4F
U555B	3E	4F
U555C	2E	4F
U555D	3E	4F
U565A	1E	2K
U565B	2E	2K
U565C	3E	2K
U565D	2E	2K
W335	6E	4E
W410	6J	7D
W419	8H	6A
W428	1M	8B
W429	3M	8B
W453	4L	8C
W459	5L	8C
W531	3G	6C
W532	2C	6D
W541	3C	7B
W543	3D	7B
W555	3C	5F
W558	2D	5G
W560	3D	5F
W992	1C	6A
W7121	6M	9C
W9000	1B	8A
W9000	1M	8A
W9000	2B	8A
W9000	3B	8A
W9000	3M	8A
W9000	4M	8A
W9000	5B	8A
W9000	5M	8A
W9000	8A	
W9000	8A	

Partial A1 also shown on diagrams 2, 3, 5, 6, 7, 8, 9, 10 and 13.

ASSEMBLY A3

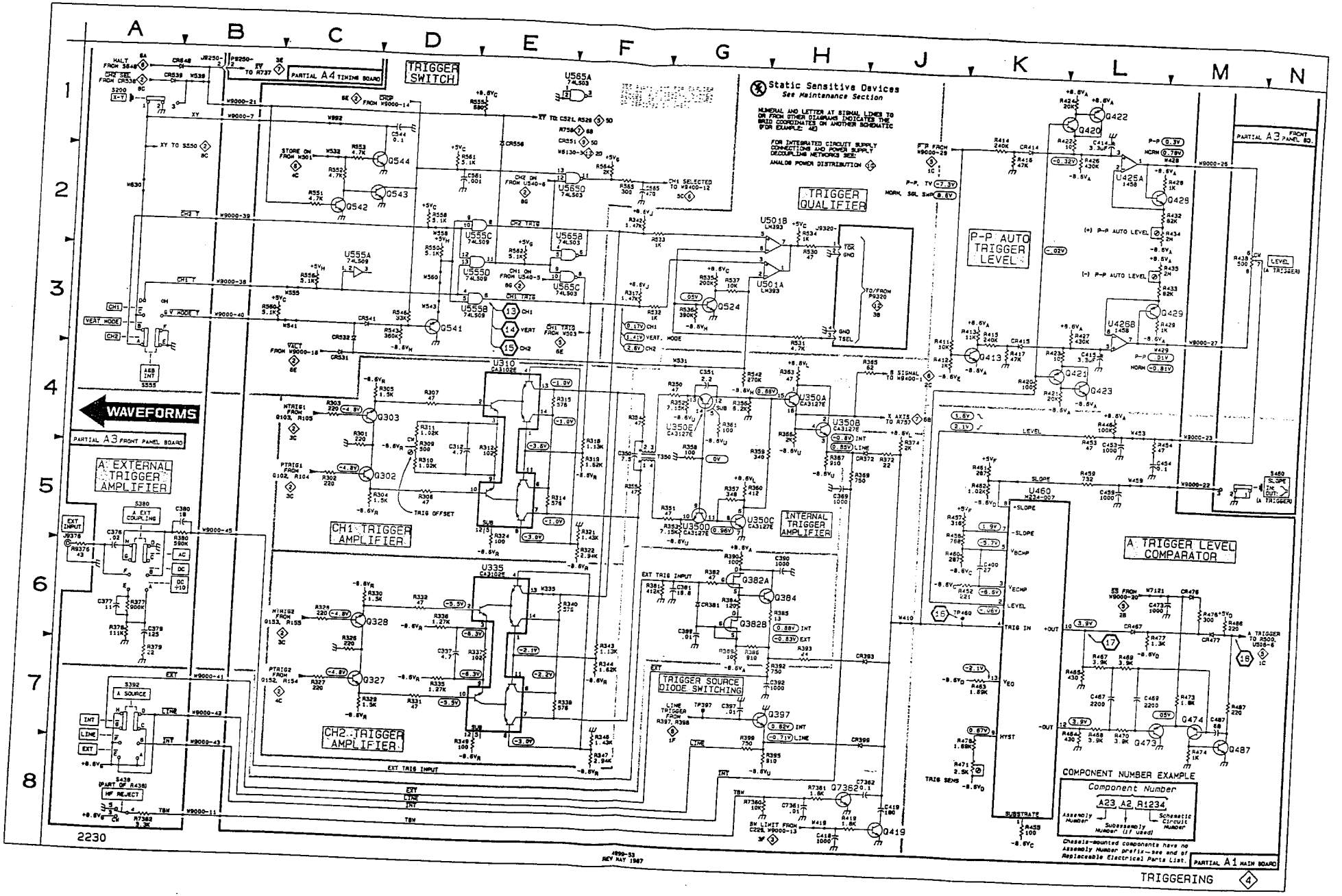
C376	6A	4F	J9250	1B	3D	R7362	8B	1C	S460	4N	2F
C377	6A	3F							S555	4A	3F
C379	6A	2F	R377	6A	2F						
C380	5B	4F	R378	6A	2F	S200	1A	2C	W539	1B	3C
CR539	1A	2A	R379	7A	2F	S380	5A	3F	W630	2A	3C
CR648	1A	3D	R380	5B	3F	S392	7A	3F			
			R438	2M	2F	S438	8A	2F			

Partial A3 also shown on diagrams 1, 2, 3, 5, 6, 7, 9, 10 and 13.

CHASSIS MOUNTED PARTS

J9376	6A	CHASSIS	P9250	1B	CHASSIS	R9376	6A	CHASSIS			

*See Par
serial nur



Is List for
nber ranges.

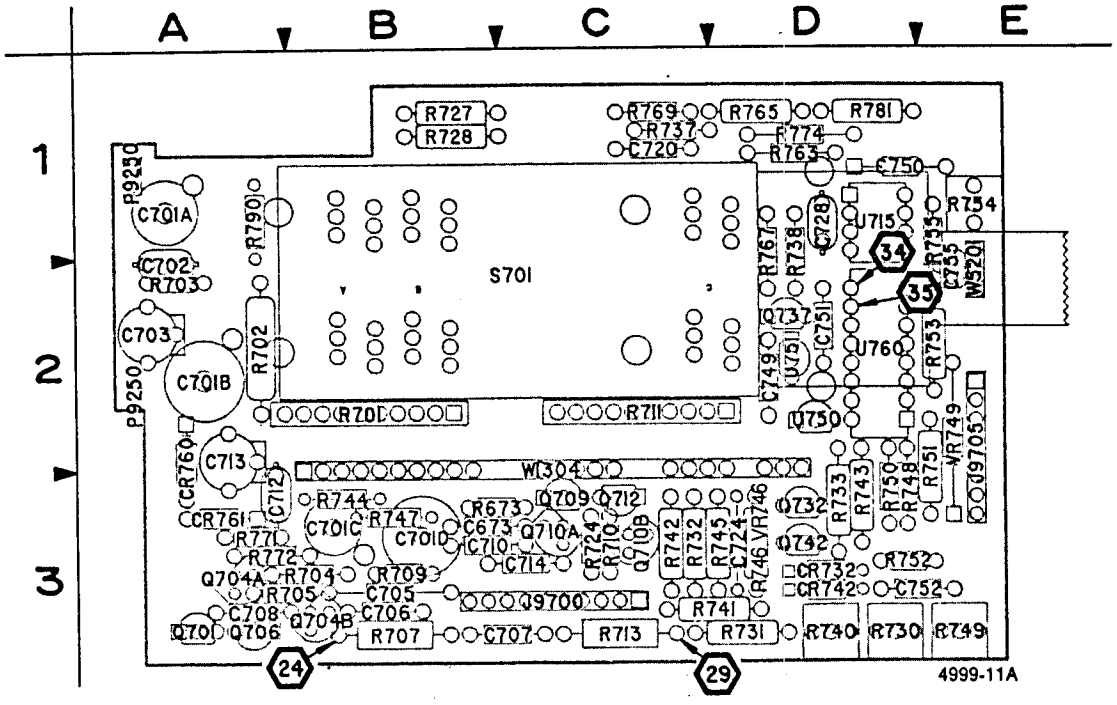
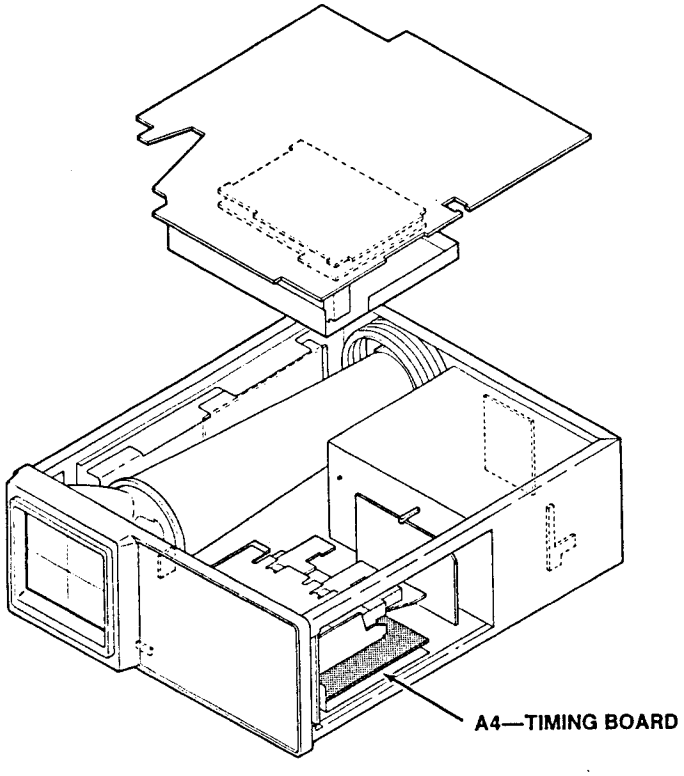


Figure 9-14. A4—Timing board.



A4—TIMING BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C673	6	Q706	5	R749	7
C701	5	Q709	6	R750	7
C701	6	Q710	6	R751	7
C702	5	Q712	6	R752	10
C703	5	Q732	7	R753	7
C705	10	Q737	7	R754	7
C706	10	Q742	7	R755	7
C707	10	R673	6	R763	6
C708	5	R701	5	R765	6
C710	10	R702	5	R767	6
C712	6	R703	5	R769	6
C713	6	R704	6	R771	6
C714	6	R705	5	R772	6
C720	7	R707	5	R774	6
C724	10	R709	6	R781	6
C728	7	R710	6	R790	5
C749	10	R711	6	S701	5
C750	10	R713	6	S701	6
C751	7	R724	10	U715	6
C752	10	R727	7	U715	6
C755	7	R728	7	U715	10
CR732	7	R730	7	U750	10
CR742	7	R731	7	U751	10
CR760	6	R732	7	U760	7
CR761	6	R733	7	U760	10
J9700	5	R737	7	VR746	7
J9700	6	R738	7	VR749	10
J9700	7	R740	7	W1304	6
J9705	7	R741	7	W1304	6
J9705	10	R742	7	W1304	6
P9250	5	R743	7	W1304	10
Q701	5	R744	6	W1304	10
Q704	5	R745	7	W5201	7
		R746	7		
		R747	6		
		R748	7		

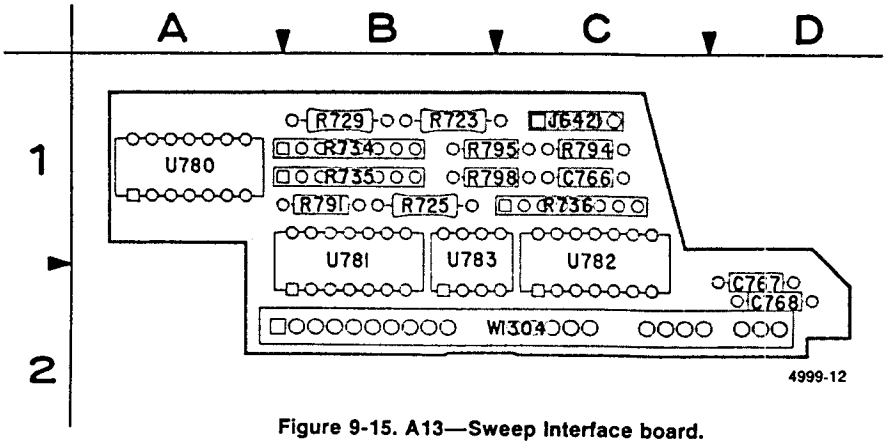
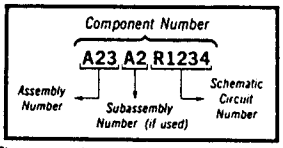


Figure 9-15. A13—Sweep Interface board.

A13—SWEEP INTERFACE BOARD

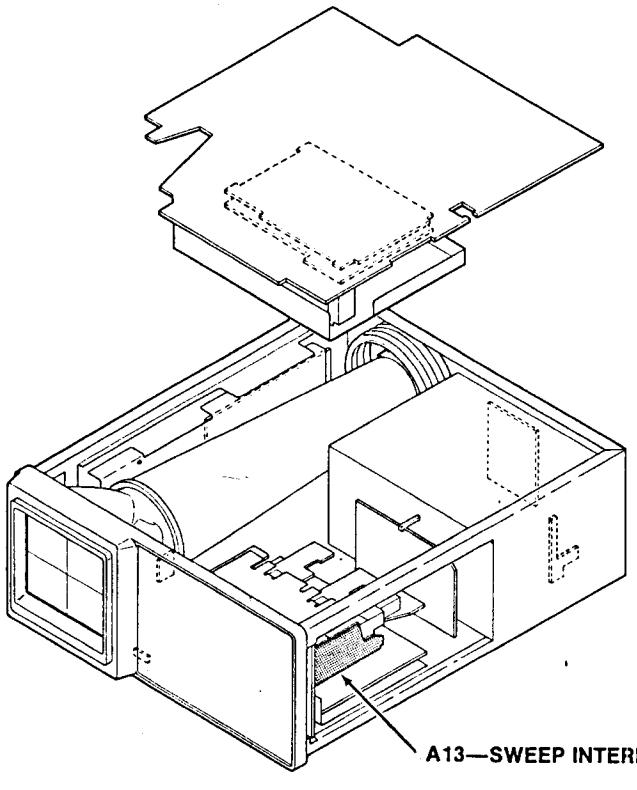
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



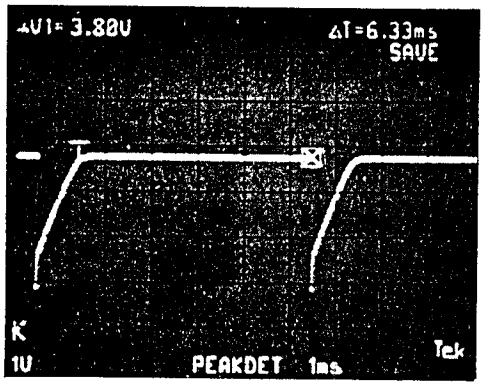
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C766	5	R735	5	U781	5
C767	10	R736	6	U781	10
C768	10	R791	5	U782	6
J6421	6	R794	5	U782	10
R723	6	R795	5	U783	6
R725	6	R798	5	U783	10
R729	6	U780	5	W1304	5
R734	5	U780	10	W1304	6
				W1304	10

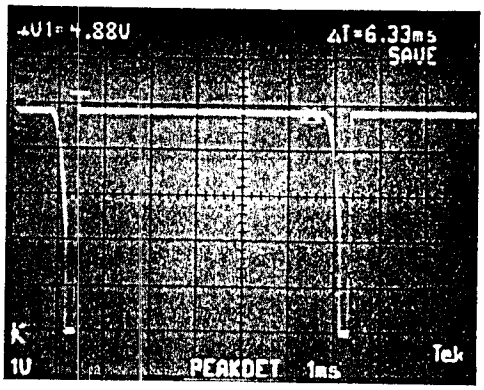


WAVEFORMS FOR DIAGRAM 5

19

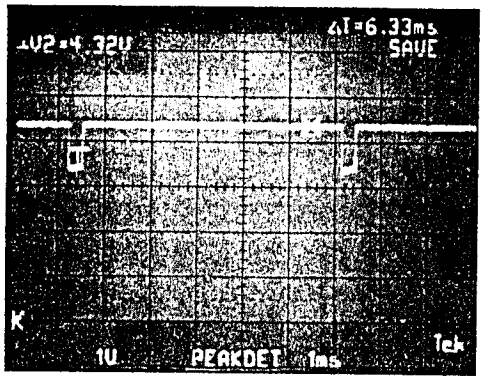


20

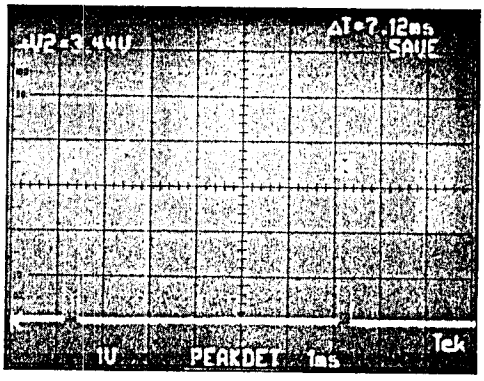


TEST SCOPE TRIGGERED ON U506 PIN 3
FOR WAVEFORMS 21 THROUGH 24.

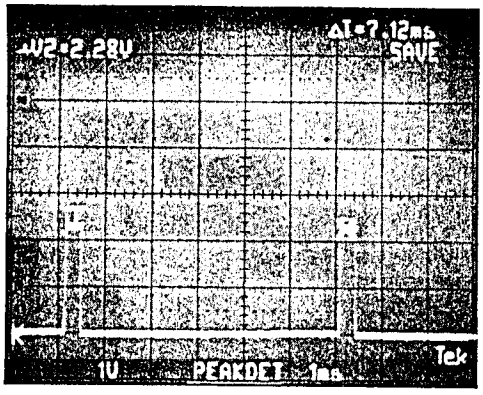
21



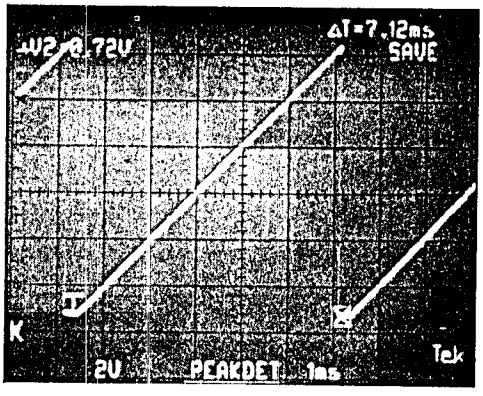
22



23



24



A SWEEP GENERATOR AND LOGIC DIAGRAM 5

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C500	1D	10D	Q7470	8D	9F	R577	1K	8E
C501	3C	10C	Q7471	8D	8F	R578	1K	9E
C504	3C	7E	Q7472	8E	8F	R580	2K	9E
C505	3B	7C				R582	1K	8E
C518	7E	8F	R500	1C	10D	R584	2L	10F
C519	7C	8F	R501	2C	10C	R585	2L	9G
C520	7C	8F	R502	2C	10D	R7117	2K	7E
C521	6D	7E	R503	3C	10D	R7420	4E	10B
C525	6F	8F	R504	3C	7E	R7421	4E	10B
C527	2L	8G	R505	3B	7D	R7430	4C	9B
C528	2K	10F	R507	2D	10C	R7431	5C	10B
C563*	1D	10D	R509	3D	10C	R7440	4D	10C
C6121	5E	8B	R510	2D	10C	R7441	4D	10C
C6122	5E	9B	R511	2H	9E	R7442	4D	10C
C6123	4E	9B	R512	2H	9E	R7470	8D	9F
			R513	2H	9E	R7471	8D	9F
CR501	6D	7E	R514	1J	9F			
CR504	3D	8E	R515	2G	10F	U502	2D	10C
CR505	2K	8E	R516	2J	10E	U504A	3D	8E
CR508	1C	10C	R517	2J	10E	U504B	7E	8E
CR509	2D	10C	R518	3D	9E	U506	1H	9E
CR514	2J	9E	R521	7F	8E	U532A	1J	10E
CR527	2K	9F	R522	6E	6E	U532B	1G	10E
			R523	7F	8F	U532C	1G	10E
J4210	1L	8E	R524	7F	8F	U532D	1D	10E
			R525	6F	8F			
Q509	3D	10C	R526	2F	10F	W502	6E	7F
Q511	2J	9E	R527	2K	9F	W503	6E	5E
Q521	7F	8E	R528	1F	10E	W7122	1C	10C
Q522	5E	7E	R529	5E	7F	W7420	4E	10C
Q523	6E	6E	R568	1D	10D	W7440	4D	10B
Q525	7F	7E	R569	1D	10D	W9000	1B	8A
Q527	2L	10F	R571	1E	9E	W9000	2B	8A
Q576	1K	8E	R572	1G	9F	W9000	2E	8A
Q578	1K	8E	R573	1J	10E	W9000	3B	8A
Q7420	4E	10B	R574	2G	10E	W9000	5B	8A
Q7440	4D	10C	R576	1K	9E	W9700	8C	9F

Partial A1 also shown on diagrams 2, 3, 4, 6, 7, 8, 9, 10 and 13.

ASSEMBLY A3

DS518	3F	2F	S401A	3A	2F	W903	7B	2E
			S401B	1A	2F	W7458	5B	3D
J9250	7B	3D	S401C	2A	2F	W9520	7A	1F
			S7401	5A	3E	W9521	7A	1F
R401	2A	1F						
R519	7A	1E	W515	2A	1F			
R520	7A	2E	W902	7A	1E			

Partial A3 also shown on diagrams 1, 2, 3, 4, 6, 7, 9, 10 and 13.

ASSEMBLY A4

C701A	3L	1A	Q701	3M	3A	R707	3N	3B
C701B	3L	2A	Q704A	4M	3A	R790	4L	1A
C702	3L	2A	*Q704B	4M	3B			
C703	3L	2A	Q706	4N	3A	S701A	3K	1A
C708	4M	3A				S701B	4K	1A
			R701	3H	2A	S701B	8C	1A
J9700	7C	3C	R702	3H	2A			
			R703	3L	2A			
P9250	7B	1A	R705	4M	3B			

Partial A4 also shown on diagrams 6, 7 and 10.

***See Parts List for serial number ranges.**

A SWEEP GENERATOR AND LOGIC DIAGRAM 5 (CONT)

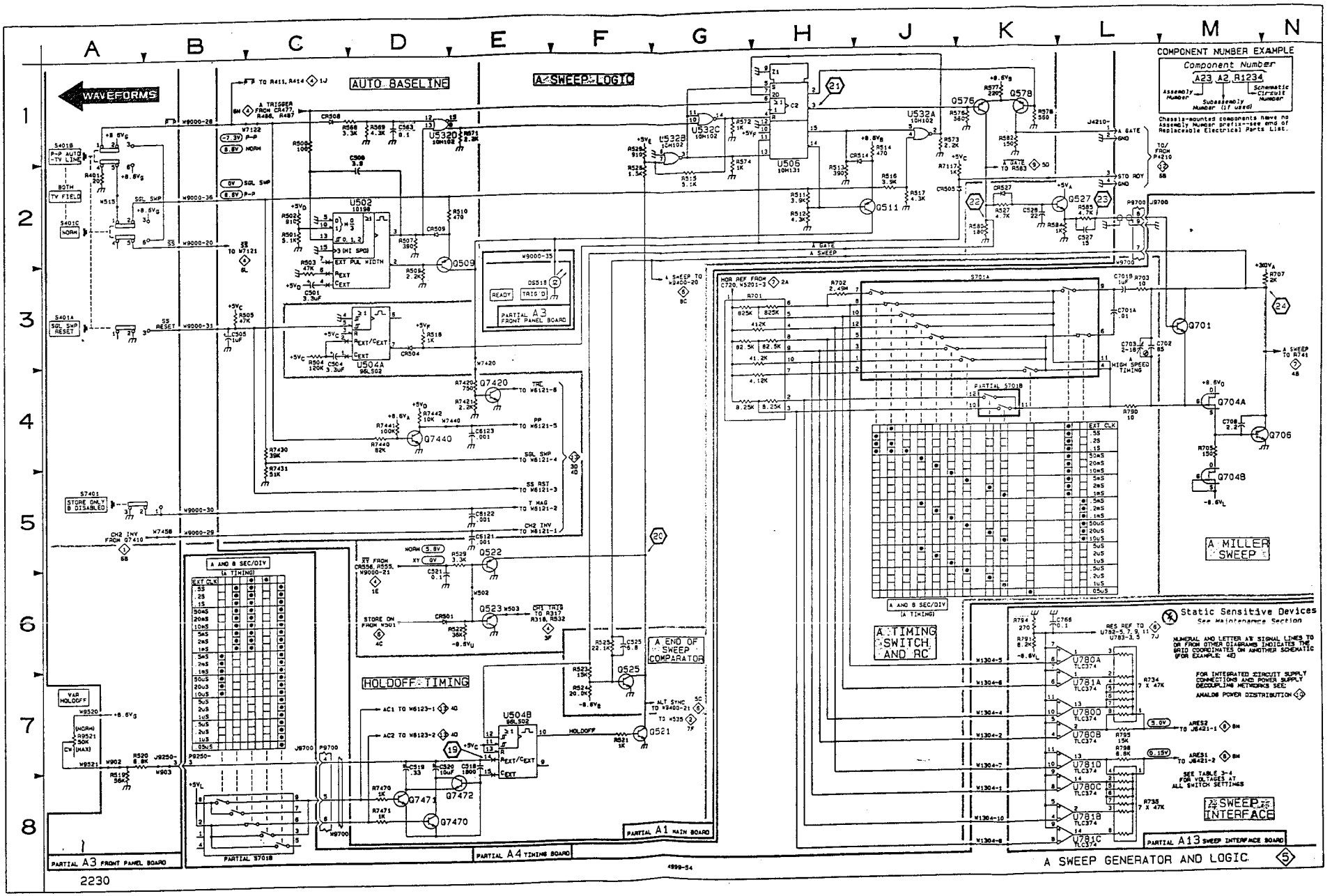
ASSEMBLY A13

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C766	6K	1C	R798	7L	1B	U781B	8L	1B
						U781C	8L	1B
R734	7L	1A	U780A	7L	1A	U781D	8L	1B
R735	8L	1A	U780B	7L	1A			
R791	6K	1B	U780C	8L	1A	W1304	7K	2A
R794	6K	1C	U780D	7L	1A			
R795	7L	1B	U781A	7L	1B			

Partial A13 also shown on diagrams 6 and 10.

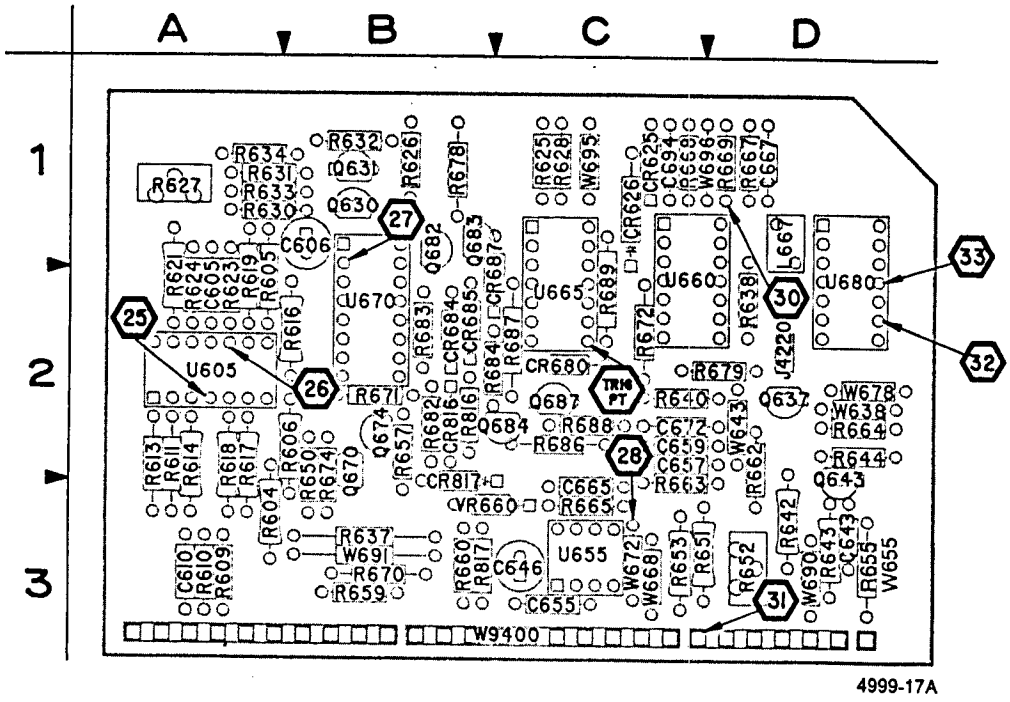
CHASSIS MOUNTED PARTS

P9700	2L	CHASSIS	R9521	7A	CHASSIS			
P9700	7C	CHASSIS						


WAVEFORMS
AUTO BASELINE
A SWEEP LOGIC
COMPONENT NUMBER EXAMPLE
Component Number
A23, A2, R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no assembly number prefix—see end of Replaceable Electrical Parts List.
A MILLER SWEEP
A TIMING SWITCH AND RC
A SWEEP INTERFACE
A SWEEP GENERATOR AND LOGIC
HOLDOFF TIMING
A END OF SWEEP COMPARATOR
Static Sensitive Devices
See Maintenance Section
PARTIAL A3 FRONT PANEL BOARD
PARTIAL A4 TIMING BOARD
PARTIAL A1 MAIN BOARD
PARTIAL A13 SWEEP INTERFACE BOARD
2230
4999-54

A5—ALTERNATE SWEEP BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C605	10	R611	6	R672	6
C606	10	R613	6	R674	6
C610	6	R614	6	R678	6
C643	6	R616	6	R679	9
C646	6	R617	6	R682	6
C655	10	R618	6	R683	6
C657	6	R619	6	R684	6
C659	10	R621	6	R686	6
C665	6	R623	6	R687	6
C667	6	R624	6	R688	6
C672	6	R625	6	R689	6
C694	10	R626	6	R816	9
		R627	6	R817	9
CR625	6	R628	6		
CR626	6	R630	6	U605	6
CR680	9	R631	6	U605	10
CR684	9	R632	6	U655	6
CR685	9	R633	6	U660	6
CR687	9	R634	6	U660	9
CR816	9	R637	6	U660	10
CR817	9	R638	6	U665	6
		R640	6	U665	9
J4220	9	R642	6	U665	10
		R643	6	U670	6
L667	6	R644	6	U670	10
		R650	6	U680	6
Q630	6	R651	6	U680	10
Q631	6	R652	6		
Q637	6	R653	6	VR660	6
Q643	6	R655	10		
Q670	6	R657	6	W638	6
Q674	6	R659	6	W643	6
Q682	6	R660	6	W655	10
Q683	6	R662	6	W668	6
Q684	6	R663	6	W672	6
Q687	6	R664	6	W678	6
		R665	6	W690	10
R604	6	R667	6	W691	10
R605	6	R668	6	W695	10
R606	6	R669	6	W696	10
R609	6	R670	6	W9400	6
R610	6	R671	6		

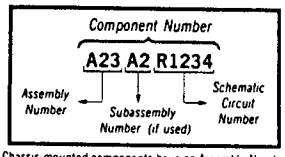


4999-17A

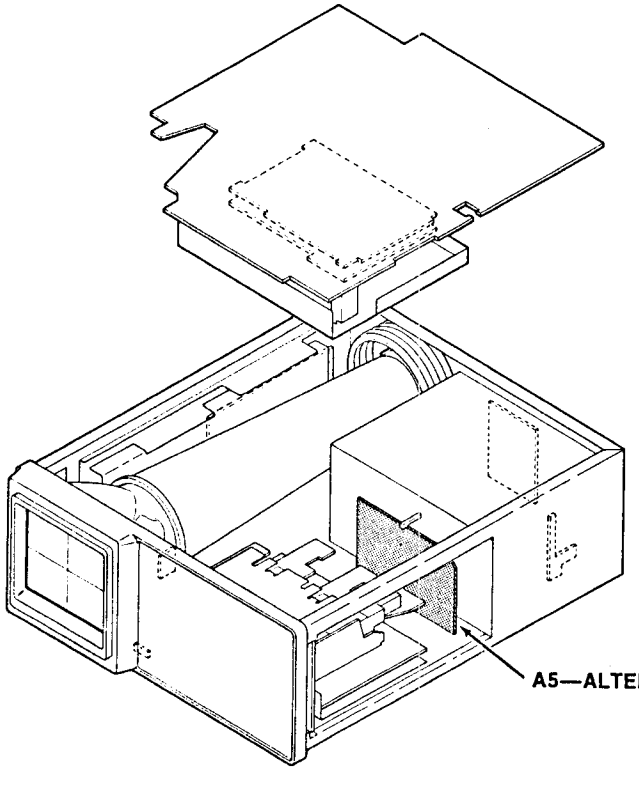
Figure 9-16. A5—Alternate Sweep board.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



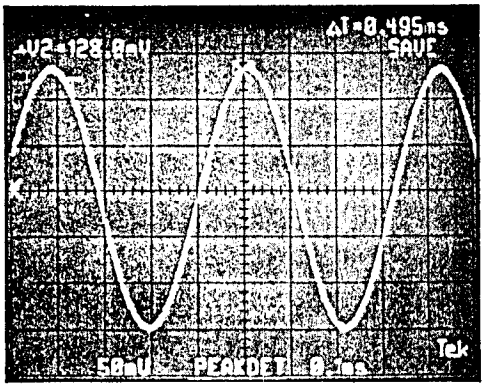
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



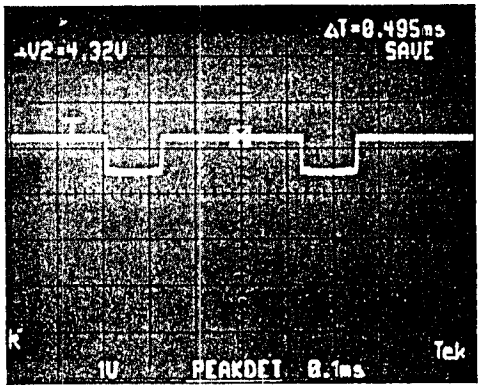
WAVEFORMS FOR DIAGRAM 6

TEST SCOPE TRIGGERED ON U665 PIN 8
FOR WAVEFORMS 25 THROUGH 30.

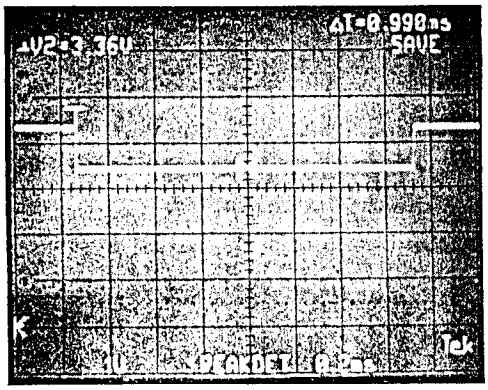
25



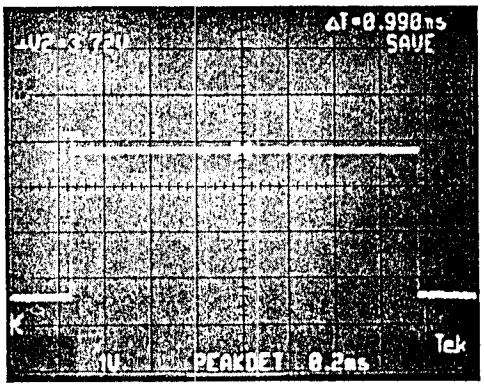
26



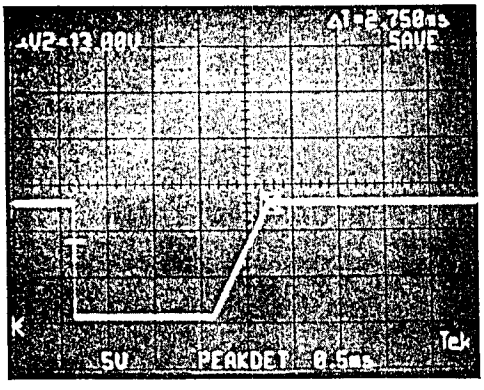
27



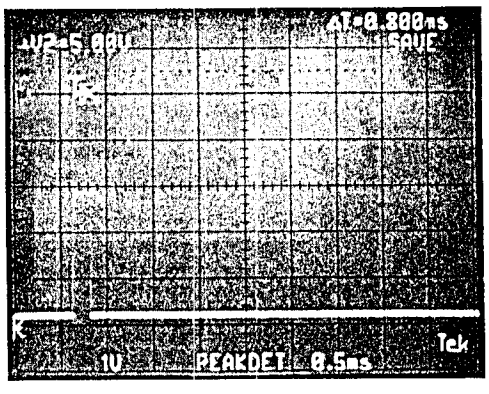
28



29

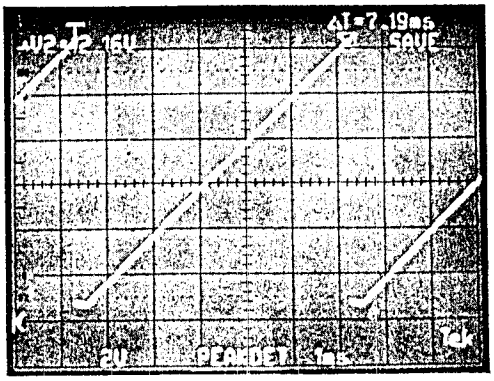


30

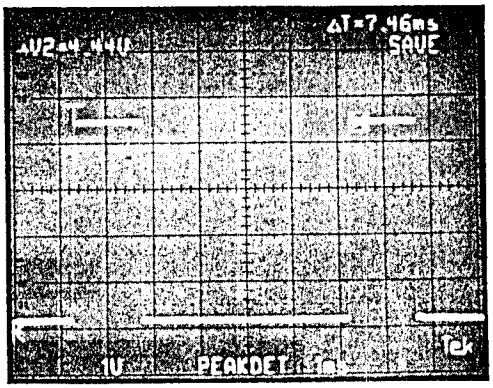


TEST SCOPE TRIGGERED ON U665 PIN 8
FOR WAVEFORMS 31 THROUGH 33.

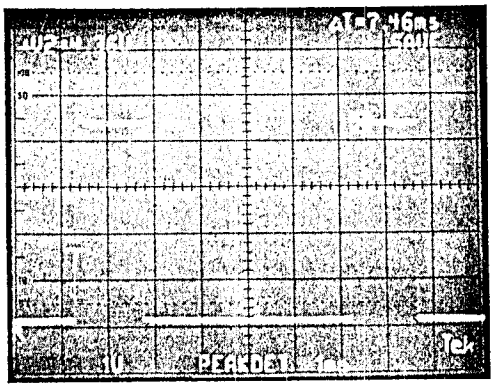
31



32



33



B TIMING AND ALTERNATE B SWEEP DIAGRAM 6

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C603	2B	7G	R554	4C	10F	W501	4C	9F	W9400	1C	9G
C635	5C	9G	R645	7B	10E	W602	1B	8G	W9400	2C	9G
C647	6C	8F	R646	8B	10E	W603	2B	8G	W9400	2K	9G
C648	6C	8F	R648	6C	10E	W635	5C	9G	W9400	3K	9G
C649	4C	7G	R649	6C	10E	W649	4C	8G	W9400	4C	9G
C7101	8B	9G	R675	2K	9G	W7120	6C	8B	W9400	5C	9G
			R7111	8B	9G	W7143	4C	10F	W9400	6C	9G
CR712	3K	10F				W9000	1B	8A	W9400	7C	9G
			VR645	7B	10F	W9000	2B	8A	W9400	8C	9G
J9010	4C	10G	VR712	3K	10F	W9000	6B	8A	W9700	3K	9F
J9644	7B	10F				W9000	6C	8A			

Partial A1 also shown on diagrams 2, 3, 4, 5, 7, 8, 9, 10 and 13.

ASSEMBLY A3

R602	1B	1F	S602	1A	1F	W901	1B	1E			
			S648	6A	2E	W904	1B	1D			

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 7, 9, 10 and 13.

ASSEMBLY A4

C673	4L	3B	Q709	4L	3C	R744	5L	3B	S701C	4J	1A
C701C	4L	3B	Q710A	5M	3C	R747	4K	3B			
C701D	4L	3B	Q710B	5M	3C	R763	6L	1D	U715A	6L	1D
C712	4L	3B	Q712	5M	3C	R765	6M	1D	U715B	6L	1D
C713	4L	2A				R767	6L	1D			
C714	5M	3C	R673	4L	3C	R769	6L	1C	W1304	6M	3B
			R704	2L	3B	R771	5L	3A	W1304	7H	3B
CR760	5L	2A	R709	4L	3B	R772	5L	3A	W1304	8H	3B
CR761	6L	3B	R710	5M	3C	R774	6L	1D			
			R711	4G	2D	R781	6M	1D			
J9700	2L	3C	R713	4M	3C						

Partial A4 also shown on diagrams 5, 7 and 10.

ASSEMBLY A5

C610	1D	3A	R610	1D	3A	R652	8D	3D	U660B	2G	1D
C643	3G	3D	R611	1D	2A	R653	8D	3C	U660D	1F	1D
C646	8D	3C	R613	3E	2A	R657	5E	2B	U660E	5D	1D
C657	7D	2C	R614	3D	2A	R659	8G	3B	U660F	2G	1D
C665	7E	3C	R616	2D	2B	R660	7D	3B	U665A	8F	1C
C667	5E	1D	R617	2D	2A	R662	7E	2D	U665C	8G	1C
C672	6K	2C	R618	2D	2A	R663	7D	3C	U665D	3J	1C
			R619	3D	2A	R664	8E	2D	U670A	1H	1B
CR625	2G	1C	R621	3D	2A	R665	7E	3C	U670B	6F	1B
CR626	2G	1C	R623	2E	2A	R667	5E	1D	U680A	5E	1D
			R624	3E	2A	R668	5D	1C	U680B	5D	1D
L667	5D	1D	R625	2H	1C	R669	5E	1D	U680C	8E	1D
			R626	1G	1B	R670	6E	3B	U680D	7E	1D
Q630	6K	1B	R627	3D	1A	R671	6E	2B			
Q631	6K	1B	R628	2G	1C	R672	6K	2C	VR660	7D	3B
Q637	1F	2D	R630	6K	1A	R674	4D	2B			
Q643	3H	2D	R631	6K	1A	R678	5G	1B	W638	1F	2D
Q670	6E	2B	R632	6K	1B	R682	6G	2B	W643	3H	2D
Q674	4E	2B	R633	6K	1A	R683	6F	2B	W668	5D	3C
Q682	6G	1B	R634	3J	1A	R684	6G	2B	W672	6K	3C
Q683	6F	1B	R637	1F	3B	R686	7G	2C	W678	5D	2D
Q684	6G	2B	R638	1F	2D	R687	7F	2C	W9400	1C	3A
Q687	7G	2C	R640	1F	2C	R688	7F	2C	W9400	2C	3A
			R642	3H	3D	R689	7G	2C	W9400	4C	3A
R604	2D	3A	R643	3G	3D				W9400	5C	3A
R605	2D	2A	R644	3H	2D	U605	1E	2A	W9400	6C	3A
R606	2D	2B	R650	4D	2B	U655	8D	3C	W9400	8C	3A
R609	1D	3A	R651	8D	3C	U660A	2G	1D			

Partial A5 also shown on diagrams 9 and 10.

B TIMING AND ALTERNATE B SWEEP DIAGRAM 6 (CONT)

ASSEMBLY A13

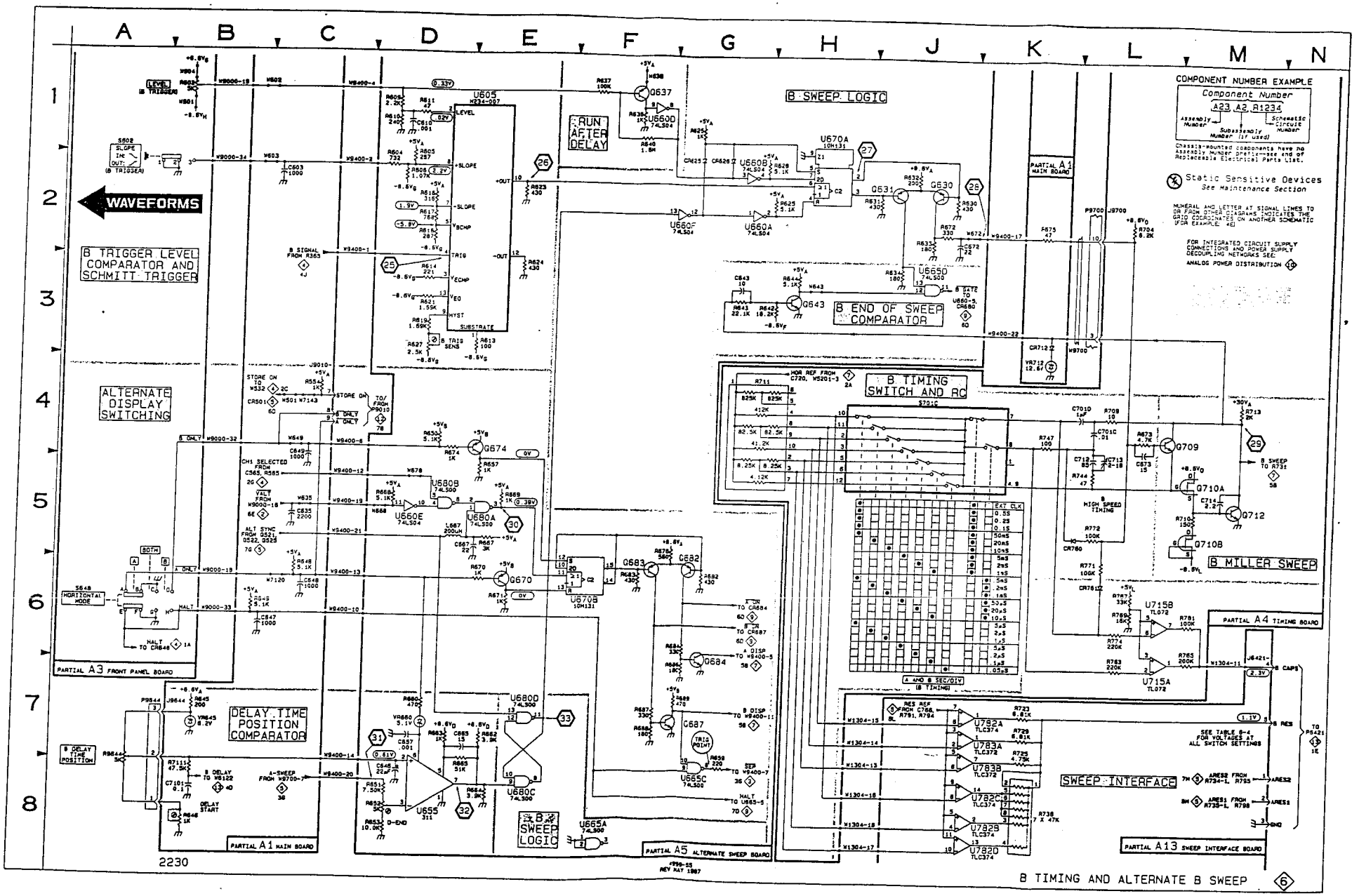
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J6421	6M	1C	R729	7K	1B	U782B	8K	1C	U783B	7K	1B
			R736	8K	1C	U782C	8K	1C			
R723	7K	1B				U782D	8K	1C	W1304	6M	2A
R725	7K	1B	U782A	7K	1C	U783A	7K	1B	W1304	7J	2A

Partial A13 also shown on diagrams 5 and 10.

CHASSIS MOUNTED PARTS

P9700	2L	CHASSIS									

WAVEFORMS FOR DIAGRAM 3



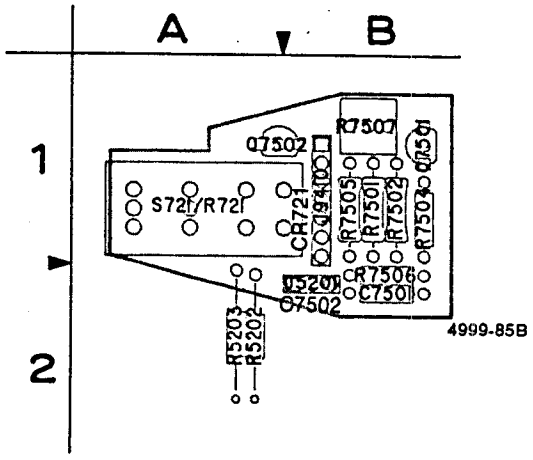
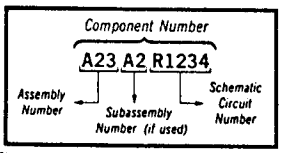


Figure 9-17. A16—Sweep Reference board.

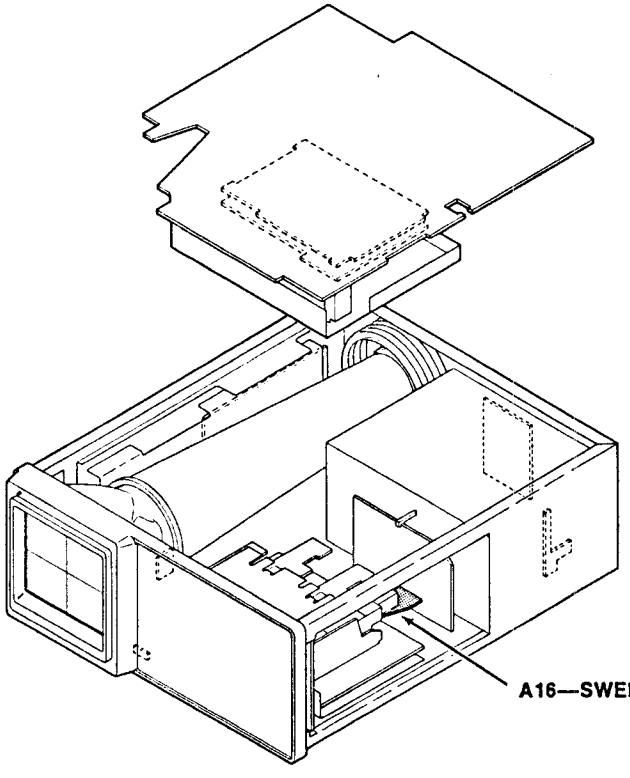
A16—SWEEP REFERENCE BOARD FIG. 9-17

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

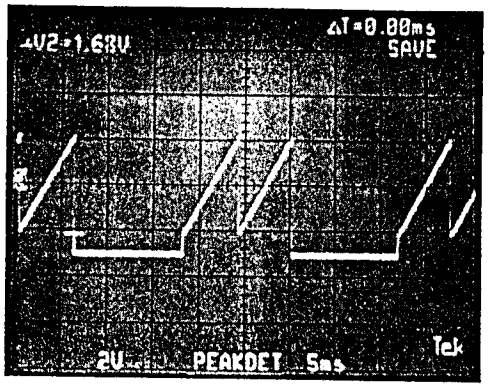


A16—SWEEP REFERENCE BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C7501	7			R7504	7
C7502	7	Q7501	7	R7505	7
		Q7502	7	R7506	7
CR721	7			R7507	7
		R721	7		
J5201	7	R7501	7	S721	7
J9410	7	R7502	7		

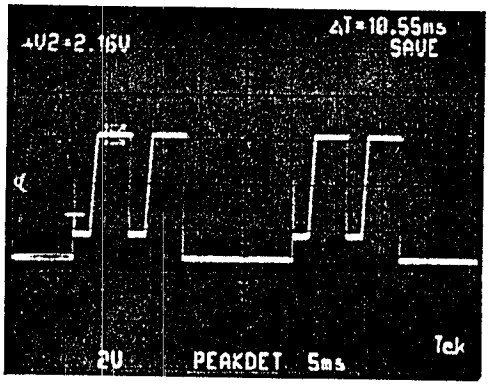
TEST SCOPE TRIGGERED ON U665 PIN 8
FOR WAVEFORMS 34 AND 35.

34



35

SN B02099
& BELOW



HORIZONTAL OUTPUT AMPLIFIER DIAGRAM 7

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C764	5J	3J	Q775	6L	3G	R786	3M	3G
C770	5K	3H	Q779	6M	4G	R787	4L	3G
C775	5L	4H	Q780	4K	3H	R788	4M	3G
C777	6L	3G	Q785	4L	3G	R789	3L	3G
C779	6L	3G	Q789	3M	3G	R792	5L	4G
C780	4K	3H				R793	5L	4G
C782	3K	2H	R566	5C	7F	R7301	7C	6E
C785	4K	3H	R676	5C	7F			
C787	3L	3G	R756	6B	6F	U758	6C	6F
C789	3L	2G	R757	6B	6E			
C7320	7C	4G	R758	6C	6E	VR764	5J	3J
			R759	6C	6E	VR782	4K	2H
CR764	5J	2J	R760	6C	6F			
CR765	5K	3H	R761	6C	6F			
						W570	5C	8F
CR768	5K	3H	R764	5J	3J	W732	5C	8F
CR770	5J	3H	R766	5K	3H	W770	4H	5G
CR780	4J	3J	R768	5K	3H	W780	6H	5G
CR7301	4H	4J	R770	6K	3H	W7320	7C	5E
CR7302	4H	4J	R773	6K	3G	W9000	7B	8A
CR7303	5H	4H	R775	5L	4H	W9400	5B	9G
CR7304	6H	3H	R776	6M	3G	W9700	6D	9F
CR7305	5H	3H	R777	5L	3G	W9705	6D	7F
CR7306	4H	4J	R778	6M	3G	W9705	6G	7F
CR7307	4H	4J	R779	6L	3G	W9778	6M	3G
CR7308	5H	4J	R780	4K	3H	W9788	4M	3G
			R782	4K	3H			
Q756	6B	6E	R783	4L	3H			
Q770	6K	3G	R785	4K	3H			

Partial A1 also shown on diagrams 2, 3, 4, 5, 6, 8, 9, 10 and 13.

ASSEMBLY A3

C987	8B	1E	R726	7B	1E	U985	8B	1D
			R985	8B	1E			
CR988	8C	1D	R986	8B	1E	W9900	8D	1A
CR989	8C	1D	R987	8B	1E			
			R988	8C	1D			
J9250	7D	3D	R989	8C	1D			
J9900	8D	1A	R990	8D	1C			

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 9, 10 and 13.

ASSEMBLY A4

C720	2B	1C	Q742	4E	3D	R745	5E	3C
C728	7E	1D				R746	5E	3D
C751	7F	2D	R727	7D	1B	R748	4G	3D
C755	3E	2E	R728	7E	1B	R749	5G	3E
			R730	5C	3D	R750	5G	3D
CR732	6D	3D	R731	5B	3D	R751	6E	2E
CR742	5D	3D	R732	5E	3C	R753	3F	2E
			R733	5E	3D	R754	3E	1E
J9700	5D	3C	R737	3E	1C	R755	3E	1E
J9705	4G	2E	R738	3E	1D	U760	2F	3E
J9705	6D	2E	R740	4C	3D			
			R741	4B	3D	VR746*	5E	3C
Q732	5E	3D	R742	4E	3C			
Q737	3E	2D	R743	4E	3D	W5201	2B	2E

Partial A4 also shown on diagrams 5, 6 and 10.

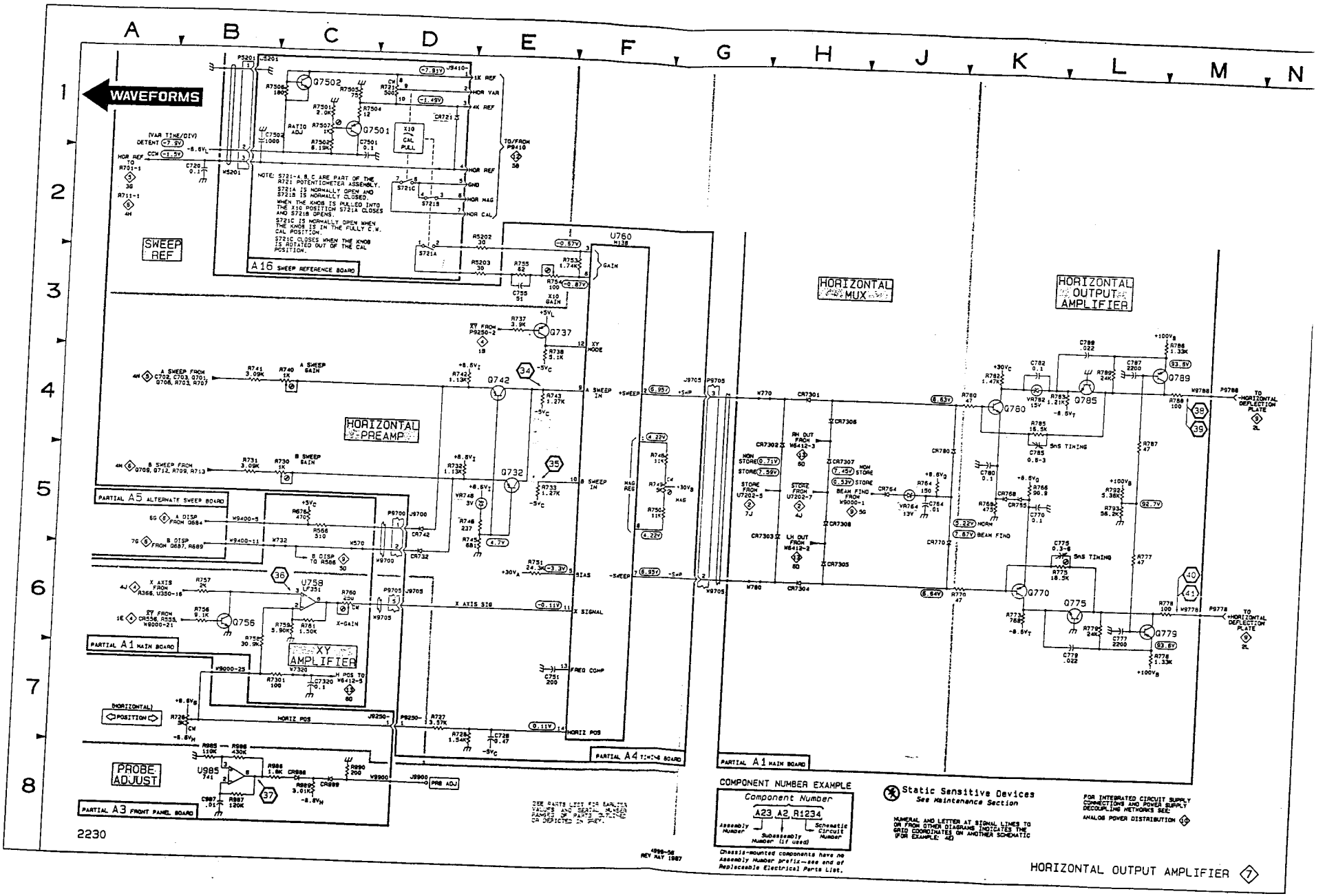
ASSEMBLY A16

C7501	1C	2B	R721	1D	1A	S721A	2D	1A
C7502*	2B	2B	R7501	1C	1B	S721B	2D	1A
CR721*	1D	1B	R7502	1C	1B	S721C	2D	1A
J5201	1B	2B	R7504	1C	1B			
J9410	1D	1B	R7505	1C	1B			
			R7506	1C	2B			
Q7501	1C	1B	R7507	1C	1B			
Q7502	1C	1B						

CHASSIS MOUNTED PARTS

P5201	1B	CHASSIS	P9705	4G	CHASSIS	P9788	4M	CHASSIS
P9250	7D	CHASSIS	P9705	6D	CHASSIS	R5202	2E	CHASSIS
P9700	5D	CHASSIS	P9778	6M	CHASSIS	R5203	3E	CHASSIS

***See Parts List f serial number ra**


WAVEFORMS
SWEEP REF
A16 SWEEP REFERENCE BOARD
HORIZONTAL PREAMP
HORIZONTAL MUX
HORIZONTAL OUTPUT AMPLIFIER
PARTIAL A5 ALTERNATE SWEEP BOARD
PARTIAL A1 MAIN BOARD
XY AMPLIFIER
PARTIAL A4 TIMING BOARD
PROBE ADJUST
PARTIAL A3 FRONT PANEL BOARD
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Static Sensitive Devices
See Maintenance Section
HORIZONTAL OUTPUT AMPLIFIER 7

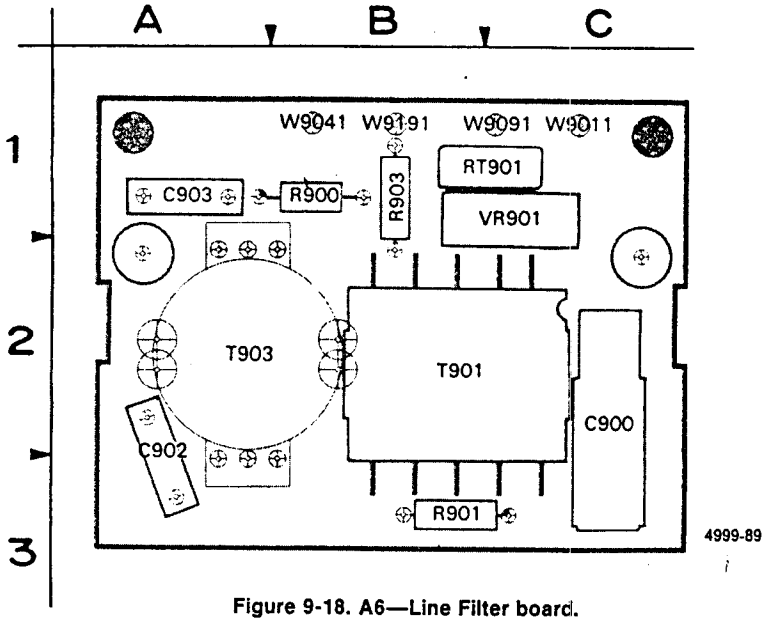
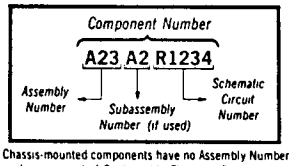


Figure 9-18. A6—Line Filter board.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

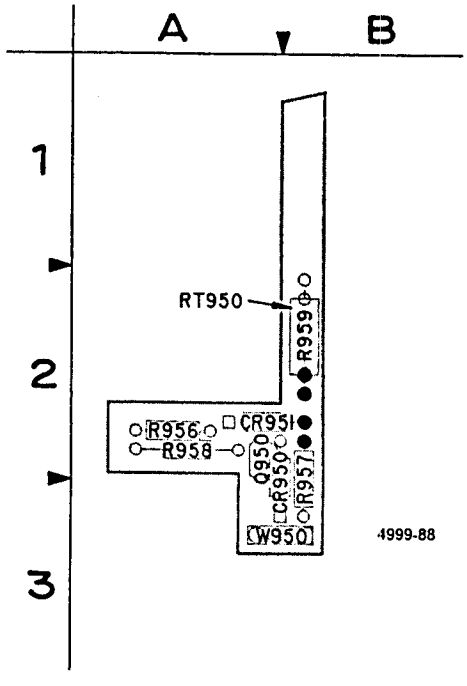


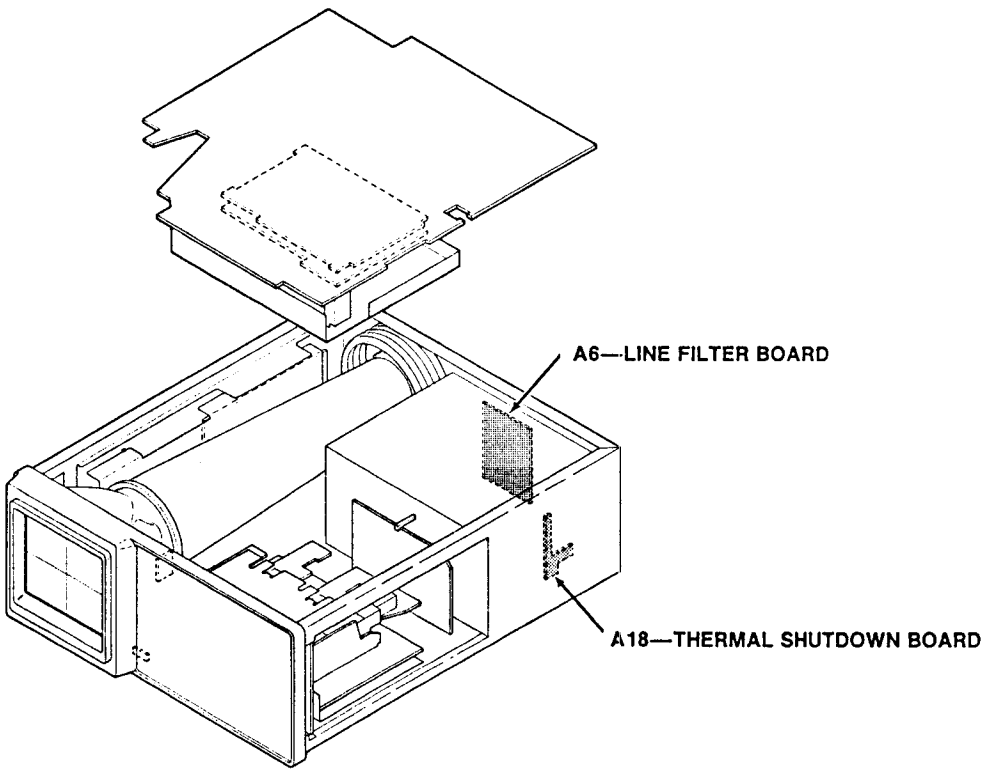
Figure 9-19. A18—Thermal Shutdown board.

A6—EMI FILTER BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C900	8	R903	8	W9011	8
C902	8	RT901	8	W9041	8
C903	8	T901	8	W9091	8
R900	8	T903	8	W9191	8
R901	8	VR901	8		

A18—THERMAL SHUTDOWN BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
CR950	8	R957	8	W950	8
CR951	8	R958	8	W950	8
Q950	8	R959	8		
R956	8	RT950	8		



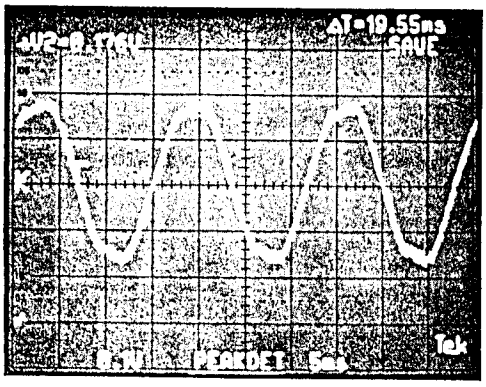
WAVEFORMS FOR DIAGRAM 8

AC Waveforms

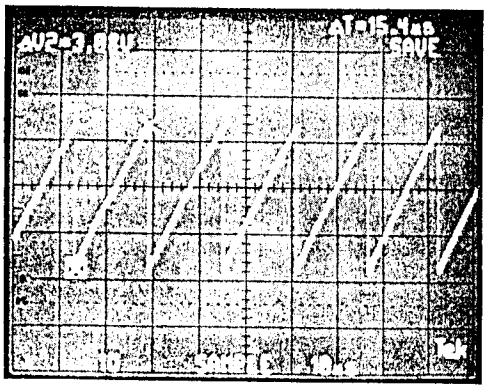
WARNING

ument must be connected to the ac-power ce using a 1:1 isolation transformer. Do not con- the test oscilloscope probe ground lead to the er circuit test points if the instrument is not iso- . AC-source voltage exists on reference points 0 and T906 pin 5.

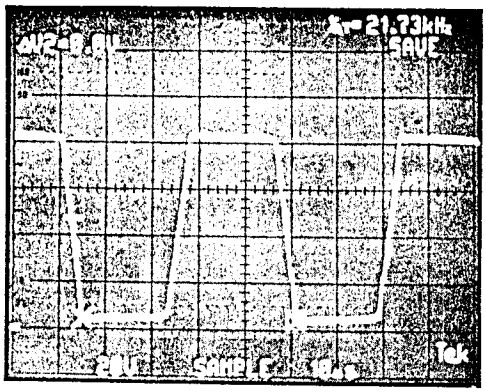
42



44



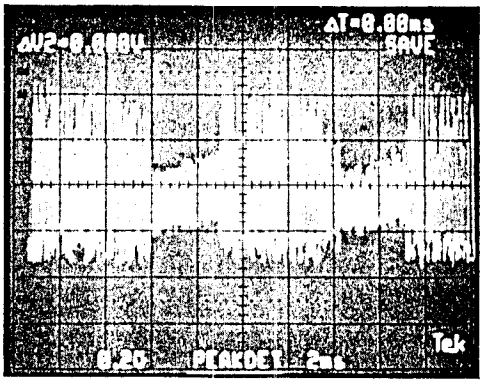
46



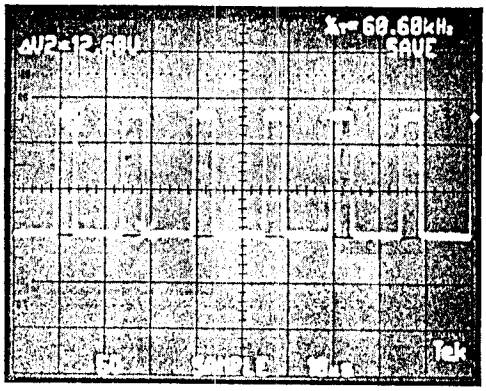
DC Voltages

Preregulator and Inverter voltages are referenced to test point noted adjacent to the voltage. Power supply output voltages are referenced to chassis ground.

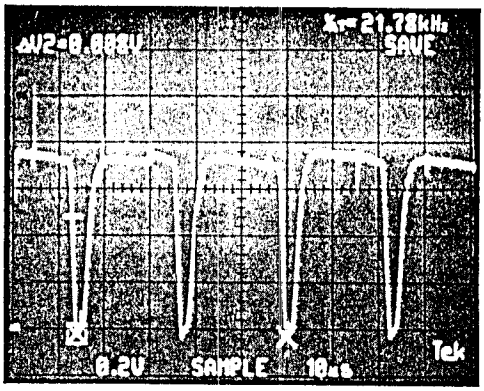
43



45



47



4999-87

POWER INPUT, PREREGULATOR AND INVERTER DIAGRAM 8

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C396	1E	5K	Q938	7J	10L	R940	8M	10L
C904	2D	5M	Q939	7J	10M	R941	7J	10M
C906	2E	7L	Q944	7L	10M	R942	7J	10L
C907	4J	8M	Q946	7M	10K	R943	7K	10L
C908	3J	7M	Q947	7M	9K	R944	7K	10M
C917	5F	10L	Q9070	4J	9K	R945	7L	10L
C919	4F	10M				R946	7M	10L
C922	3F	9L	R397	1E	6G	R947	7M	9K
C925	3E	10M	R398	1E	6G	R948	8K	10M
C940	5H	8K	R905	1D	5L	R949	7M	10L
C941	5J	8K	R906	1D	6L			
C942	7J	10L	R907	5H	8K	S901	1D	5M
C943	7M	10L	R908	5H	9L			
C944	7L	9L	R909	4H	9L	T390	1E	6L
C945	7L	10M	R910	1D	6B	T906	3H	8L
			R912	5E	9L	T944	7L	9K
CR901	2E	6M	R913	5E	9M			
CR902	2D	6M	R914	4F	9L	TP940	5J	10M
CR903	2E	6M	R915	4F	9L	TP950	2E	9L
CR904	2D	6M	R916	4F	10M			
CR907	4J	7L	R917	4F	9L	U930	5G	9M
CR908	4H	9L	R919	4F	10M			
CR920	2H	8M	R921	5F	9M	VR925	3F	9M
CR946	7L	10K	R922	4F	10M	VR935	8H	10M
CR947	7L	10K	R925	3F	9M	VR943	6K	10L
CR948	8K	10L	R926	2E	9M			
			R927	3F	9M	W950	6J	10L
E907	5H	8K	R928	3F	9M	W9040	2C	6L
			R929	2F	9M	W9070-1	5H	7K
P9070	4J	8K	R930	3F	9M	W9070-2	5H	8L
			R934	7H	10M	W9070-3	5H	9L
Q908	5H	9L	R935	8H	10M	W9150	1C	6A
Q928	3F	9M	R937	6J	10L	W9190	2C	6L
Q930	3G	9M	R938	7J	10M			
Q935	8H	10M	R939	7J	10L			

Partial A1 also shown on diagrams 2, 3, 4, 5, 6, 7, 9, 10 and 13.

ASSEMBLY A6

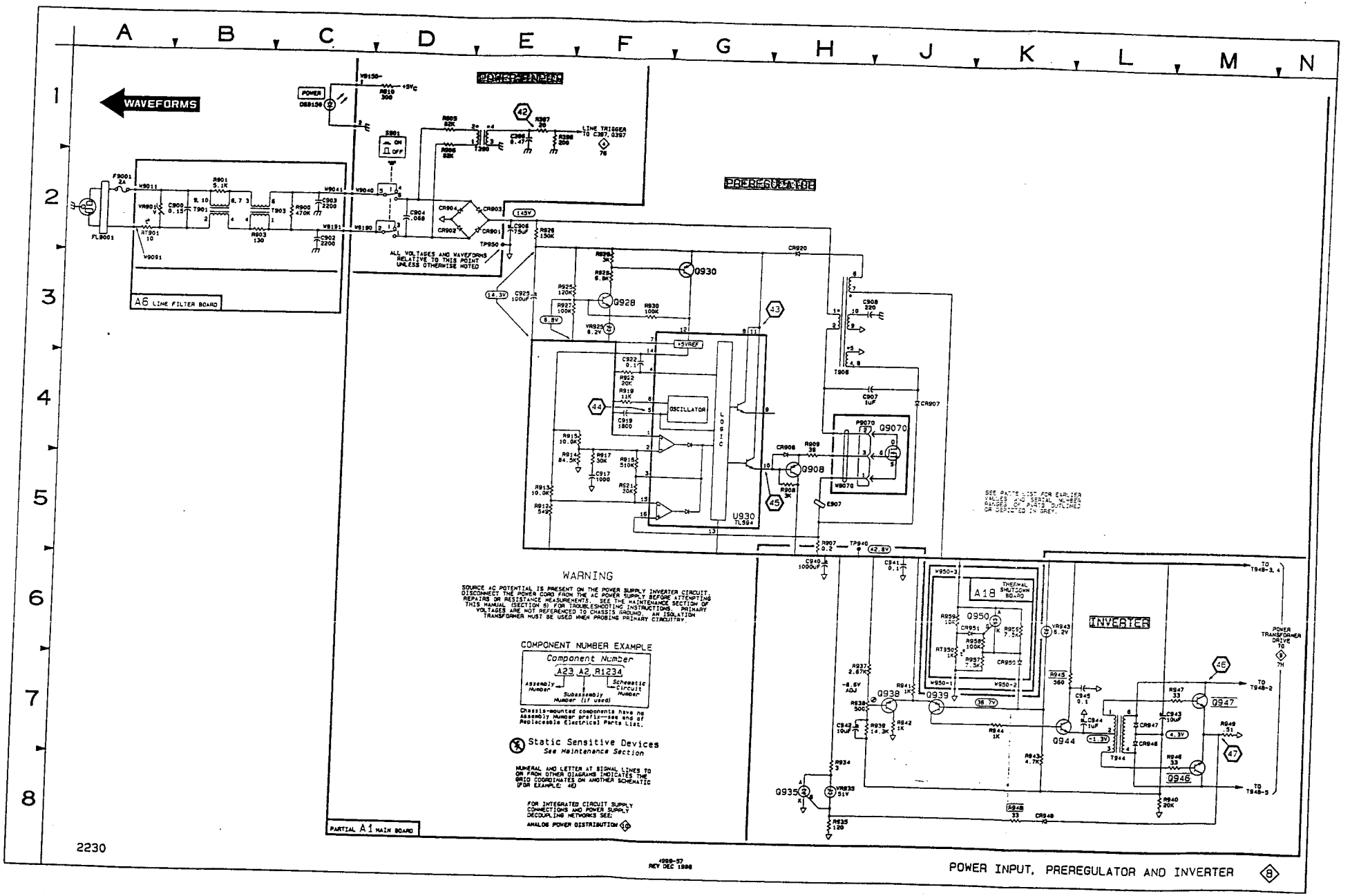
C900	2B	2C	RT901	2A	1C	W9011	2A	1C
C902	2C	2A				W9041	2C	1B
C903	2C	1A	T901	2B	2B	W9091	2A	1C
			T903	2B	2A	W9191	2C	1B
R900	2C	1B						
R901	2B	3B	VR901	2A	1C			
R903	2B	1B						

ASSEMBLY A18

CR950	6K	3B	R956	6K	2A	RT950	6K	2B
CR951	6K	2A	R957	6K	3B			
			R958	6K	2A	W950	6J	3B
Q950	6K	3A	R959	6K	2B	W950	7J	3B

CHASSIS MOUNTED PARTS

DS9150	1C	CHASSIS	FL9001	2A	CHASSIS			
F9001	2A	CHASSIS	P9070	4J	CHASSIS			



Static Sensitive Devic
See Maintenance Sectic

IMPONENT NUMBER EXAN

mber

R1234

Subassembly Number (if used)

mounted components have no Assem
see end of Replaceable Electrical P

FIG. 9-20
A7-INTENSITY POT BOARD

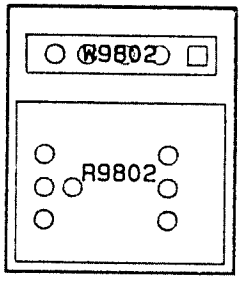
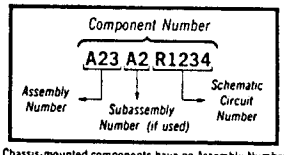


Figure 9-20. A7—Intensity Pot board.

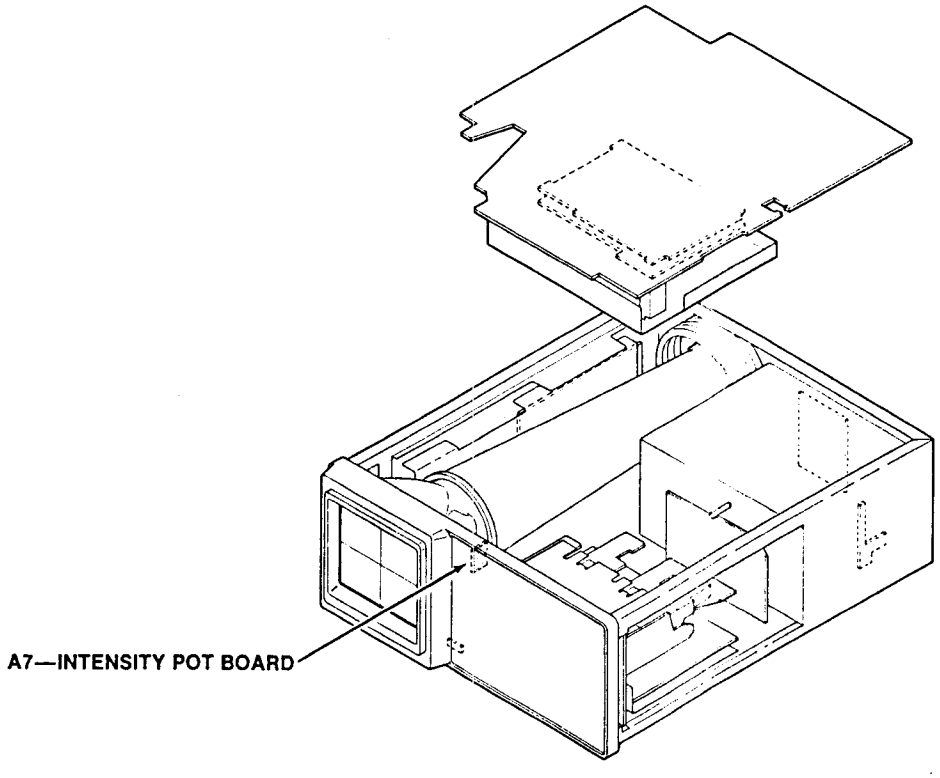
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
R9802	9	R9802	9	W9802	9

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



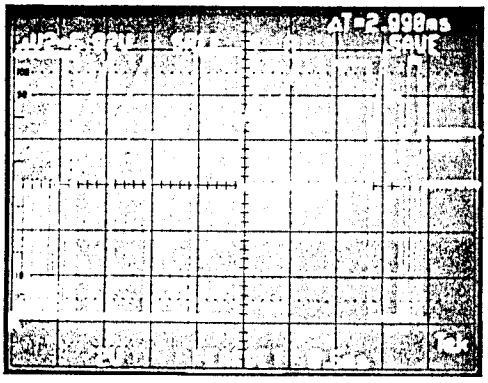
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



WAVEFORMS FOR DIAGRAM 9

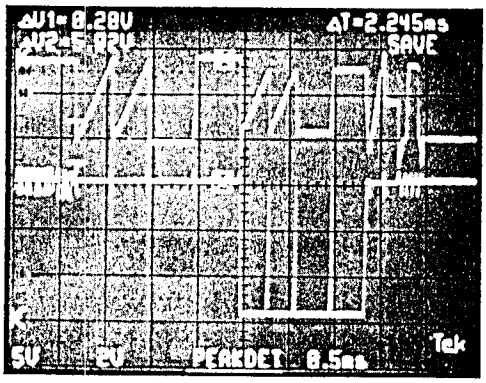
SET WAVEFORM REFERENCE/MENU SELECT SWITCH TO MENU SELECT
AND SELECT BOX FOR WAVEFORMS 48 THROUGH 50 AND 53.

11



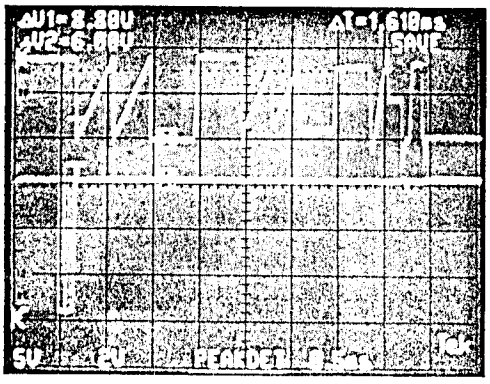
48

11



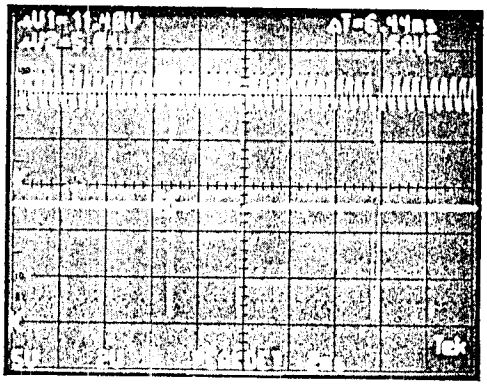
49

11



50

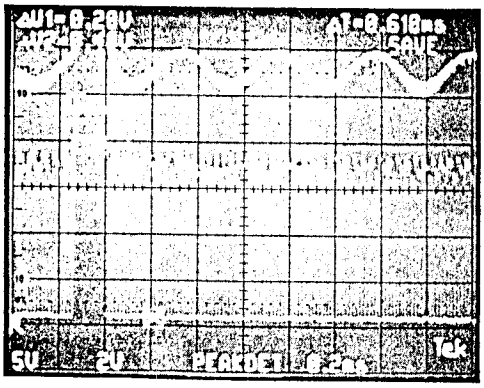
11



51

SET VERTICAL MODE SWITCH TO BOTH-CHOP

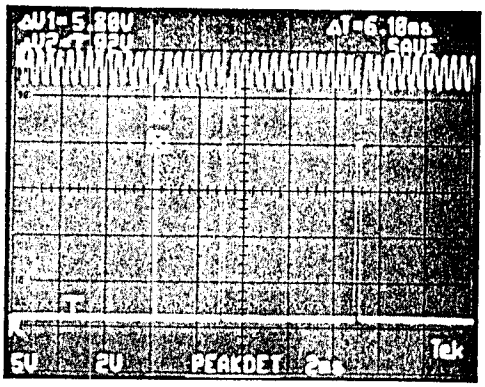
11



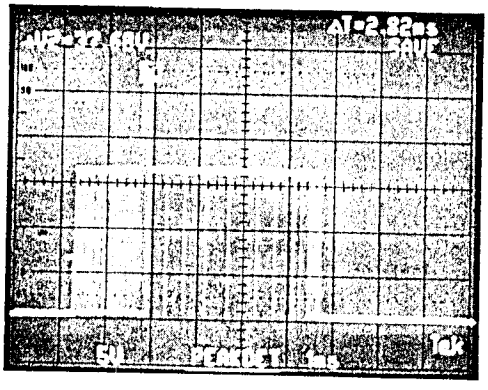
52

SET VERTICAL MODE SWITCH TO BOTH-ALT

11



52



53

POWER SUPPLY SECONDARIES, Z AXIS AND CRT DIAGRAM 9

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C547	3F	2M	CR853	4K	7K	R547	3F	2M	R888	2K	5J
C824	6F	8F	CR854	4K	6K	R548	4F	2M	R889	2K	5J
C825	5F	3L	CR855	4K	6K	R549	3G	2M	R890	2K	5J
C828	5G	4L	CR954	6K	7H	R581	3E	2L	R891	3K	5J
C835	4H	4L	CR955	5K	7H	R583	5D	8F	R892	3K	6H
C845	3H	4M	CR956	6K	7H	R586	5D	8F	R893	3K	5H
C847	3J	3M	CR957	6K	7H	R590	1F	3L	R894	3K	6H
C851	4J	7K	CR960	7J	10J	R595	1F	2L	R965	6K	10J
C853	4K	7J	CR961	7J	9H	R800	6B	6B	R976	5J	6J
C854	4K	7J	CR962	7J	10J	R804	5B	6B	R978	5K	6J
C855	3K	6K	CR963	7J	9H	R805	5B	6B	R7203	1B	1L
C871	2M	1L	CR965	6J	9J	R810	5B	6B	R7204	2F	2M
C873	3M	1K	CR967	6J	9J	R814	6B	6B	R7205	2C	1L
C875	3M	1K	CR980	8J	9J	R818	5E	7F	R7206	2F	2M
C877	4M	1L	CR981	8J	9J	R820	5E	7F	R7207	2B	1L
C893	4K	5J	CR7201	1G	2M	R822	4B	3M	R7208	2F	2M
C954	5K	7H	CR7202	2G	3M	R823	4B	3M	R7209	3B	2L
C956	6K	7H	CR7203	2G	3M	R825	5F	3L	R7260	2C	2L
C958	8L	10H				R826	4F	3M	R7261	1B	1L
C959	8L	10H	DS856	4K	6J	R828	5F	2K	R7262	2C	1L
C960	7K	10K	DS858	4K	6J	R830	4G	3M	R7263	2B	1L
C961	7K	10H	DS870	5L	6J	R832	1G	3M			
C962	7L	10J				R834	4H	4L	T948	5J	8J
C963	7L	10H	J9210	1B	2K	R835	4G	4L			
C964	8K	10J	J9802	5B	5B	R836	4G	4M	TP842	3J	4L
C965	6K	9K	J9965	6K	10J	R840	4H	4L			
C968	8K	9H				R841	4H	4M	U5378	3F	1M
C970	8L	8H	L960	7K	10J	R842	3J	4M	U975	5J	6H
C975	5J	6J	L961	7K	10H	R844	3H	3M			
C976	5J	7J	L962	8K	10J	R845	3H	3M	VR828	5F	3L
C979	5K	6J	L968	8K	9H	R849	3H	3M			
C7201	3F	3M				R851	4J	4M	W565	3E	4K
			Q583	5E	8F	R852	4J	4M	W575	3E	3L
CR551	5E	7F	Q586	5E	8F	R853	4K	7J	W7202	3B	2L
CR590	1G	2M	Q804	5B	6B	R854	4K	7J	W7250	5C	6B
CR805	6B	6B	Q814	6C	6B	R858	4K	6J	W9000	5F	8A
CR818	5E	8F	Q825	4F	3L	R860	4K	6J	W9080	8J	8H
CR820	5E	7F	Q829	4G	3M	R870	2N	1K	W9400	6C	9G
CR823	4B	3L	Q835	4H	4M	R871	2N	1K	W9400	6F	9G
CR824	4G	2M	Q840	4H	4M	R872	3N	1K	W9800	4B	4M
CR825	4G	3M	Q845	3H	3M	R873	2N	1K	W9870-10	2M	1L
CR829	4F	3M	Q7201	1C	1L	R874	3N	1K	W9870-4	4L	6J
CR840	4H	4M	Q7202	2C	1M	R875	3N	1K			
CR845	3H	3M	Q7203	2C	1M	R877	4M	1K			
CR851	4J	7J	Q7204	3E	2M	R886	2K	5J			

Partial A1 also shown on diagrams 2, 3, 4, 5, 6, 7, 8, 10 and 13.

ASSEMBLY A3

J9006	1M	2A	R982 R983	1M 1M	2A 2A	S390	6G	2A			

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 10 and 13.

ASSEMBLY A5

CR680	6E	2B	CR816	6E	2B	R679	7E	2D	U660C	7D	1D
CR684	6E	2B	CR817	6E	3B	R816	6E	2B	U665B	7D	1C
CR685	7E	2B				R817	6E	3B			
CR687	6E	2B	J4220	7E	2D						

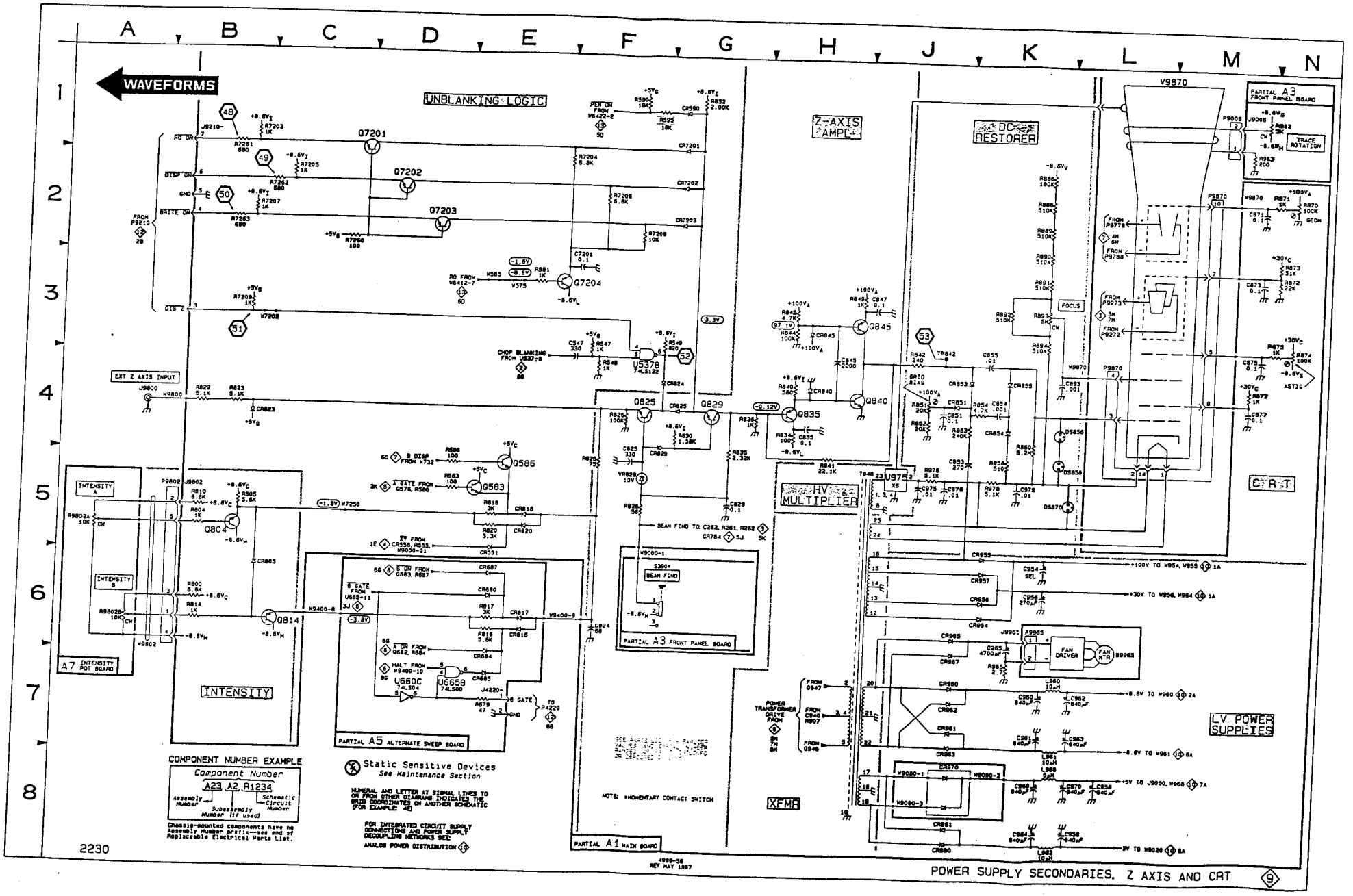
Partial A5 also shown on diagrams 6 and 10.

ASSEMBLY A7

R9802A	5A	1A	R9802B	6A	1A	W9802	6A	1A			

CHASSIS MOUNTED PARTS

B9965	6L	CHASSIS	J9800	4A	CHASSIS	P9802 P9965	5B 6K	CHASSIS CHASSIS	V9870	1L	CHASSIS



POWER SUPPLY SECONDARIES, Z AXIS AND CRT 9

A1—MAIN BOARD FIG. 9-9
A7-INTENSITY POT BOARD FIG. 9-20
A5—ALTERNATE SWEEP BOARD FIG. 9-16
A16—SWEEP REFERENCE BOARD FIG. 9-17
A2—ATTN, A14—CH 1 &
A6—LINE FILTER, A18—THERMAL SHUTDOWN BOARDS FIG. 9-18, -19

ANALOG POWER DISTRIBUTION DIAGRAM 10

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C116	4B	4C	C849	1A	3M	U501	2D	6C	W961	6A	10G
C200	3C	4F	C849	1A	3M	U502	7D	10C	W964	1A	4K
C201	4B	4F	C7203	3B	3K	U504	7B	8E	W965	2A	3K
C215	4A	1C	C7260	3B	1L	U506	8D	9E	W968	7A	10G
C220	3C	2E				U532	8D	10E	W971	2A	9F
C255	4B	1G	E200	3C	5F	U537	8G	1M	W972	3A	7F
C274	2A	2K	E201	4A	5F	U540	8G	2L	W974	3A	3L
C420	2B	7C	E272	1B	2J	U555	8F	4F	W975	3A	3K
C421	6B	8C	E590	7C	10D	U565	8G	2K	W976	6A	9F
C460	8C	8D				U758	4F	6F	W977	5A	7F
C480	5D	9D	J9010	7H	10G	U7201	8G	2J	W979	5D	3K
C494	3F	7E	J9050	7H	7G	U7202	3B	3J	W991	2C	7C
C499	5F	6D	J9060	7H	7G				W993	6G	7C
C502	7C	10C	J9300	8H	4L	W400	5D	9C	W995	6E	8B
C503	7A	7E				W408	6D	9B	W997	3C	5F
C506	8C	9E	R220	3D	2E	W494	3F	7E	W998	5A	5F
C507	7A	7C	R494	3F	7F	W542	8A	7B	W999	4A	3F
C531	8C	10D	R499	5F	7F	W544	2C	6A	W9000	2J	8A
C537	7F	1M	R796	5D	2J	W556	8F	3K	W9000	3J	8A
C540	7F	2L	R797	3A	3J	W591	8C	9E	W9020	8A	10G
C553	8F	4F	R799	1B	4G	W592	7C	10D	W9035	2A	10F
C562*	5G	7A	R964	7F	4L	W885	5G	5K	W9068	7F	10G
C590	8C	8D	R966	7A	9F	W954	1A	7G	W9400	5J	9G
C796	4D	2J				W955	1A	4L	W9400	6J	9G
C797	3A	3J	U225	4D	1D	W956	1A	6G	W9705	5J	7F
C799	1B	4G	U426	4E	8B	W959	1A	5G	W9991	2J	7F
C832	3B	3L	U460	8D	8D	W960	2A	10G			

Partial A1 also shown on diagrams 2, 3, 4, 5, 6, 7, 8, 9 and 13.

ASSEMBLY A2

C90	1J	2F	J9991	1J	3F	U10	1K	1C	W94	1K	1F
C91	1J	3F				U60	1L	3C	W96	2K	3F
C93	1J	2F	L90	1J	2F						
C94	1K	1E	L91	1J	3F	VR10	1K	1D			
C96	2J	3F	L93	1J	3F	VR60	1L	3D			
C97	2K	3D	L96	2J	3F						

Partial A2 also shown on diagram 1.

ASSEMBLY A3

C905*	2J	1B	U985	2K	1D						

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9 and 13.

ASSEMBLY A4

C705	4K	3B	C750	4K	1D	R752	3K	3D	VR749	3J	2E
C706	5K	3B	C752	3K	3D						
C707	3J	3C				U715	3J	1D	W1304	3H	3B
C710	4K	3B	J9705	3J	2E	U750	4J	2D	W1304	4M	3B
C724	5K	3D				U751	4J	2D	W1304	5M	3B
C749	4K	2D	R724	4K	3C	U760	4K	3E			

Partial A4 also shown on diagrams 5, 6 and 7.

ASSEMBLY A5

C605	6J	2A	C694	6K	1C	U665	6M	1C	W690	6J	3D
C606	6J	1B	R655*	J5	3D	U670	6K	1B	W691	6K	3B
C655	6K	3C	U605	6K	2A	U680	6L	1D	W695	6M	1C
C659	5K	2C	U660	6L	1D	W655*	5J	3D	W696	6M	1C

Partial A5 also shown on diagrams 6 and 9.

ASSEMBLY A13

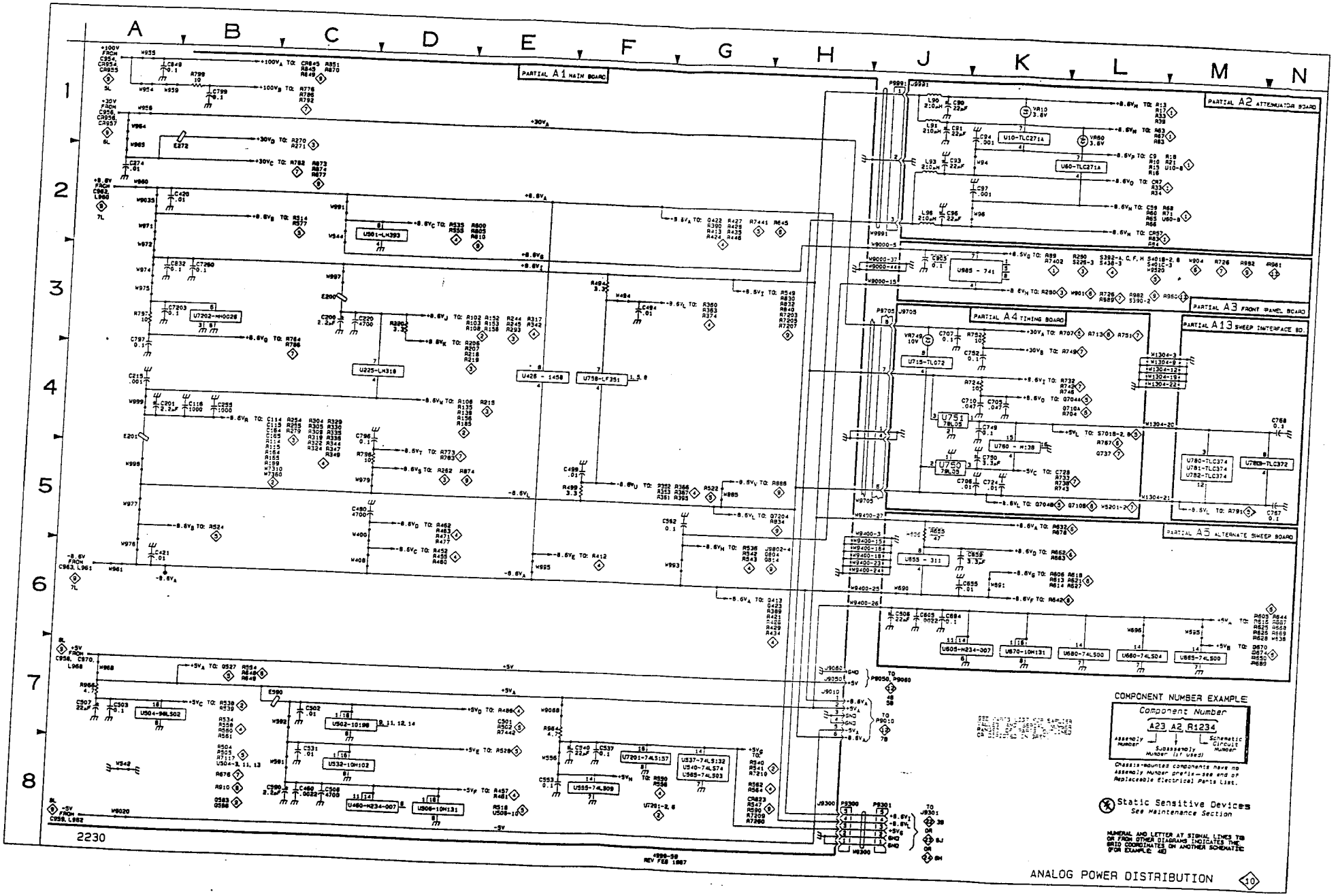
C767	5N	2D	U780	4M	1A	U783	4N	1B			
C768	4N	2D	U781	4M	1B						
			U782	4M	1C						

Partial A13 also shown on diagrams 5 and 6.

CHASSIS MOUNTED PARTS

P9705	3J	CHASSIS	P9991	1J	CHASSIS						

***See Parts List serial number ra**



A1—MAIN BOARD FIG. 9-9

A7-INTENSITY POT BOARD FIG. 9-

A5—ALTERNATE SWEEP

A16—SWEEP REFERENCE BOARD FIG. 9-17

A6—LINE FILTER, A18—THERMAL

or
nges.

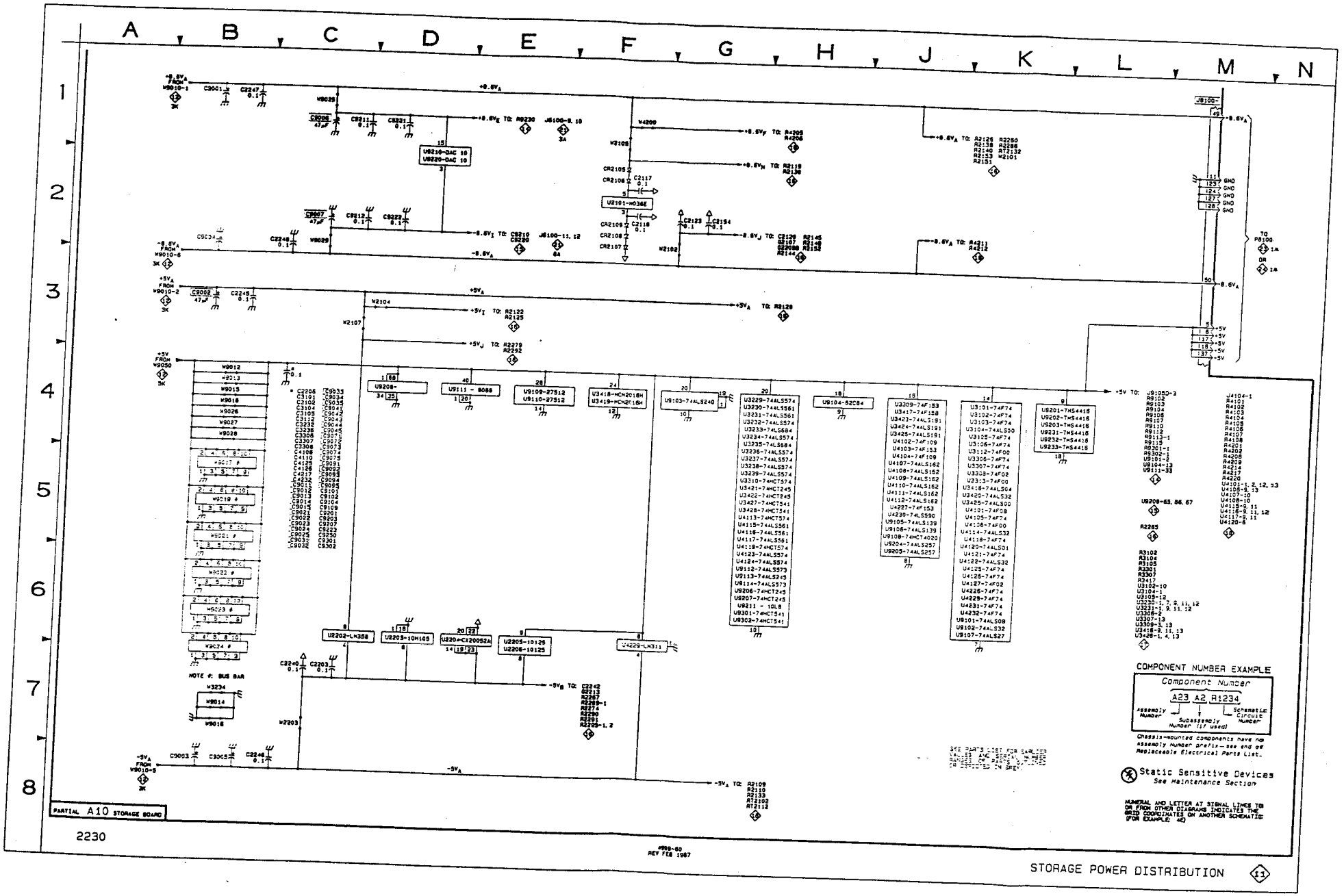
STORAGE POWER DISTRIBUTION DIAGRAM 11

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2117	2F	2G
C2118	2F	2G
C2123	2G	3H
C2154	2G	1H
C2203	7C	1K
C2206	4C	3K
C2240	7C	2J
C2245	3B	4G
C2246	8C	4F
C2247	1B	4G
C2248	2C	4F
C3101	4C	4M
C3102	4C	3L
C3104	4C	3L
C3105	4C	2L
C3112	4C	5K
C3232	4C	4J
C3236	4C	4J
C3306	4C	4K
C3307	4C	5K
C3308	4C	5L
C4106	5C	8L
C4110	5C	7M
C4125	5C	8M
C4126	5C	5M
C4217	5C	9M
C4232	5C	9L
C9001*	1B	
C9002	3B	10F
C9003*	8B	
C9004*	2B	
C9005*	8B	
C9006	1C	9E
C9007	2C	9E
C9011	5C	5G
C9012	5C	6G
C9013	5C	7G
C9014	5C	8G
C9015	5C	9G
C9021	5C	5H
C9022	5C	6H
C9023	5C	7H
C9024	5C	8H
C9025	5C	9H
C9031	5C	5J
C9032	5C	6J
C9033	4C	7J
C9034	4C	8J
C9035	4C	9J
C9041	4C	5K
C9042	4C	6K
C9043	4C	7K
C9044	4C	8K
C9045	4C	9K
C9071	4C	4D
C9072	4C	5D
C9073	4C	6D
C9074	5C	7D
C9075	5C	8D
C9091	5C	4E
C9092	5C	5E
C9093	5C	6E
C9094	5C	7E
C9095	5C	8E
C9101	5C	3E
C9102	5C	7E
C9104	5C	6E
C9109	5C	3C
C9201	5C	7C
C9203	5C	5C
C9207	5C	5C
C9211	1B	9C
C9212	2C	10C
C9221	1D	9D
C9222	2D	10D
C9223	5C	8B
C9250	5C	7B
C9301	5C	5B
C9302	5C	4B
CR2105	2F	2G
CR2106	2F	2G
CR2107	2F	1F
CR2108	2F	1F
CR2109	2F	1F
J8100	1M	2D
U2101	2F	2G
U2202	6C	3J
U2203	6D	3L
U2204	6E	3K
U2205	6E	3K
U2206	6E	3K
U3101	4K	4M
U3102	4K	3L
U3103	4K	4L
U3104	4K	3L
U3105	4K	2L
U3106	4K	6M
U3112	4K	6K
U3229	4H	4K
U3230	4H	7K
U3231	4H	5K
U3232	4H	4J
U3233	4H	5J
U3234	4H	7J
U3235	4H	7J
U3236	4H	4J
U3237	4H	5J
U3238	5H	7H
U3239	5H	8H
U3306	4K	4K
U3307	4K	5K
U3308	5K	5L
U3309	4J	4L
U3310	5H	5F
U3313	5K	5L
U3416	5K	5H
U3417	4J	5H
U3418	4F	5G
U3419	4F	5H
U3420	5K	5G
U3421	5H	8G
U3422	5H	8H
U3423	4J	6G
U3424	4J	6G
U3425	4J	6F
U3426	5K	5G
U3427	5H	7G
U3428	5H	7F
U4101	5K	5M
U4102	4J	7K
U4103	4J	7L
U4104	4J	7L
U4105	5K	9M
U4106	5K	8L
U4107	4J	7K
U4108	5J	7K
U4109	5J	7L
U4110	5J	7L
U4111	5J	8K
U4112	5J	8L
U4113	5H	8K
U4114	5K	9H
U4115	5H	9G
U4116	5H	8F
U4117	5H	9H
U4118	5K	10J
U4119	5H	9J
U4120	5K	9J
U4121	5K	10J
U4122	5K	9H
U4123	5H	9G
U4124	5H	9H
U4125	5K	8M
U4126	6K	6M
U4127	6K	7M
U4226	6K	9K
U4227	5J	9K
U4228	6K	9L
U4229	6F	9L
U4230	5J	8J
U4231	6K	9J
U4232	6K	9L
U9101	6K	5E
U9102	6K	7E
U9103	4G	6D
U9104	4H	6E
U9105	5J	8E
U9106	5J	7E
U9107	6K	6D
U9108	5J	6E
U9109	4E	4C
U9110	4E	4C
U9111	4E	4E
U9112	6H	4D
U9113	6H	4E
U9114	6H	5D
U9201	4L	7C
U9202	4L	8D
U9203	4L	7D
U9204	5J	5D
U9205	5J	5C
U9206	6H	7C
U9207	6H	6B
U9208	4D	8B
U9210	1D	10C
U9211	6H	6C
U9220	2D	10C
U9231	4L	6C
U9232	4L	8D
U9233	4L	7D
U9301	6H	5B
U9302	6H	4B
W2102	2G	4F
W2104	3D	4G
W2105	1F	4F
W2107	3C	4H
W2203	7C	3H
W3234	7B	7J
W4200	1F	10K
W9012	4B	8E
W9013*	4B	8D
W9014	7B	3C
W9015	4B	3E
W9016	7B	3D
W9017*	5B	3D
W9018	4B	3E
W9019*	5B	3E
W9021*	5B	5G
W9022*	6B	5H
W9023*	6B	5J
W9024*	7B	5K
W9025	1C	9D
W9026	4B	4L
W9027	4B	10J
W9028	4B	5J
W9029	2C	10D

Partial A10 also shown on diagrams 12, 14, 15, 16, 17, 18 and 21.

*See Parts List for serial number ranges.


A B C D E F G H J K L M N
1 2 3 4 5 6 7 8
PARTIAL A10 STORAGE BOARD
2230
STORAGE POWER DISTRIBUTION
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no assembly number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4D)
NOTE #: BUS BAR
TO P8100
TO: R2265
TO: U9050-3 R9102 R9103 R9104 R9106 R9107 R9110 R9112 R9113-1 R9115 R9301-1 R9302-1 U9101-3 U9104-13 U9113-13
U9208-65, 66, 67
R3102 R3104 R3105 R3301 R3307 R3417 U3102-10 U3104-1 U3109-12 U3232-1, 2, 9, 11, 12 U3231-1, 9, 11, 12 C3206-2 C3307-13 C3309-3, 13 C3418-9, 11, 13 C3426-1, 4, 13
U4104-1 R4101 R4102 R4103 R4104 R4105 R4106 R4107 R4108 R4201 R4202 R4208 R4209 R4214 R4217 R4226 C4101-1, 2, 12, 13 C4106-9, 13 C4107-10 C4108-10 C4115-9, 11 C4116-9, 11, 12 C4117-9, 11 C4120-8
+8.6V FROM W9010-1
+8.6V FROM W9010-6
+5V FROM W9010-2
+5V FROM W9050
-5V FROM W9010-5
-8.6V
+5V
-5V
GND
U8210-DAC 10
U8220-DAC 10
U2101-MC1536E
U9111 - 8088
U9109-27512
U9110-27512
U9103-74ALS240
U9104-82C84
U9208-
U2202-LM358
U2203-10H105
U2204-CX20052A
U2205-10125
U2206-10125
U4229-LM311
U3418-MCM2016H
U3419-MCM2016H
U3229-74ALS574
U3230-74ALS561
U3231-74ALS561
U3232-74ALS574
U3233-74ALS684
U3234-74ALS574
U3235-74ALS684
U3236-74ALS574
U3237-74ALS574
U3238-74ALS574
U3239-74ALS574
U3310-74HC7574
U3421-74HCT245
U3422-74HCT245
U3427-74HC7541
U3428-74HC7541
U4113-74HC7574
U4115-74ALS561
U4116-74ALS561
U4117-74ALS561
U4118-74HC7574
U4123-74ALS574
U4124-74ALS574
U9112-74ALS573
U9113-74ALS245
U9114-74ALS573
U9206-74HCT245
U9207-74HCT245
U9211 - 10LB
U9301-74HC7541
U9302-74HC7541
U3309-74F153
U3417-74F158
U3423-74ALS191
U3424-74ALS191
U3425-74ALS191
U4102-74F109
U4103-74F153
U4104-74F109
U4107-74ALS162
U4108-74ALS162
U4109-74ALS162
U4110-74ALS162
U4111-74ALS162
U4112-74ALS162
U4227-74F153
U4239-74LS590
U9105-74ALS139
U9106-74ALS139
U9108-74HCT4020
U9204-74ALS257
U9205-74ALS257
U3101-74F74
U3102-74F74
U3103-74F74
U3104-74ALS00
U3125-74F74
U3106-74F74
U3112-74F00
U3306-74F74
U3307-74F74
U3308-74F02
U3313-74F00
U3416-74ALS04
U3426-74ALS32
U3425-74ALS00
U4101-74F08
U4105-74F74
U4126-74F00
U4114-74ALS32
U4118-74F74
U4120-74ALS01
U4121-74F74
U4122-74ALS32
U4125-74F74
U4126-74F74
U4127-74F02
U4226-74F74
U4228-74F74
U4231-74F74
U4232-74F74
U9101-74ALS08
U9102-74ALS32
U9107-74ALS27
U9201-THS4416
U9202-THS4416
U9203-THS4416
U9231-THS4416
U9232-THS4416
U9233-THS4416
SEE PART'S LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS NOT LISTED IN GREY
REV FEB 1987

STORAGE WIRING INTERCONNECT DIAGRAM 12

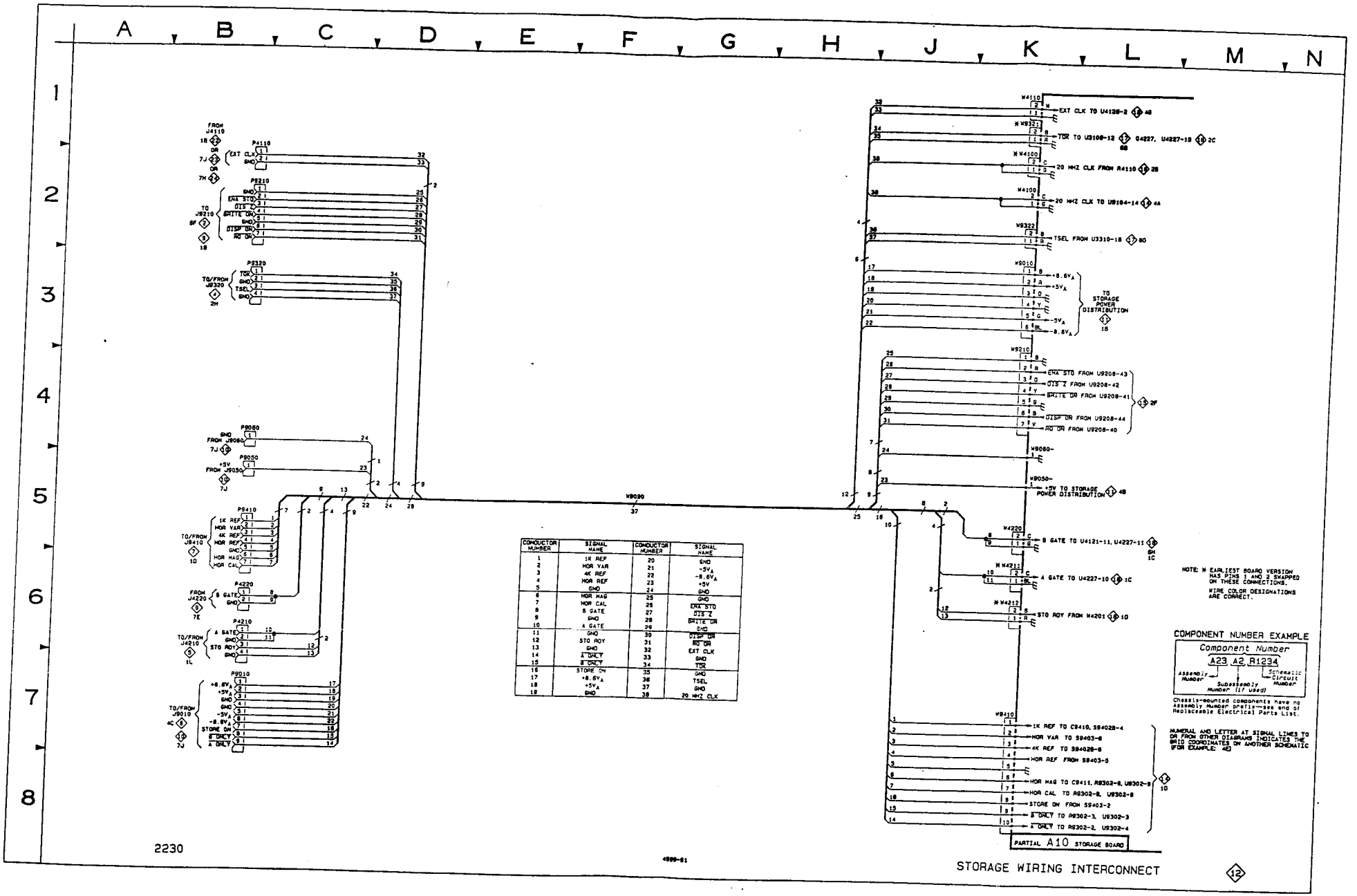
ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
W4100-1	1K	6E	W4212	6K	10K	W9090	5F	10G
W4100-2	2K	7K	W4220	5K	10K	W9210	4K	9B
W4110	1K	5L	W9010	3K	9F	W9321	1K	5L
W4211	5K	10K	W9050	5K	10F	W9322	2K	5F
W4212	6K	10K	W9060	4K	10F	W9410	7K	7B

Partial A10 also shown on diagrams 11, 14, 15, 16, 17, 18 and 21.

CHASSIS MOUNTED PARTS

P4110	1B	CHASSIS	P9010	7B	CHASSIS	P9210	2B	CHASSIS
P4210	6B	CHASSIS	P9050	5B	CHASSIS	P9320	3B	CHASSIS
P4220	6B	CHASSIS	P9060	4B	CHASSIS	P9410	5B	CHASSIS



CONDUCTOR NUMBER	SIGNAL NAME	CONDUCTOR NUMBER	SIGNAL NAME
1	1K REF	20	GND
2	HOR VAR	21	$-5V_A$
3	4K REF	22	$-8.6V_A$
4	HOR REF	23	+5V
5	GND	24	GND
6	HOR MAG	25	GND
7	HOR CAL	26	ENA STO
8	B GATE	27	DIS Z
9	GND	28	BRITE ON
10	A GATE	29	GND
11	GND	30	DISP ON
12	STO ROY	31	RD ON
13	GND	32	EXT CLK
14	A ONLY	33	GND
15	B ONLY	34	TSR
16	STORE ON	35	GND
17	$+8.6V_A$	36	TSEL
18	$+5V_A$	37	GND
19	GND	38	20 MHZ CLK

NOTE: * EARLIEST BOARD VERSION HAS PINS 1 AND 2 SWAPPED ON THESE CONNECTIONS.
WIRE COLOR DESIGNATIONS ARE CORRECT.

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4C)

STORAGE WIRING INTERCONNECT 12

INPUT/OUTPUT WIRING INTERCONNECT DIAGRAM 13

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C951	3C	6A	VR954	3C	8B	W6411	6D	2D
R953	2C	7A	W6121	3D	8A	W6412	6D	4J
R954	3C	8A	W6122	4D	8F	W6413	3D	6A
VR953	2C	6A	W6123	4D	9F	W6422	5D	3L
			W6130	2D	7A	W9000	2C	8A
						W9000	3C	8A

Partial A1 also shown on diagrams 2, 3, 4, 5, 6, 7, 8, 9 and 10.

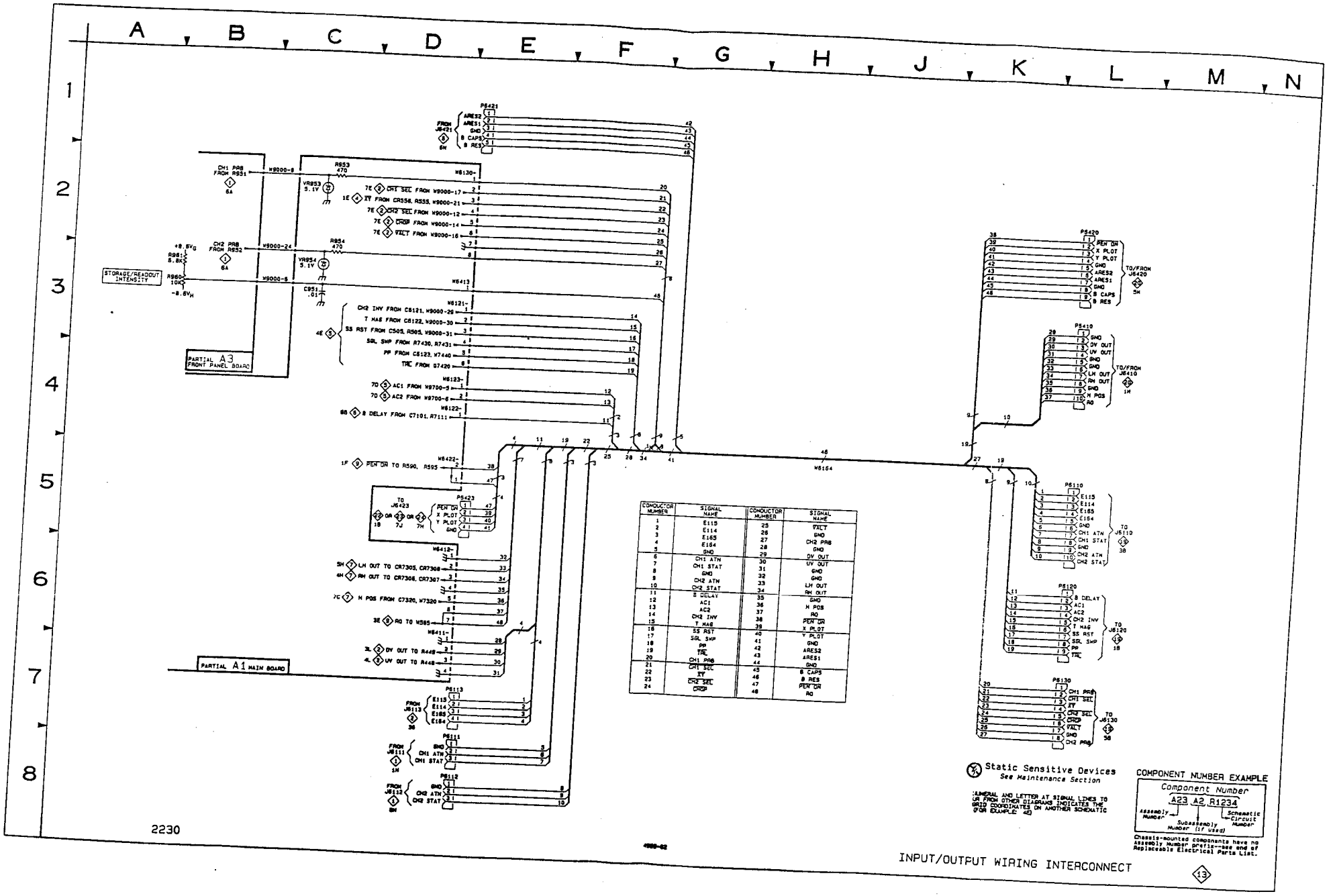
ASSEMBLY A3

R960	3B	3A	R961	3B	1A			

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9 and 10.

CHASSIS MOUNTED PARTS

P6110	5L	CHASSIS	P6120	6L	CHASSIS	P6421	1E	CHASSIS
P6111	7E	CHASSIS	P6130	7L	CHASSIS	P6423	5E	CHASSIS
P6112	8E	CHASSIS	P6410	3L	CHASSIS			
P6113	7E	CHASSIS	P6420	2L	CHASSIS			


A7—INTENSITY POT
A5—ALTERNATE SWEEP
A6—LINE FILTER, A18—THERMAL
A B C D E F G H J K L M N
1 2 3 4 5 6 7 8
PARTIAL A3 FRONT PANEL BOARD
PARTIAL A1 MAIN BOARD
STORAGE/READOUT INTENSITY
CH1 PRB FROM R951
CH2 PRB FROM R952
W9000-8
W9000-24
W9000-6
R953 470
R954 470
VR953 5.1V
VR954 5.1V
C951 .01
R961 5.6K
R960 10K
+8.5V
-8.5V
W8130
W8413
W8121
W8123
W8122
W8422
W8412
W8411
P5421
P5423
P5113
P5111
P5112
P5420
P5410
P5110
P5120
P5130
TO/FROM J6420
TO/FROM J6410
TO J5110
TO J6120
TO J6130
TO J5423
FROM J6421
FROM J6113
FROM J6111
FROM J6112
CH1 ATN
CH1 STAT
CH2 ATN
CH2 STAT
CH1 SEL FROM W9000-17
XY FROM CR556, R555, W9000-21
CH2 SEL FROM W9000-12
CRDP FROM W9000-14
VALT FROM W9000-16
CH2 INV FROM C8121, W9000-26
T MAG FROM C8122, W9000-30
SS RST FROM C505, R505, W9000-31
SGL SWP FROM R7430, R7431
PP FROM C8123, W7440
TRC FROM Q7420
AC1 FROM W8700-5
AC2 FROM W8700-6
B DELAY FROM C7101, R7111
PEN DR TO R590, R595
LH OUT TO CR7305, CR7306
RH OUT TO CR7308, CR7307
H POS FROM C7320, W7320
RO TO W585
DV OUT TO R448
UV OUT TO R448
PEN DR
X PLOT
Y PLOT
GND
B CAPS
B RES
ARES2
ARES1
CONDUCTOR NUMBER
SIGNAL NAME
E115
E114
E165
E164
GND
CH1 ATN
CH1 STAT
CH2 ATN
CH2 STAT
B DELAY
AC1
AC2
CH2 INV
T MAG
SS RST
SGL SWP
PP
TRC
CH1 PRB
CH1 SEL
XY
CH2 SEL
CRDP
VALT
CH2 PRB
DV OUT
UV OUT
LH OUT
RH OUT
H POS
RO
PEN DR
X PLOT
Y PLOT
B CAPS
B RES
ARES2
ARES1
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES OF ANOTHER SCHEMATIC
EXAMPLE 4E
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
INPUT/OUTPUT WIRING INTERCONNECT
13
2230

A B C D E F G H J K L M
1 2 3 4 5 6 7 8 9 10
J8100
U9109
U9110
U9111
U9112
U9113
U9114
U9930
U9205
U9204
U9210
U9206
U9208
S9401
S9402
S9403
U2204
T2202
U2207
U2208
U2210
U3105
U3102
U3103
U3104
U3107
U3108
U3109
U3110
U3112
U3233
U3234
U3236
U3238
U3239
U3330
U3331
U3332
U3333
U3334
U3335
U3336
U3337
U3338
U3339
U3340
U3341
U3342
U3343
U3344
U3345
U3346
U3347
U3348
U3349
U3350
U3351
U3352
U3353
U3354
U3355
U3356
U3357
U3358
U3359
U3360
U3361
U3362
U3363
U3364
U3365
U3366
U3367
U3368
U3369

A10—STORAGE BOARD (cont)

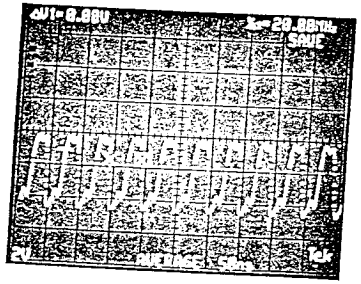
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
U4126	18	U9113	11	W2105	11
U4127	11	U9113	14	W2107	11
U4127	18	U9114	11	W2203	11
U4226	11	U9114	14	W3234	11
U4226	18	U9201	11	W4100	12
U4227	11	U9201	15	W4110	12
U4227	18	U9202	11	W4200	11
U4228	11	U9202	15	W4201	18
U4228	18	U9203	11	W4211	12
U4229	11	U9203	15	W4212	12
U4229	18	U9204	11	W4220	12
U4230	11	U9204	15	W9010	12
U4230	18	U9205	11	W9012	11
U4231	11	U9205	15	W9013	11
U4231	18	U9206	11	W9014	11
U4232	11	U9206	15	W9015	11
U4232	18	U9207	11	W9016	11
U9101	11	U9207	15	W9017	11
U9101	14	U9208	11	W9018	11
U9102	11	U9208	15	W9019	11
U9102	14	U9210	11	W9021	11
U9103	11	U9210	15	W9022	11
U9103	14	U9211	11	W9023	11
U9104	11	U9211	15	W9024	11
U9104	14	U9220	11	W9025	11
U9105	11	U9220	15	W9026	11
U9105	14	U9231	11	W9027	11
U9106	11	U9231	15	W9028	11
U9106	14	U9232	11	W9029	11
U9107	11	U9232	15	W9050	12
U9107	14	U9233	11	W9060	12
U9108	11	U9233	15	W9090	12
U9108	14	U9301	11	W9210	12
U9109	11	U9301	14	W9211	15
U9109	14	U9302	11	W9321	12
U9110	11	U9302	14	W9322	12
U9110	14			W9410	12
U9111	11	W2101	16		
U9111	14	W2102	11	Y4100	18
U9112	11	W2103	16		
U9112	14	W2104	11		

A10—STORAGE BOARD

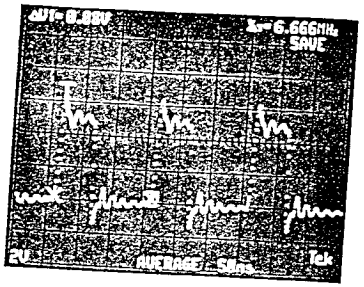
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C2101	16	C9032	11	Q2207	16	R2286	16			U3416	11
C2102	16	C9033	11	Q2208	16	R2287	16	RT2101	16	U3416	17
C2103	16	C9034	11	Q2209	16	R2289	16	RT2102	16	U3417	11
C2104	16	C9035	11	Q2211	16	R2290	16	RT2103	16	U3417	17
C2111	16	C9041	11	Q2212	16	R2291	16	RT2111	16	U3418	11
C2112	16	C9042	11	Q2213	16	R2292	16	RT2112	16	U3418	17
C2113	16	C9043	11	Q4203	18	R2293	16	RT2113	16	U3419	11
C2114	16	C9044	11	Q4204	18	R2295	16	RT2131	16	U3420	11
C2115	16	C9045	11	Q4205	18	R2296	16	RT2132	16	U3420	17
C2116	16	C9071	11	Q4207	18	R2297	16			U3421	11
C2117	11	C9072	11	Q4227	18	R3102	17	S9401	14	U3421	17
C2118	11	C9073	11	Q9100	14	R3104	17	S9402	14	U3422	11
C2119	16	C9074	11			R3105	17	S9403	14	U3422	17
C2120	16	C9075	11	R2101	16	R3232	17			U3423	11
C2123	11	C9091	11	R2102	16	R3234	17	T2201	16	U3423	17
C2151	16	C9092	11	R2104	16	R3301	17	T2202	16	U3424	11
C2152	16	C9093	11	R2105	16	R3307	17	T2203	16	U3424	17
C2153	16	C9094	11	R2106	16	R3310	17			U3425	11
C2154	11	C9095	11	R2107	16	R3417	17	U2101	11	U3425	17
C2203	11	C9101	11	R2108	16	R3423	17	U2101	16	U3426	11
C2206	11	C9102	11	R2109	16	R4101	18	U2202	11	U3426	17
C2224	16	C9104	11	R2110	16	R4102	18	U2202	16	U3427	11
C2225	16	C9107	14	R2111	16	R4103	18	U2203	11	U3427	17
C2226	16	C9109	11	R2112	16	R4104	18	U2203	16	U3428	11
C2228	16	C9201	11	R2114	16	R4105	18	U2204	11	U3428	17
C2229	16	C9202	15	R2115	16	R4106	18	U2204	16	U4101	11
C2230	16	C9203	11	R2116	16	R4107	18	U2205	11	U4101	17
C2233	16	C9205	14	R2117	16	R4108	18	U2205	16	U4101	18
C2235	16	C9206	14	R2118	16	R4110	18	U2206	11	U4102	11
C2236	16	C9207	11	R2119	16	R4115	18	U2206	16	U4102	18
C2237	16	C9210	15	R2120	16	R4119	18	U3101	11	U4103	11
C2238	16	C9211	11	R2121	16	R4201	18	U3101	17	U4103	17
C2239	16	C9212	11	R2122	16	R4202	18	U3102	11	U4103	18
C2240	11	C9220	15	R2123	16	R4203	18	U3102	17	U4104	11
C2241	16	C9221	11	R2124	16	R4204	18	U3103	11	U4104	17
C2242	16	C9222	11	R2125	16	R4205	18	U3103	17	U4104	18
C2245	11	C9223	11	R2126	16	R4206	18	U3104	11	U4105	11
C2246	11	C9250	11	R2127	16	R4207	18	U3104	17	U4105	18
C2247	11	C9301	11	R2128	16	R4208	18	U3105	11	U4106	11
C2248	11	C9302	11	R2129	16	R4209	18	U3105	17	U4106	18
C3101	11	C9410	14	R2130	16	R4210	18	U3106	11	U4107	11
C3102	11	C9411	14	R2131	16	R4211	18	U3106	17	U4107	18
C3104	11			R2133	16	R4212	17	U3112	11	U4108	11
C3105	11	CR2101	16	R2137	16	R4213	18	U3112	17	U4108	18
C3112	11	CR2102	16	R2138	16	R4214	18	U3112	18	U4109	11
C3232	11	CR2103	16	R2139	16	R4215	18	U3113	18	U4109	18
C3236	11	CR2104	16	R2140	16	R4216	18	U3229	11	U4110	11
C3306	11	CR2105	11	R2141	16	R4217	18	U3229	17	U4110	18
C3307	11	CR2106	11	R2143	16	R4220	18	U3230	11	U4111	11
C3308	11	CR2107	11	R2144	16	R4227	17	U3230	17	U4111	18
C4101	18	CR2108	11	R2145	16	R9101	14	U3231	11	U4112	11
C4106	11	CR2109	11	R2146	16	R9102	14	U3231	17	U4112	18
C4110	11	CR2111	16	R2147	16	R9103	14	U3232	11	U4113	11
C4115	18	CR2112	16	R2148	16	R9104	14	U3232	17	U4113	18
C4118	18	CR2203	16	R2149	16	R9106	14	U3233	11	U4114	11
C4125	11			R2150	16	R9107	14	U3233	17	U4114	18
C4126	11	J2111	16	R2151	16	R9108	14	U3234	11	U4115	11
C4201	18	J2112	16	R2152	16	R9109	14	U3234	17	U4115	18
C4202	18	J4104	18	R2153	16	R9110	14	U3235	11	U4116	11
C4203	18	J6100	14	R2154	16	R9112	14	U3235	17	U4116	18
C4217	11	J6100	15	R2155	16	R9113	14	U3236	11	U4117	11
C4232	11	J6100	21	R2156	16	R9114	14	U3236	17	U4117	18
C9001	11	J8100	11	R2157	16	R9115	14	U3237	11	U4118	11
C9002	11	J8100	14	R2257	16	R9120	14	U3237	17	U4118	18
C9003	11	J9104	14	R2258	16	R9210	15	U3238	11	U4119	11
C9004	11	J9105	14	R2259	16	R9211	15	U3238	17	U4119	18
C9005	11	J9107	14	R2260	16	R9212	15	U3239	11	U4120	11
C9006	11	J9430	14	R2265	16	R9213	15	U3239	17	U4120	18
C9007	11			R2266	16	R9214	15	U3306	11	U4121	11
C9011	11	L2137	16	R2267	16	R9219	15	U3306	17	U4121	18
C9012	11	L2139	16	R2268	16	R9220	15	U3307	11	U4122	11
C9013	11			R2269	16	R9221	15	U3307	17	U4122	17
C9014	11	Q2101	16	R2270	16	R9222	15	U3308	11	U4122	18
C9015	11	Q2102	16	R2274	16	R9223	15	U3308	17	U4123	11
C9021	11	Q2103	16	R2275	16	R9224	15	U3309	11	U4123	18
C9022	11	Q2104	16	R2276	16	R9230	14	U3309	17	U4124	11
C9023	11	Q2105	16	R2277	16	R9301	14	U3310	11	U4124	18
C9024	11	Q2106	16	R2278	16	R9302	14	U3310	17	U4125	11
C9025	11	Q2107	16	R2279	16	R9401	14	U3313	11	U4125	18
C9031	11	Q2150	16	R2281	16	R9402	14	U3313	17	U4126	11

WAVEFORMS FOR DIAGRAM 14

54

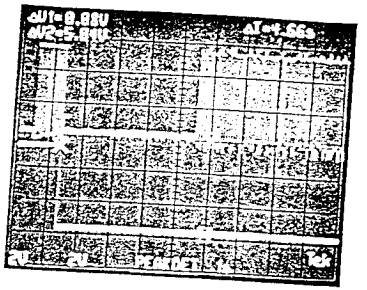


55



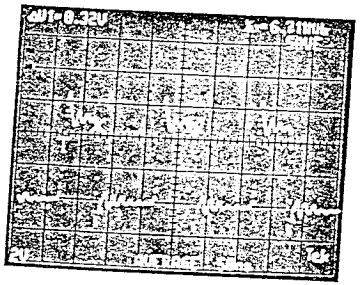
60

56



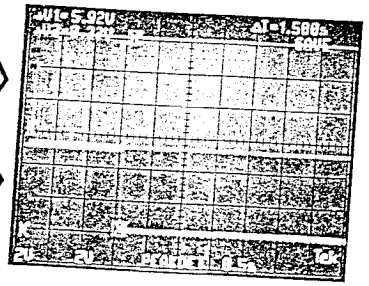
TEST SCOPE TRIGGERED ON U911 PIN 21
FOR WAVEFORMS 57 THROUGH 62.

56



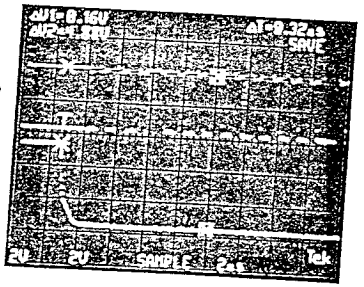
55

56



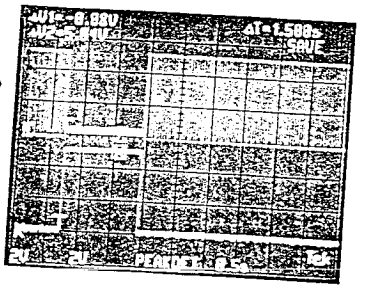
61

56



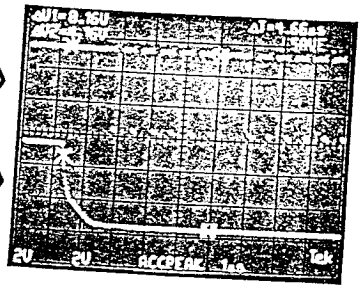
62

56



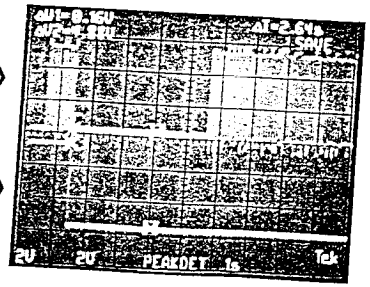
57

56



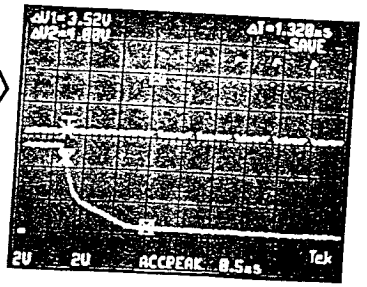
58

56



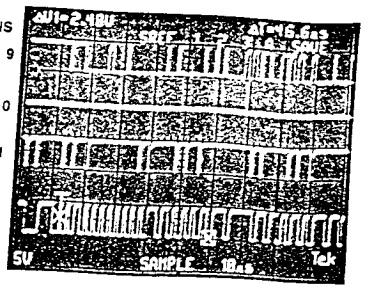
62

56

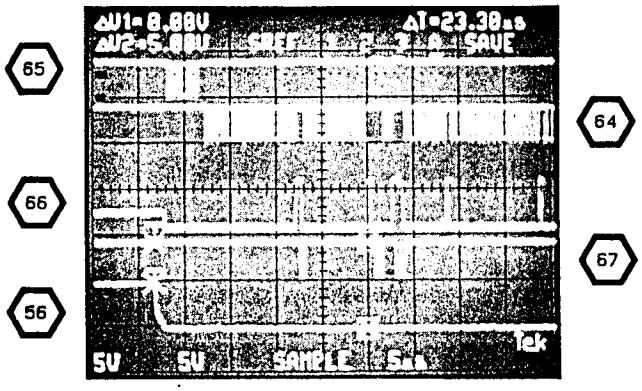


PINS
9
10
11
12

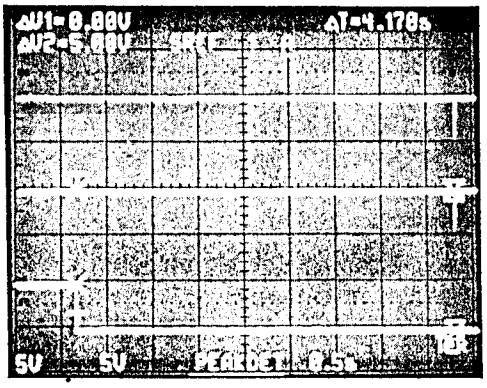
63



TEST SCOPE TRIGGERED ON U911 PIN 21
FOR WAVEFORMS 64 THROUGH 69.



65 64 66 67 56



68 69 56

MICROPROCESSOR AND STORE PANEL CONTROLS DIAGRAM 14

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C9107	4A	6E	R9110	8C	7C	U9102B	7K	7E
C9205	1M	9C	R9112	6C	7E	U9102C	4B	7E
C9206	1M	9D	R9113H	7C	4D	U9102D	6H	7E
C9410	2E	7B	R9113	4E	4D	U9103A	7B	6D
C9411	1G	7B	R9114	7B	7E	U9103B	7H	6D
			R9115	6B	7E	U9103C	6G	6D
J6100	1M	10D	R9120	8E	5E	U9103D	7H	6D
J6100	8A	10D	R9230	1M	9D	U9103E	5G	6D
J8100	3C	2D	R9301	2J	5B	U9103F	6H	6D
J8100	5M	2D	R9302	1J	4B	U9103G	8C	6D
J8100	6A	2D	R9401	2M	10C	U9103H	5H	6D
J9104	5A	6E	R9402	2M	10C	U9104	3B	6E
J9105A	7C	6D				U9105D	7K	8E
J9105B	5E	5E	S9401A	1A	5A	U9105	3J	8E
J9105C	8F	8E	S9401B	1B	5A	U9106	7G	7E
J9105D	6K	4E	S9401C	1B	5A	U9107A	7H	6D
J9107	5A	8E	S9401D	1B	5A	U9107B	6H	6D
J9430*	1M	7B	S9401E	1C	5A	U9107C	5H	6D
			S9402A	1C	8A	U9108	6C	6E
Q9100	7B	6E	S9402B	1E	8A	U9109	4J	4C
			S9402C	1E	8A	U9110	5J	4C
R9101	4B	6E	S9402D	1F	8A	U9111	3D	4E
R9102	6B	8E	S9403	1G	4B	U9112	4F	4D
R9103	8F	8E				U9113	4L	4E
R9104	5A	5E	U9101A	6F	5E	U9114	5F	5D
R9106	4B	5E	U9101B	6G	5E	U9301	2K	5B
R9107	4A	5E	U9101C	6B	5E	U9302	1K	4B
R9108	8C	7E	U9101D	6H	5E			
R9109	6E	5D	U9102A	7H	7E			

Partial A10 also shown on diagrams 11, 12, 15, 16, 17, 18 and 21.

ASSEMBLY A24*

R9412A* R9412B*	1L 2L		S9412*	2L		W9430*	2M	

CHASSIS MOUNTED PARTS

P9105C	8E	CHASSIS	P9430	1M	CHASSIS			

*See Parts List for serial number ranges.

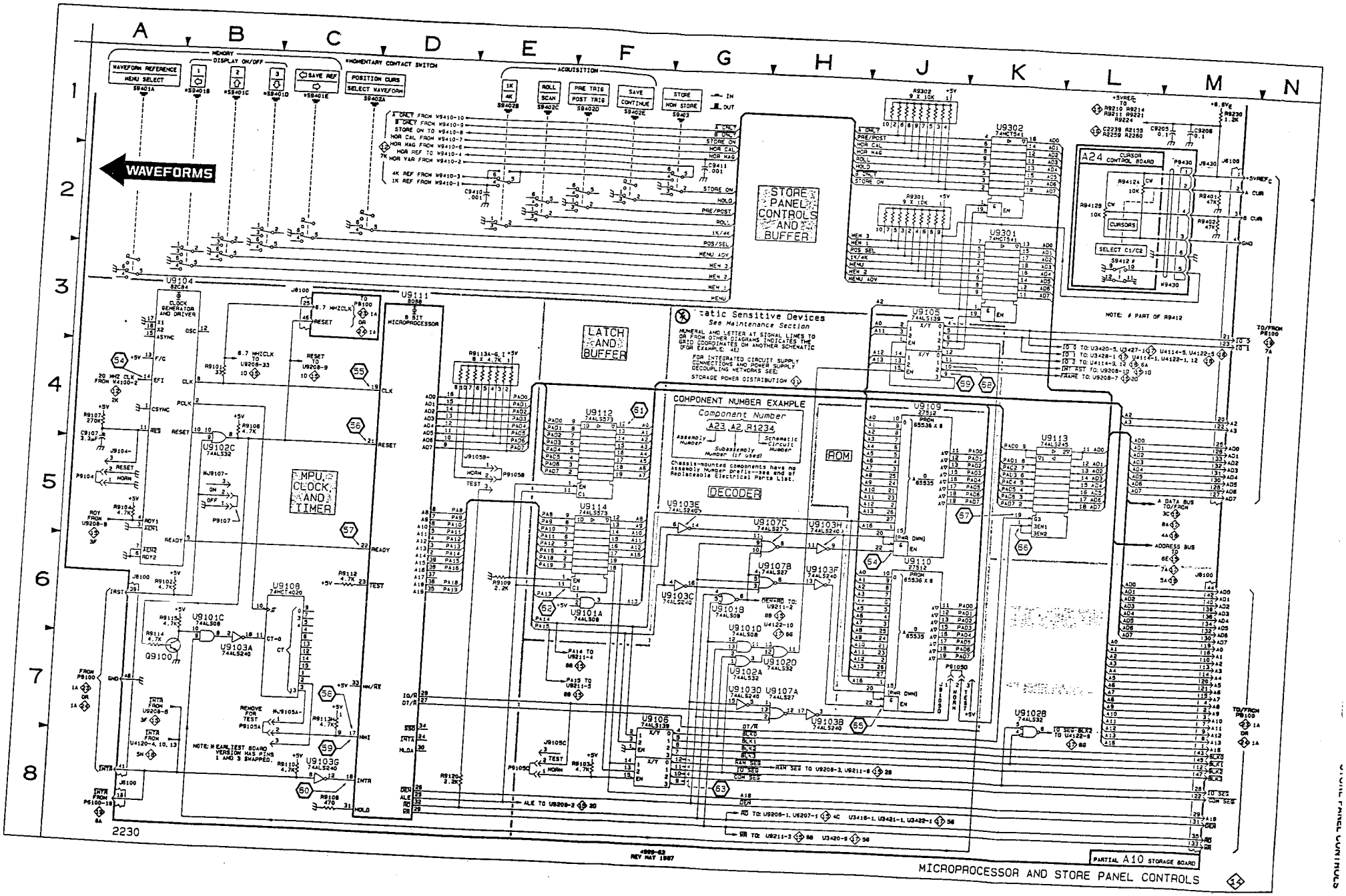
A6—LINE FILTER, A18—THERMAL

A7—INTENSITY POT

A8—ALTERNATE SWEEP

A10—STORAGE BOARD FIG. 9-21

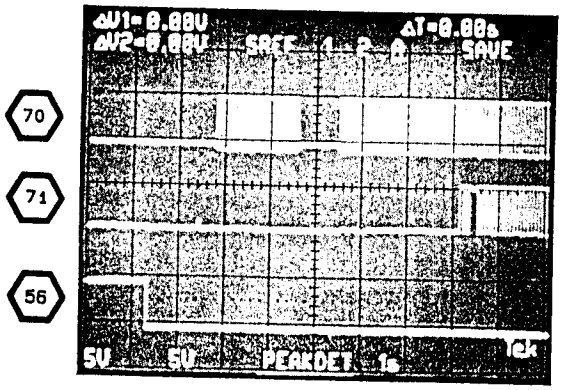
WAVEFORMS FOR DIAGRAM 14



CIRCUIT DIAGRAMS CONTINUED

WAVEFORMS FOR DIAGRAM 15

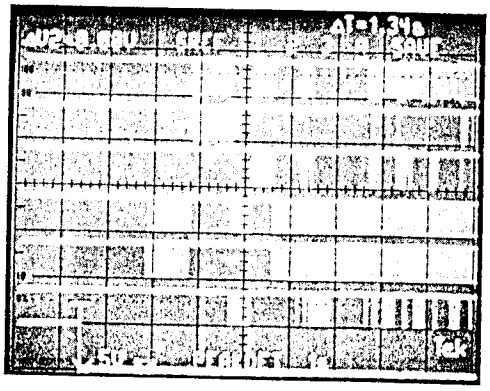
TEST SCOPE TRIGGERED ON U9111 PIN 21
FOR WAVEFORMS 70 THROUGH 77.



70

71

56



73

74

75

56

72

76

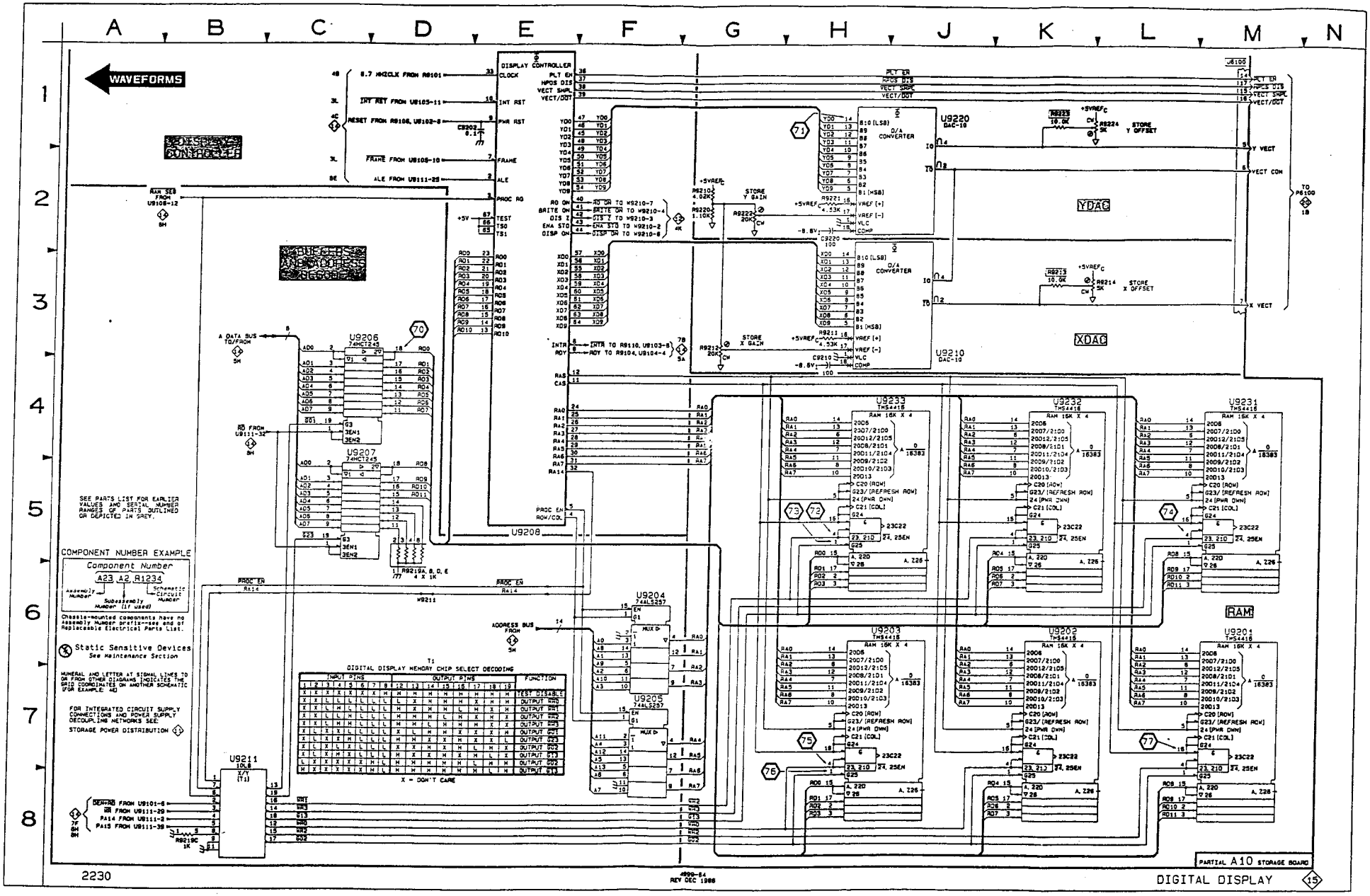
77

DIGITAL DISPLAY DIAGRAM 15

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C9202	1E	8B	R9219A	6D	7B	U9206	3C	7C
C9210	3H	9C	R9219B	6D	7B	U9207	5C	6B
C9220	2H	9D	R9219D	6D	7B	U9208	5E	8B
			R9220	2G	10C	U9210	3J	10C
J6100	1M	10D	R9221	2H	9D	U9211	8B	6C
			R9222	2G	10D	U9220	1J	10C
R9210	2G	9C	R9223	1K	10C	U9231	4M	6C
R9211	3H	9C	R9224	1L	10D	U9232	4K	8D
R9212	3G	10C				U9233	4J	7D
R9213	3K	10C	U9201	6M	7C			
R9214	3L	10C	U9202	6K	8D	W9211	6D	5C
R9219C	8B	7B	U9203	6J	7D			
			U9204	6F	5D			
			U9205	7F	5C			

Partial A10 also shown on diagrams 11, 12, 14, 16, 17, 18 and 21.

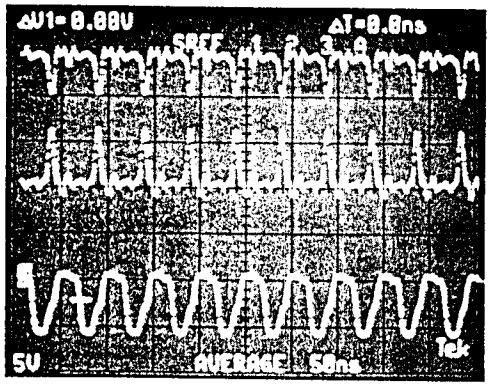


A10—STORAGE BOARD FIG. 9-21
WAVEFORMS FOR DIAGRAM 14
WAVEFORMS FOR DIAGRAM 15

WAVEFORMS FOR DIAGRAM 16

TEST SCOPE TRIGGERED AT JUNCTION OF R2265 AND R2266
FOR WAVEFORMS 81 THROUGH 86.

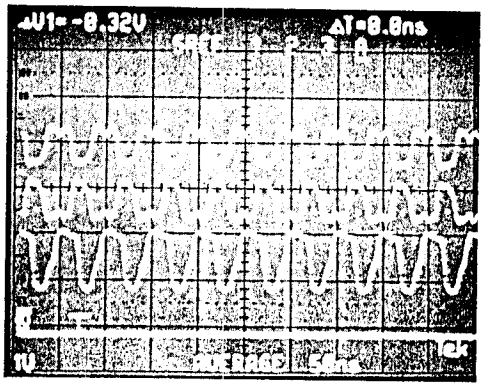
80



79

78

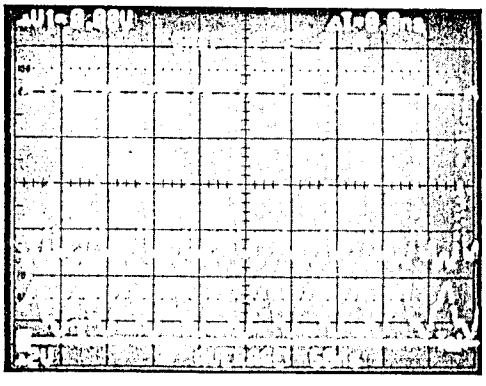
81



82

78

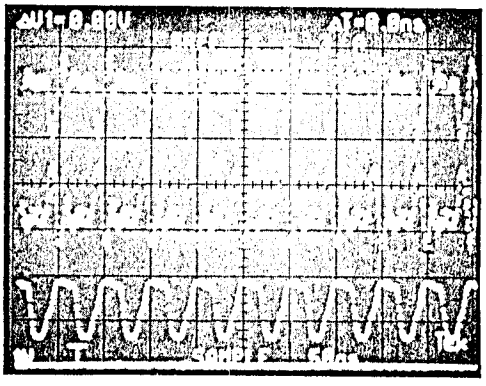
84



83

78

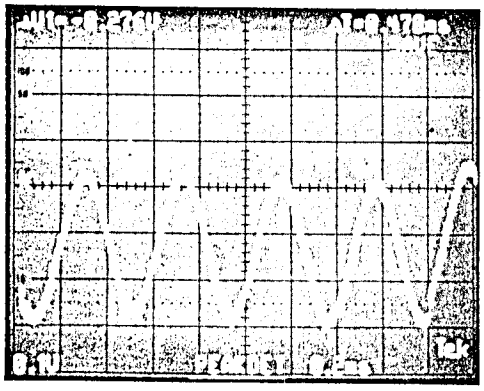
86



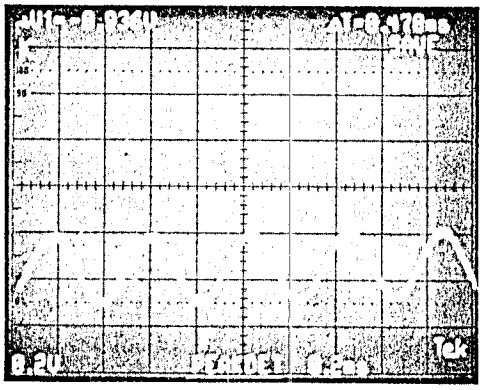
85

78

87



88



STORAGE ACQUISITION DIAGRAM 16

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2101	2C	1G
C2102	2C	1G
C2103	2C	2G
C2104	4D	3G
C2111	4C	4G
C2112	4C	4G
C2113	4C	3G
C2114	2D	2G
C2115	4B	3F
C2116	2B	2F
C2119	6D	3H
C2120	5F	3H
C2151	2G	2H
C2152	2H	2H
C2153	3H	1H
C2224	7D	3L
C2225	7E	2L
C2226	5J	1J
C2228	7H	1K
C2229	4H	1H
C2230	4J	1H
C2233	4G	2J
C2235	2J	2H
C2236	1J	2J
C2237	2K	2J
C2238	4H	2J
C2239	6F	3J
C2241	8K	2K
C2242	3J	2J
CR2101	5D	1G
CR2102	5D	1H
CR2103	5C	3H
CR2104	5C	3H
CR2111	2D	1G
CR2112	4D	3G
CR2203	1J	2H
J2111	2A	2G
J2112	3A	3G
L2137	3F	2H
L2139	3F	2H
Q2101	3F	2H
Q2102	4F	2H
Q2103	4G	3H
Q2104	5G	3H
Q2105	2G	2H
Q2106	2H	2H
Q2107	3H	1H
Q2150	1H	3J
Q2207	7H	1J
Q2208	7J	1J
Q2209A	2J	2J
Q2209B	2J	2J
Q2211	3K	2J
Q2212	2K	2J
Q2213	6G	3J
R2101	4B	3G
R2102	3B	3G
R2104	3C	4G
R2105	4C	3G
R2106	3C	3G
R2107	3D	3G
R2108	4D	3G
R2109	4B	3F
R2110	2B	2F
R2111	2B	2G
R2112	2B	2G
R2114	2C	1G
R2115	2C	2G
R2116	3C	2G
R2117	2D	2G
R2118	2D	2G
R2119	2D	2F
R2120	2B	2G
R2121	2B	2G
R2122	2B	2G
R2123	4B	3G
R2124	3B	3G
R2125	4B	3G
R2126	5D	2G
R2127	5D	1G
R2128	4C	4H
R2129	5C	3H
R2130	4D	3F
R2131	3F	1H
R2133	6D	3H
R2137	4F	2H
R2138	3F	1H
R2139	3F	2H
R2140	3F	2H
R2141	3F	2H
R2143	5F	3H
R2144	5F	3H
R2145	5G	3H
R2146	4F	3H
R2147	3G	2H
R2148	2G	2H
R2149	1G	2H
R2150	2H	2H
R2151	2H	2H
R2152	2H	2H
R2153	2H	1H
R2154	3H	1J
R2155	1F	3J
R2156	1G	3J
R2157	1G	3J
R2257	6G	3J
R2258	6G	3J
R2259	6G	3J
R2260	6G	3J
R2265	7D	3L
R2266	1J	3L
R2266	7D	3L
R2267	8D	2K
R2268	8D	2L
R2269	8F	3K
R2270	7E	2L
R2274	7H	1J
R2275	7H	1J
R2276	7J	1J
R2277	7H	1K
R2278	7H	1K
R2279	5J	2J
R2281	4J	2H
R2286	1J	2J
R2287	2J	2J
R2289	3J	2J
R2290	3J	3J
R2291	3K	2J
R2292	2K	2J
R2293	2K	2J
R2295	3L	3J
R2296	7K	2K
R2297	7K	2K
RT2101	4C	3G
RT2102	4D	2F
RT2103	4C	4G
RT2111	2C	2G
RT2112	2D	2F
RT2113	2C	1G
RT2131	4F	2H
RT2132	1G	2H
T2201	5J	1H
T2202	6H	1J
T2203	3J	2H
U2101	1E	2G
U2202A	1G	3J
U2202B	6G	3J
U2203A	7F	3L
U2203B	7F	3L
U2203C	8E	3L
U2204	1L	3K
U2205	2M	3K
U2206	3M	3K
W2101	1H	3H
W2103	5C	4F

Partial A10 also shown on diagrams 11, 12, 14, 15, 17, 18 and 21.

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

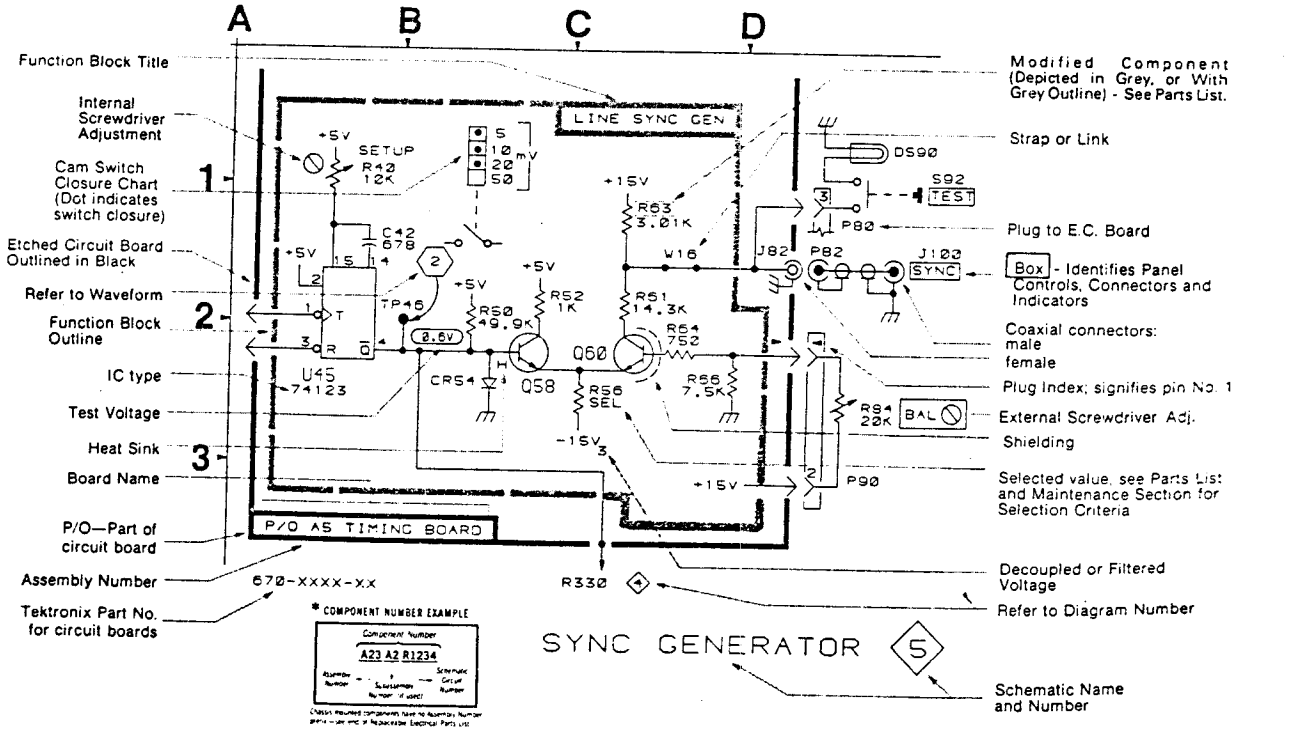
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

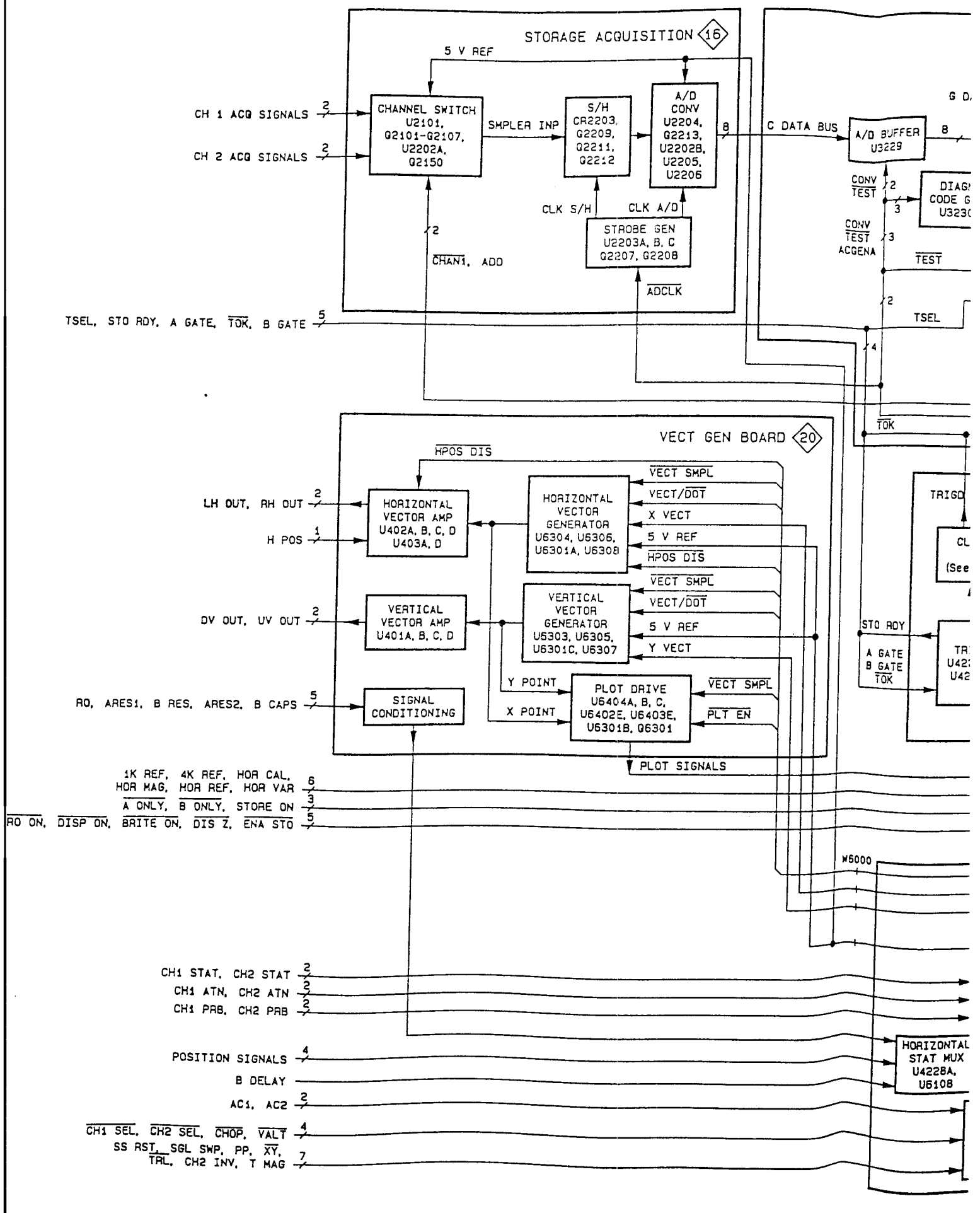
The information and special symbols below may appear in this manual.

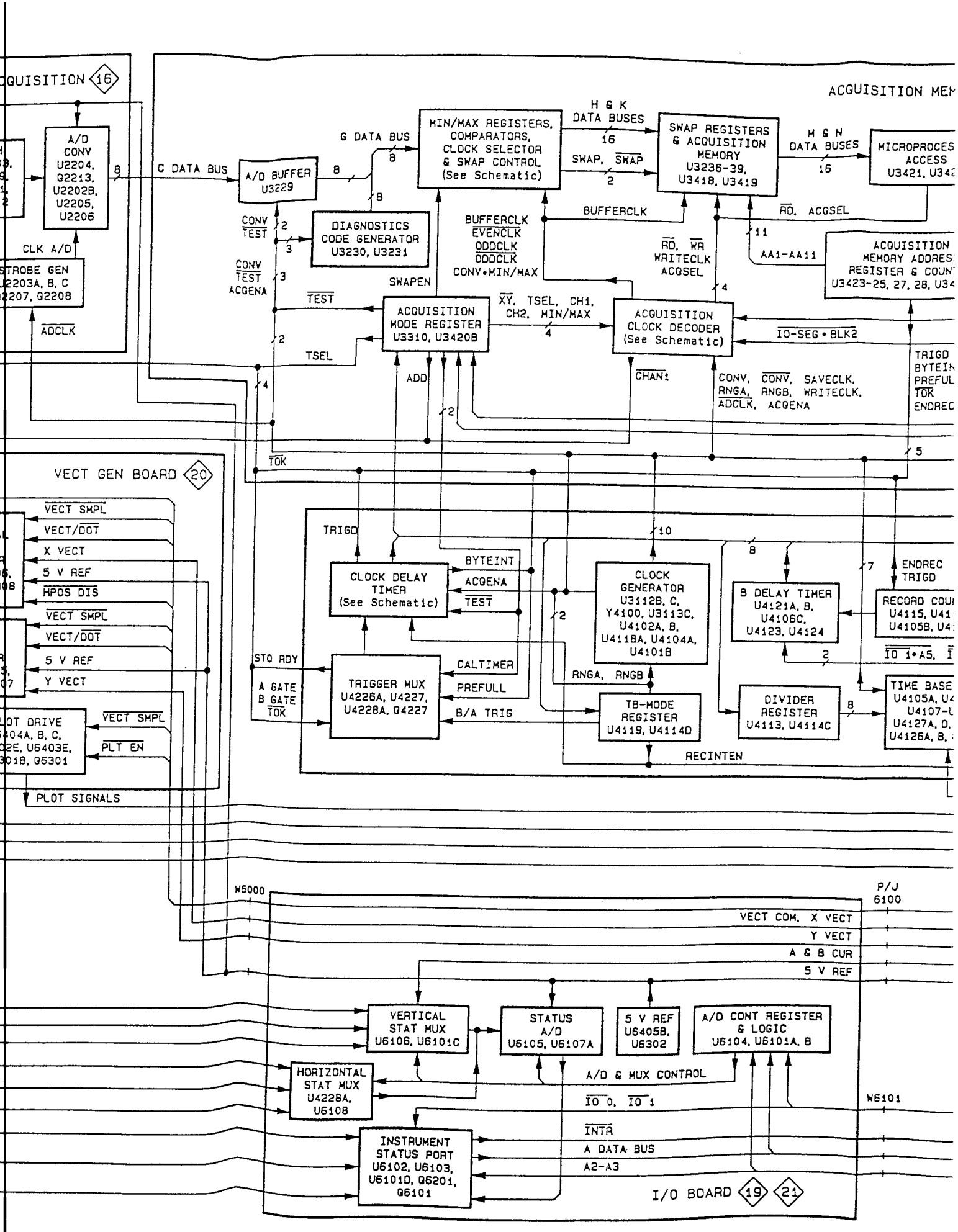
Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.




STORAGE ACQUISITION 16
5 V REF
CH 1 ACQ SIGNALS
CH 2 ACQ SIGNALS
CHANNEL SWITCH U2101, Q2101-Q2107, U2202A, Q2150
SMPLER INP
S/H CR2203, Q2209, Q2211, Q2212
A/D CONV U2204, Q2213, U2202B, U2205, U2206
C DATA BUS
A/D BUFFER U3229
CLK S/H
CLK A/D
STROBE GEN U2203A, B, C Q2207, Q2208
CHAN1, ADD
ADCLK
CONV TEST
CONV TEST ACQENA
TEST
TSEL
TSEL, STO RDY, A GATE, TOK, B GATE
TOK
VECT GEN BOARD 20
HPOS DIS
LH OUT, RH OUT
H POS
HORIZONTAL VECTOR AMP U402A, B, C, D U403A, D
HORIZONTAL VECTOR GENERATOR U6304, U6306, U6301A, U6308
VECT SMPL
VECT/DOT
X VECT
5 V REF
HPOS DIS
DV OUT, UV OUT
VERTICAL VECTOR AMP U401A, B, C, D
VERTICAL VECTOR GENERATOR U6303, U6305, U6301C, U6307
Y VECT
RO, ARES1, B RES, ARES2, B CAPS
SIGNAL CONDITIONING
Y POINT
X POINT
PLOT DRIVE U6404A, B, C, U6402E, U6403E, U6301B, Q6301
PLT EN
PLOT SIGNALS
STO RDY
A GATE
B GATE
TOK
1K REF, 4K REF, HOR CAL, HOR MAG, HOR REF, HOR VAR
A ONLY, B ONLY, STORE ON
RO ON, DISP ON, BRITE ON, DIS Z, ENA STO
W6000
CH1 STAT, CH2 STAT
CH1 ATN, CH2 ATN
CH1 PRB, CH2 PRB
POSITION SIGNALS
B DELAY
AC1, AC2
CH1 SEL, CH2 SEL, CHOP, VALT
SS RST, SGL SWP, PP, XY, TRL, CH2 INV, T MAG
HORIZONTAL STAT MUX U4228A, U6108


ACQUISITION MEM
A/D CONV U2204, G2213, U2202B, U2205, U2206
CLK A/D
STROBE GEN U2203A, B, C U2207, G2208
ADCLK
C DATA BUS
A/D BUFFER U3229
G DATA BUS
MIN/MAX REGISTERS, COMPARATORS, CLOCK SELECTOR & SWAP CONTROL (See Schematic)
H G K DATA BUSES
SWAP, SWAP
SWAP REGISTERS & ACQUISITION MEMORY U3236-39, U3418, U3419
H G N DATA BUSES
MICROPROCES ACCESS U3421, U342
CONV TEST
CONV TEST ACQENA
DIAGNOSTICS CODE GENERATOR U3230, U3231
BUFFERCLK
EVENCLK
ODDCLK
ODDCLK
CONV•MIN/MAX
SWAPEN
RD, ACQSEL
RD, WR WRITECLK ACQSEL
AA1-AA11
ACQUISITION MEMORY ADDRES REGISTER & COUN U3423-25, 27, 28, U34
TEST
ACQUISITION MODE REGISTER U3310, U3420B
XY, TSEL, CH1, CH2, MIN/MAX
ACQUISITION CLOCK DECODER (See Schematic)
IO-SEG • BLK2
TSEL
ADD
CHAN1
CONV, CONV, SAVECLK, RNGA, RNGB, WRITECLK, ADCLK, ACQENA
TRIGD
BYTEIN
PREFUL
TOK
ENDREC
TOK
VECT GEN BOARD 20
VECT SMPL
VECT/DOT
X VECT
5 V REF
HPOS DIS
VECT SMPL
VECT/DOT
5 V REF
Y VECT
PLT EN
PLOT SIGNALS
TRIGD
BYTEINT
ACQENA
TEST
CLOCK DELAY TIMER (See Schematic)
CLOCK GENERATOR U3112B, C, Y4100, U3113C, U4102A, B, U4118A, U4104A, U4101B
B DELAY TIMER U4121A, B, U4106C, U4123, U4124
ENDREC TRIGD
RECORD COU U4115, U41 U4105B, U4
IO 1•A5,
STO RDY
A GATE
B GATE
TOK
TRIGGER MUX U4226A, U4227, U4228A, Q4227
CALTIMER
PREFULL
B/A TRIG
RNGA, RNGB
TB-MODE REGISTER U4119, U4114D
DIVIDER REGISTER U4113, U4114C
TIME BASE U4105A, U4 U4107-L U4127A, D, U4126A, B,
RECINTEN
W5000
P/J 6100
VECT COM, X VECT
Y VECT
A & B CUR
5 V REF
VERTICAL STAT MUX U6106, U6101C
STATUS A/D U6105, U6107A
5 V REF U6405B, U6302
A/D CONT REGISTER & LOGIC U6104, U6101A, B
HORIZONTAL STAT MUX U4228A, U6108
A/D & MUX CONTROL
IO 0, IO 1
W6101
INSTRUMENT STATUS PORT U6102, U6103, U6101D, Q6201, Q6101
INTR
A DATA BUS
A2-A3
I/O BOARD 19 21

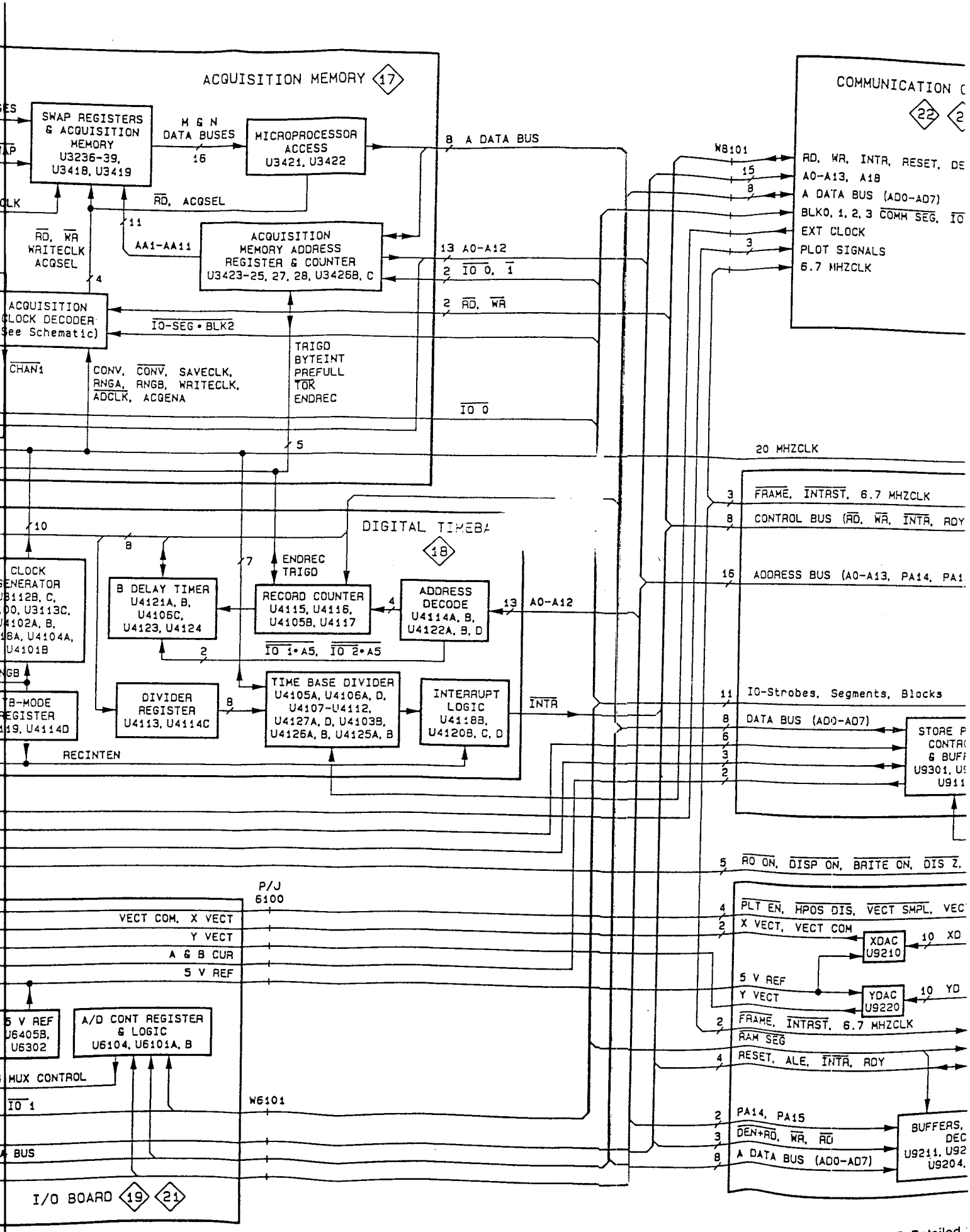


Figure 9-5. Detailed

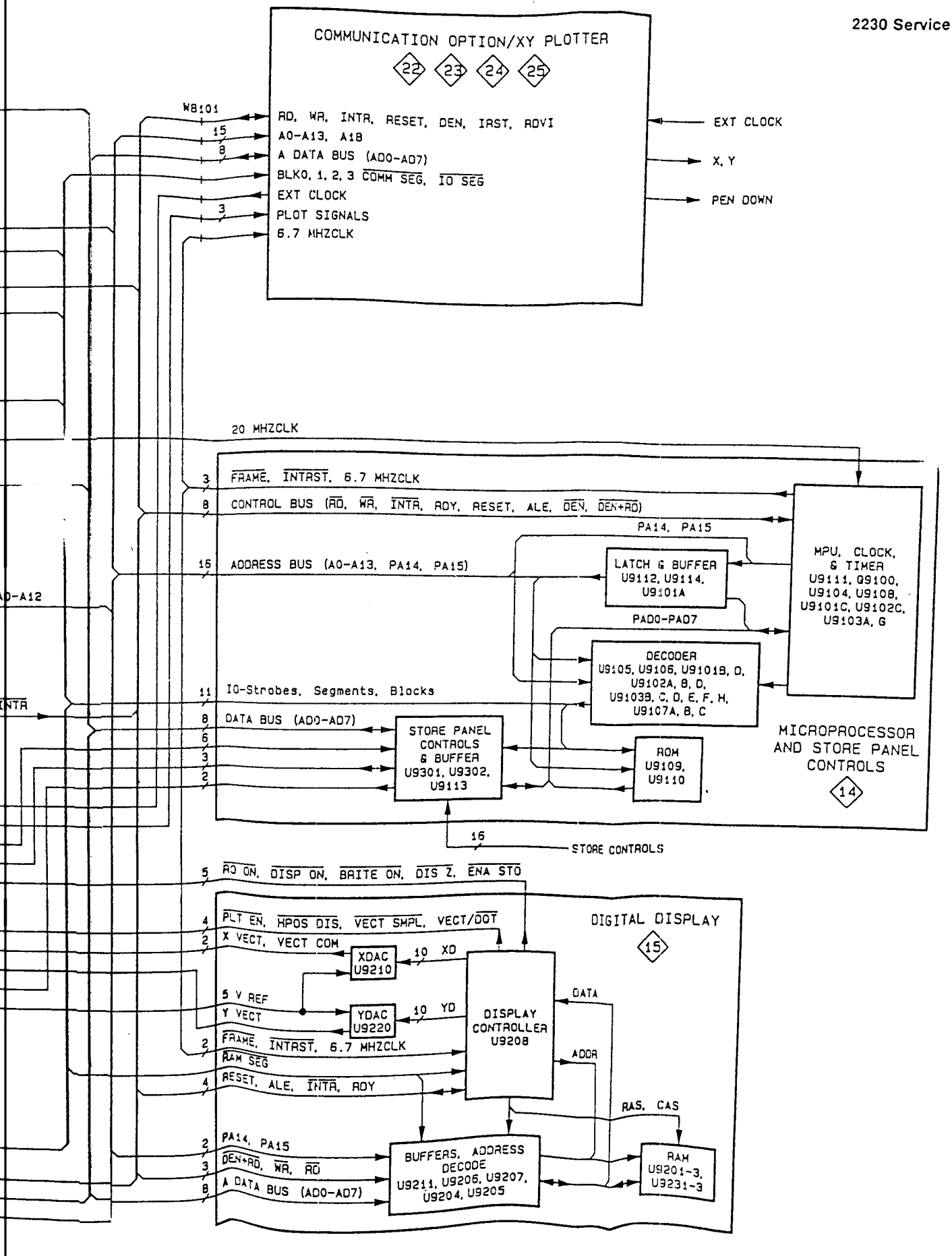
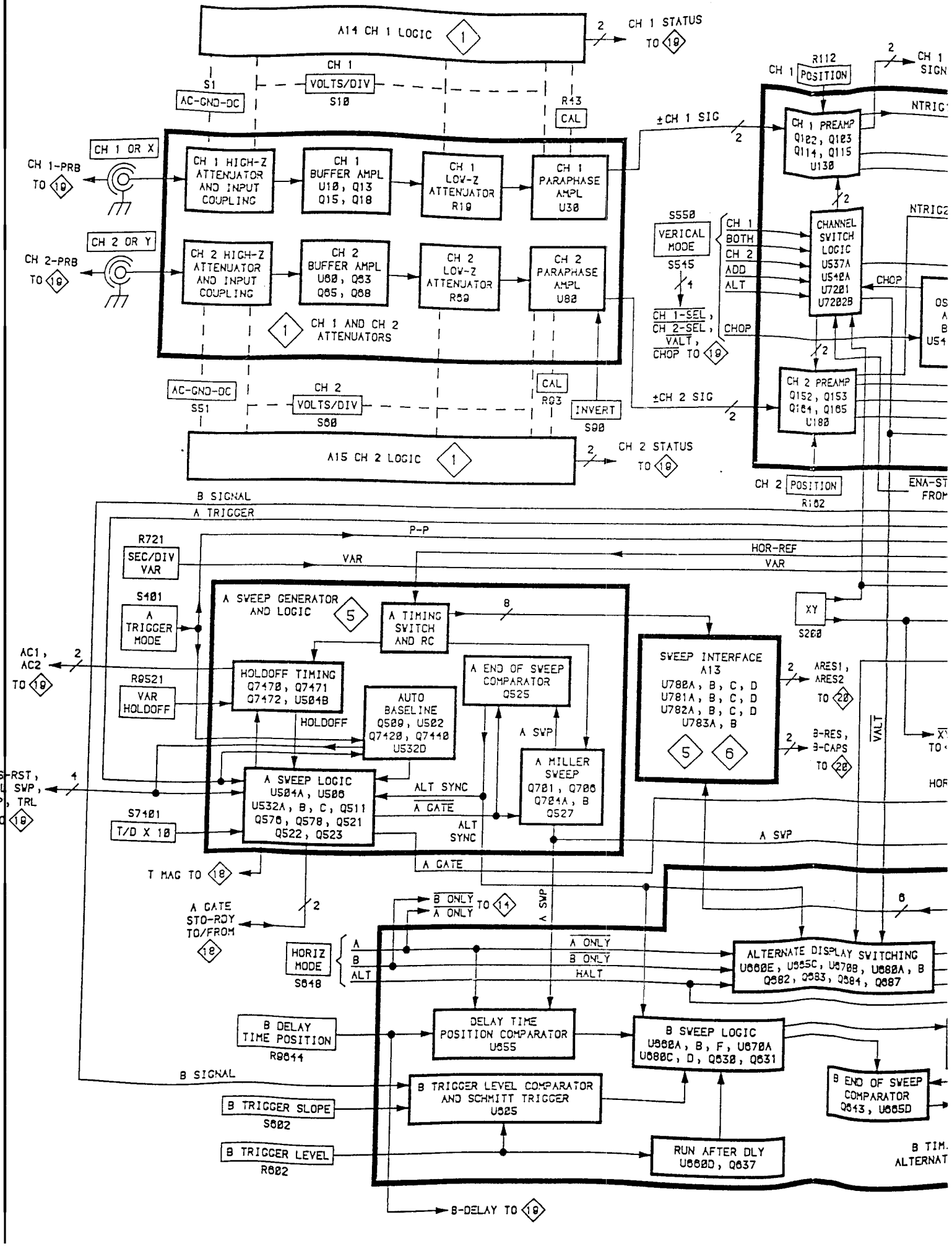


Figure 9-5. Detailed Storage block diagram.

4999-22


A14 CH 1 LOGIC
CH 1 STATUS
TO 18
CH 1
VOLTS/DIV
S10
S1
AC-GND-DC
R43
CAL
CH 1 OR X
CH 1-PRB
TO 19
CH 1 HIGH-Z ATTENUATOR AND INPUT COUPLING
CH 1 BUFFER AMPL U10, Q13 Q15, Q18
CH 1 LOW-Z ATTENUATOR R19
CH 1 PARAPHASE AMPL U30
±CH 1 SIG
CH 1 PREAMP Q102, Q103 Q114, Q115 U130
R112
CH 1 POSITION
CH 2 OR Y
CH 2-PRB
TO 19
CH 2 HIGH-Z ATTENUATOR AND INPUT COUPLING
CH 2 BUFFER AMPL U60, Q63 Q65, Q68
CH 2 LOW-Z ATTENUATOR R59
CH 2 PARAPHASE AMPL U80
CH 1 AND CH 2 ATTENUATORS
S550
VERICAL MODE
S545
CH 1
BOTH
CH 2
ADD
ALT
CHOP
CH 1-SEL, CH 2-SEL, VALT, CHOP TO 19
CHANNEL SWITCH LOGIC U537A U540A U7201 U7202B
CH 2
VOLTS/DIV
S60
S51
AC-GND-DC
CAL
R93
INVERT
S90
±CH 2 SIG
CH 2 PREAMP Q152, Q153 Q164, Q165 U180
R182
CH 2 POSITION
A15 CH 2 LOGIC
CH 2 STATUS
TO 18
B SIGNAL
A TRIGGER
P-P
VAR
HOR-REF
VAR
R721
SEC/DIV VAR
S401
A TRIGGER MODE
A SWEEP GENERATOR AND LOGIC
A TIMING SWITCH AND RC
XY
S260
AC1, AC2
TO 19
R9521
VAR HOLDOFF
HOLDOFF TIMING Q7470, Q7471 Q7472, U504B
AUTO BASELINE Q509, U502 Q7420, Q7440 U532D
A END OF SWEEP COMPARATOR Q525
A SWP
A MILLER SWEEP Q701, Q706 Q704A, B Q527
SWEEP INTERFACE A13 U780A, B, C, D U781A, B, C, D U782A, B, C, D U783A, B
ARES1, ARES2
TO 28
B-RES, B-CAPS
TO 28
VALT
S-RST, L SWP, TRL
TO 19
A SWEEP LOGIC U504A, U506 U532A, B, C, Q511 Q576, Q578, Q521 Q522, Q523
ALT SYNC
A GATE
ALT SYNC
S7401
T/D X 10
T MAG TO 18
A GATE
A SWP
A GATE STO-RDY TO/FROM 18
B ONLY TO 14
A ONLY
A SWP
HORIZ MODE
S648
A
B
ALT
A ONLY
B ONLY
HALT
ALTERNATE DISPLAY SWITCHING U660E, U655C, U670B, U680A, B Q682, Q683, Q684, Q687
B DELAY TIME POSITION
R9644
DELAY TIME POSITION COMPARATOR U655
B SWEEP LOGIC U660A, B, F, U670A U680C, D, Q638, Q631
B SIGNAL
B TRIGGER LEVEL COMPARATOR AND SCHMITT TRIGGER U625
B END OF SWEEP COMPARATOR Q643, U665D
B TRIGGER SLOPE
S602
B TRIGGER LEVEL
R602
RUN AFTER DLY U660D, Q637
B TIM. ALTERNAT
B-DELAY TO 19

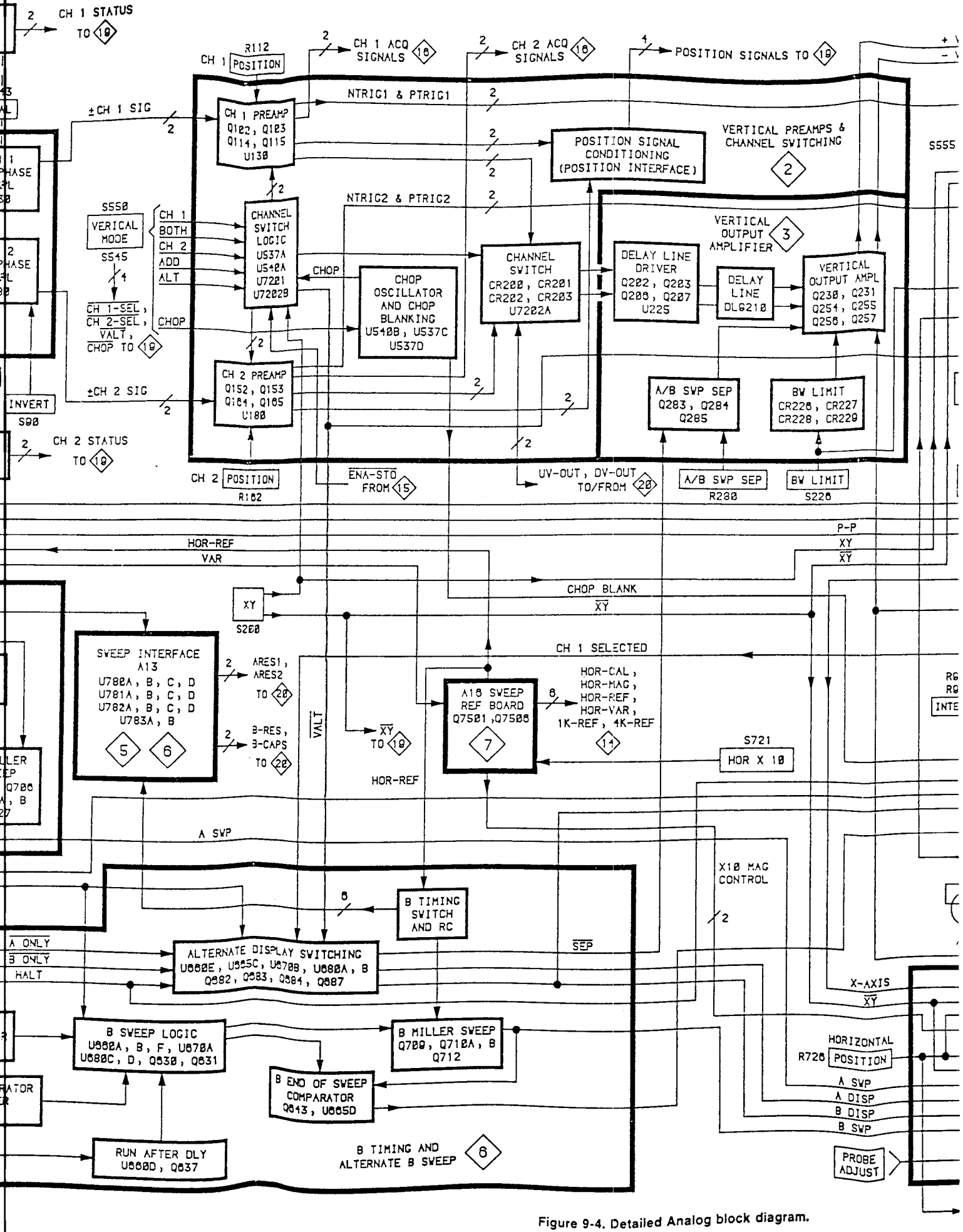
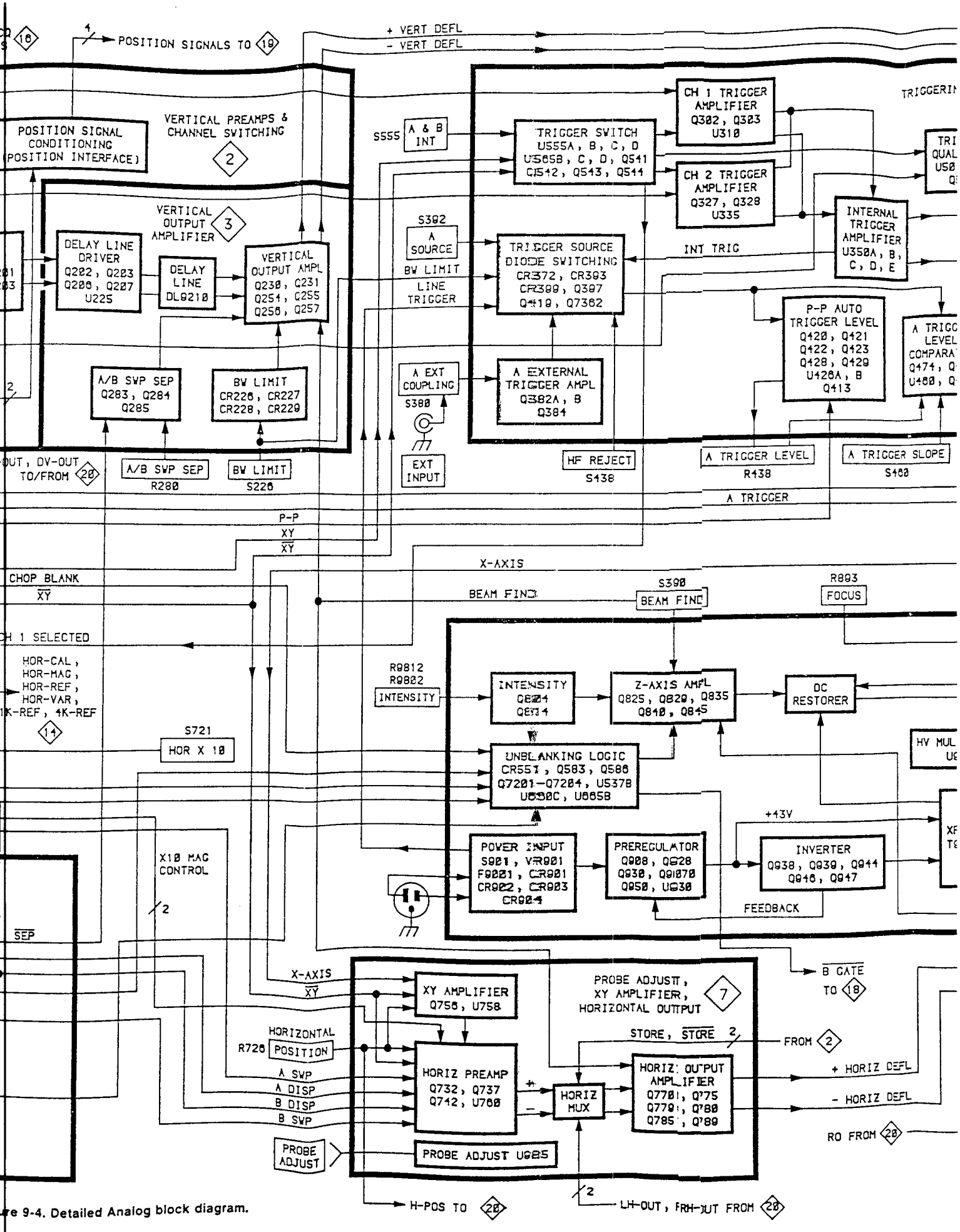
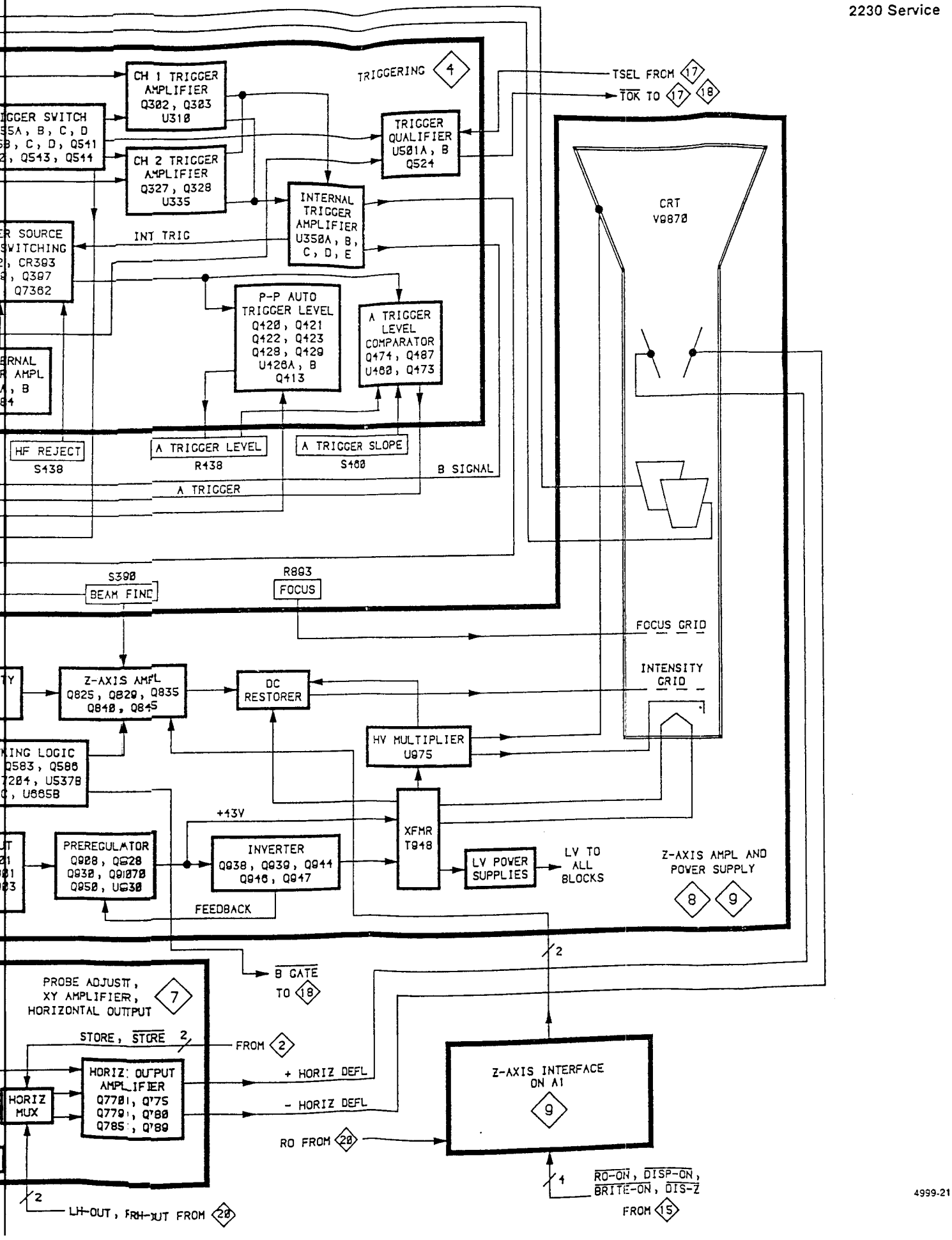


Figure 9-4. Detailed Analog block diagram.



re 9-4. Detailed Analog block diagram.


TRIGGERING 4
CH 1 TRIGGER AMPLIFIER Q302, Q303 U310
CH 2 TRIGGER AMPLIFIER Q327, Q328 U335
TRIGGER QUALIFIER U501A, B Q524
INTERNAL TRIGGER AMPLIFIER U350A, B, C, D, E
INT TRIG
P-P AUTO TRIGGER LEVEL Q420, Q421 Q422, Q423 Q428, Q429 U426A, B Q413
A TRIGGER LEVEL COMPARATOR Q474, Q487 U480, Q473
TSEL FROM 17
TOK TO 17 18
CRT V9870
HF REJECT S438
A TRIGGER LEVEL R438
A TRIGGER SLOPE S480
B SIGNAL
A TRIGGER
S390 BEAM FIND
R893 FOCUS
FOCUS GRID
INTENSITY GRID
Z-AXIS AMPL Q825, Q829, Q835 Q840, Q845
DC RESTORER
HV MULTIPLIER U975
+43V
XFMR T948
PREREGULATOR Q908, Q928 Q930, Q1070 Q950, U930
INVERTER Q938, Q939, Q944 Q946, Q947
LV POWER SUPPLIES
LV TO ALL BLOCKS
Z-AXIS AMPL AND POWER SUPPLY 8 9
FEEDBACK
B GATE TO 18
PROBE ADJUST, XY AMPLIFIER, HORIZONTAL OUTPUT 7
STORE, STORE 2
FROM 2
HORIZ MUX
HORIZ OUTPUT AMPLIFIER Q778, Q775 Q779, Q780 Q785, Q789
+ HORIZ DEFL
- HORIZ DEFL
Z-AXIS INTERFACE ON A1 9
RO FROM 20
RO-ON, DISP-ON, BRITE-ON, DIS-Z
FROM 15
LH-OUT, RH-OUT FROM 20

4999-21

To identify any component mounted on a circuit board and to locate that component in the appropriate schematic diagram

1. Locate the Circuit Board Illustration.

   a. Identify the particular circuit board that the component is located on by using the Circuit Board Location illustration (Figure 9-5) to determine the Assembly Number.

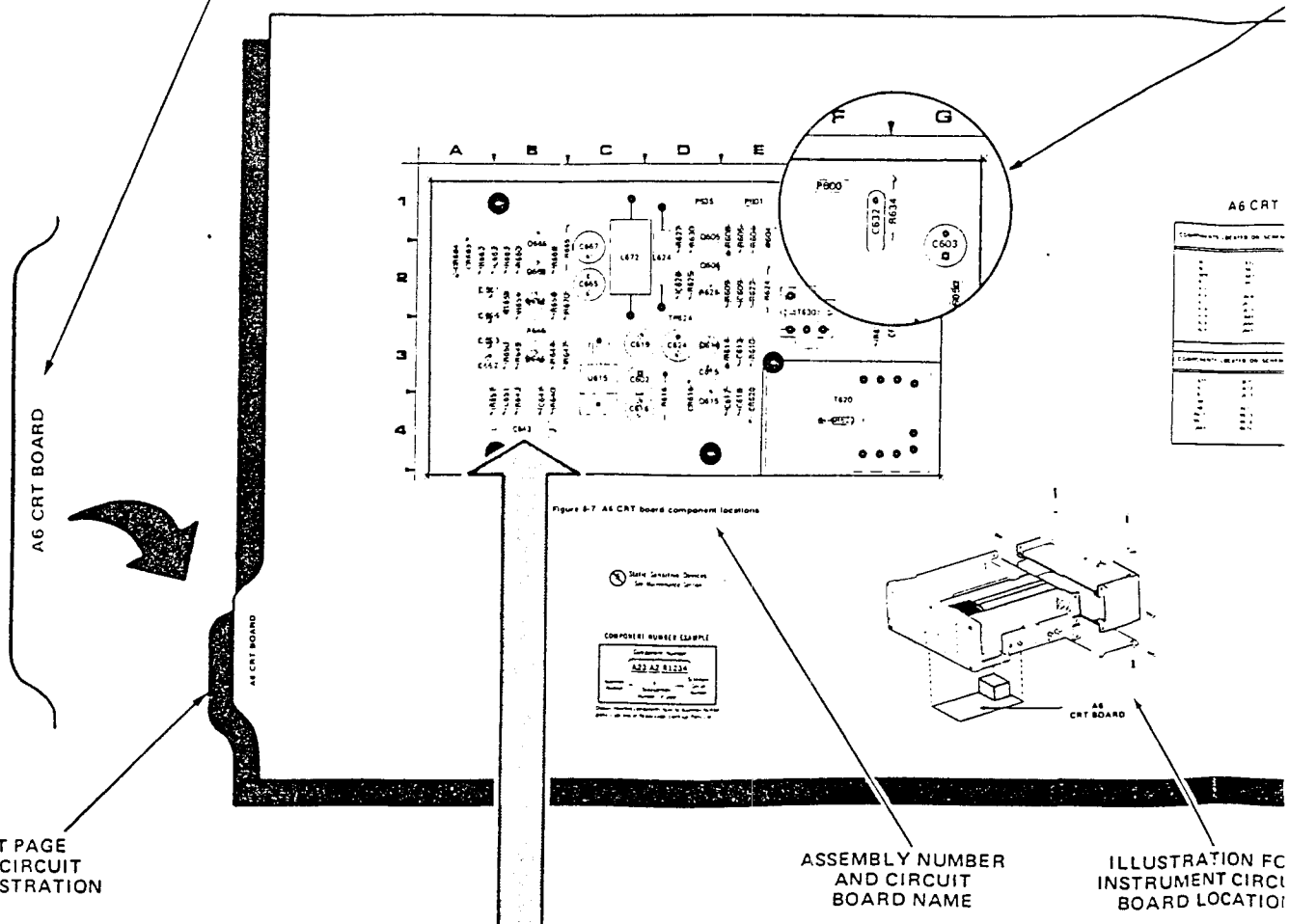
   b. In the manual locate and pull out tabbed page whose title corresponds with the Assembly Number of the circuit board. Circuit board assembly numbers and board nomenclature are printed on the back side of the tabs (facing the rear of the manual).

2. Determine the Circuit Numbe

   a. Compare the circuit board the desired component by tion.

   b. Scan the table adjacent to th find the Circuit Number of

   c. Determine the Schematic component is located.



4. Determine the Circuit Board Illustration and Component Location

   a. From the schematic diagram, determine the Assemt Number of the circuit board on which the component mounted. This information is boxed and located in a corr of the heavy line that distinguishes the board outline.

   b. Scan the Component Location Table for the Assemt Number just determined and find the Circuit Number of t desired component.

   c. Under the BOARD LOCATION column, read the gr coordinates for the desired component.

5. Locate the Component on the Circuit Board

   a. In the manual, locate and pull out the tabbed page whose title and Assembly Number correspond with the desired circuit board. This information is on the back side of the tabs.

   b. Using the Circuit Number and grid coordinates, locate the component on the Circuit Board Illustration.

   c. In the circuit board location illustration, determine the location of the circuit board in the instrument.

   d. Find the circuit board in the instrument and compare it with its illustration in the manual to locate the desired component on the board.

Figure 9-3. Locating components on schematic diagrams and

mponent is
Location
Assembly

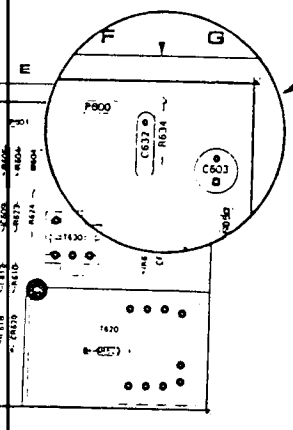
whose title
the circuit
and board
the tabs

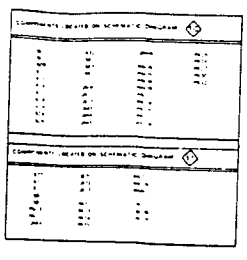
2. Determine the Circuit Number

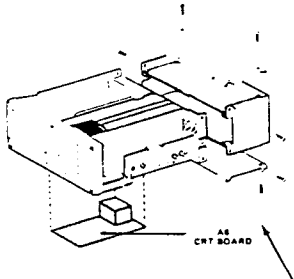
a. Compare the circuit board with its illustration and locate the desired component by area and shape on the illustration.

b. Scan the table adjacent to the Circuit Board Illustration and find the Circuit Number of the desired component.

c. Determine the Schematic Diagram Number in which the component is located.







ASSEMBLY NUMBER AND CIRCUIT BOARD NAME

ILLUSTRATION FOR INSTRUMENT CIRCUIT BOARD LOCATION

MANUAL BINDER

A6 CRT BOARD

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 10

C602	C632	Q668	R625
C603	C641		R626
C609	C643	R604	R627
C671	C651	R605	R630
C615		R608	R632
C616	Q606	R609	
C617	Q610	R610	
C618	Q615	R614	
C619	Q645	R616	
C624	Q656	R623	
C626	Q665	R624	

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 11

C670	Q670	R677
C671	Q672	R679
C673	Q673	R680
C680		
C681	R671	U617
P603	R673	U618
P607	R674	U619
Q669	R675	

CRT CIRCUIT DIAGRAM 10

A6 ASSEMBLY

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION
C602	2C	3C	Q656	2F
C603	1C	1G	Q665	1G
C609	4E	2E	Q668	2G
C612	7C	3E		
C615	7C	3D	R604	4C
C616	2C	3C	R605	5D
C617	7D	3D	R608	4E
C618	7E	3E	R609	4E
C619	6E	3C	R610	7B
C624	4F	3D	R614	7C
C626	7G	2D	R616	1C
C632	8G	1E	R623	4D
C643	3D	4B	R625	7F
C651	3E	3B	R627	7F
		3B	R630	7G
				4E
Q606	4E	2D		
Q610	7C	3D	TP624	3B
Q615	7D	3D		
Q645	3E	3B	U615	1D

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION
L635	5I	CHASSIS	V635	6J

Determine the Circuit Board Illustration and Component tion

From the schematic diagram, determine the Assembly Number of the circuit board on which the component is mounted. This information is boxed and located in a corner of the heavy line that distinguishes the board outline.

Scan the Component Location Table for the Assembly Number just determined and find the Circuit Number of the desired component.

Under the BOARD LOCATION column, read the grid coordinates for the desired component.

3. Locating components on schematic diagrams and circuit board illustrations.

3. Locate the Component on the Schematic Diagram

a. Locate and pull out tabbed page whose number ar correspond with the Schematic Diagram Numbe determined in the table. Schematic diagram nomenc and numbers are printed on the front side of th (facing the front of the manual).

b. Scan the Component Location Table adjacent t schematic diagram and find the Circuit Number desired component.

A6 CRT BOARD

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 10

C602 C603 C609 C671 C615 C616 C617 C618 C619 C624 C626	C632 C641 C643 C651 Q606 Q610 Q615 Q645 Q656 Q665	Q668 R604 R605 R608 R609 R610 R614 R616 R623 R624	R625 R626 R627 R630 R632

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 11

C670 C671 C673 C680 C681 P603 P607 Q669	Q670 Q672 Q673 R671 R673 R674 R675	R677 R679 R680 U617 U618 U619	

COMPONENT LOCATION TABLE

CRT CIRCUIT DIAGRAM 10

CRT CIRCUIT DIAGRAM 10

A6 ASSEMBLY

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C602	2C	3C	Q656	2F	2B
C603	1C	1G	Q665	1G	1B
C609	4E	[illegible]	Q668	2G	2B
C612	7C	3E			
C615	7C	3D	R604	4C	1E
C616	2C	3C	R605	5D	1E
C617	7D	3D	R608	4E	1D
C618	7E	3E	R609	4E	2D
C619	6E	3C	R610	7B	3E
C624	4F	3D	R614	7C	3D
C626	7G	2D	R616	1C	3D
C632	8G	1E	R623	4D	2E
C643	3D	4B	R625	7F	2D
C651	3E	3B	[illegible]	7F	2D
		3B	R627	7G	1D
			R630	4E	[illegible]
C609	4E	2D			
Q606	7C	3D	TP624	3B	2D
Q610	7D	3D			
Q615	3E	3B	U615	1D	3C
Q645					

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L635	5I	CHASSIS	V635	6J	CHASSIS

MANUAL BINDER

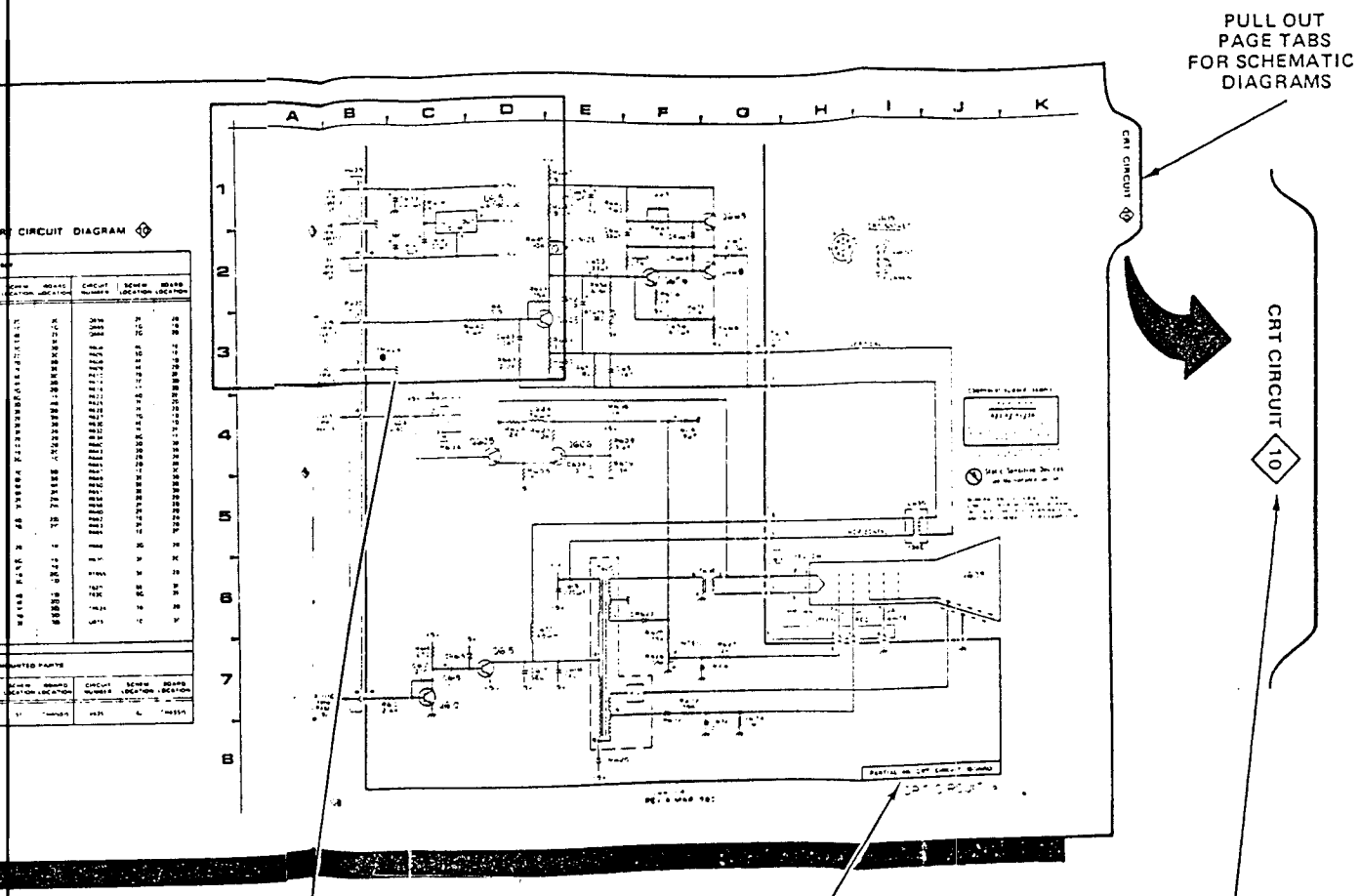
3. Locate the Component on the Schematic Diagram

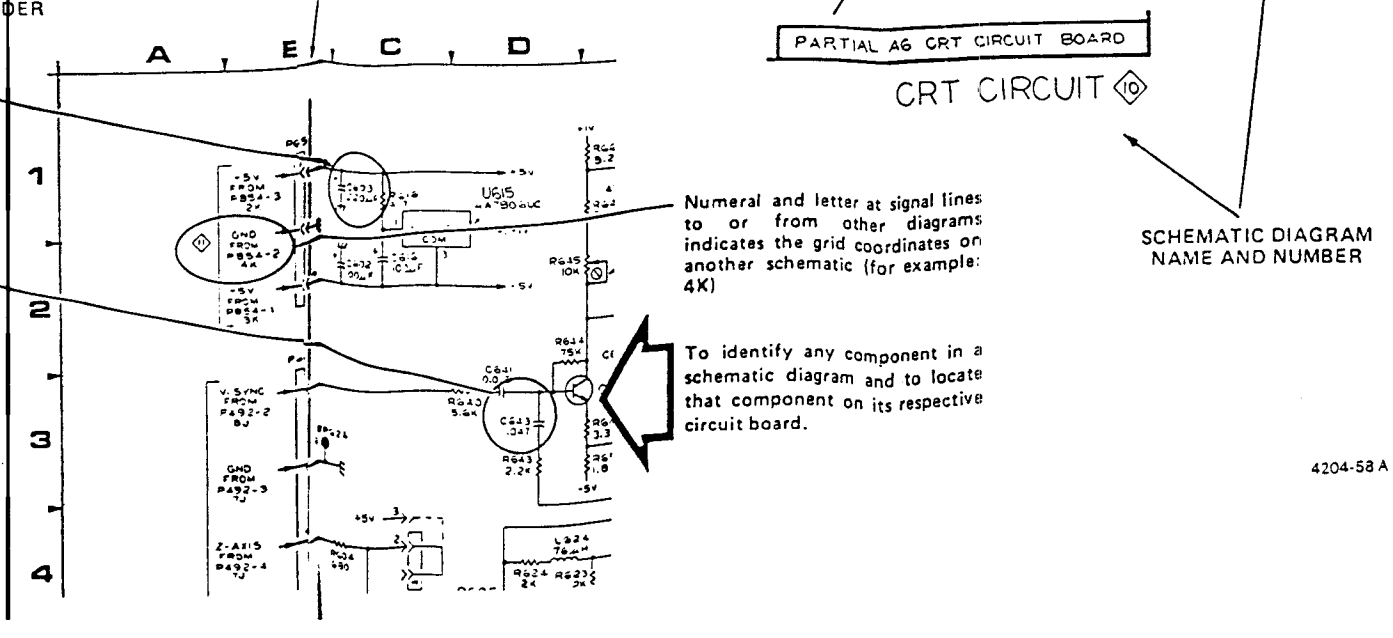
a. Locate and pull out tabbed page whose number and title correspond with the Schematic Diagram Number just determined in the table. Schematic diagram nomenclature and numbers are printed on the front side of the tabs (facing the front of the manual).

b. Scan the Component Location Table adjacent to the schematic diagram and find the Circuit Number of the desired component.

c Under the SCHEM LOCATION column, read the grid coordinates for the desired component.

d Using the Circuit Number and grid coordinates, locate the component on the schematic diagram.

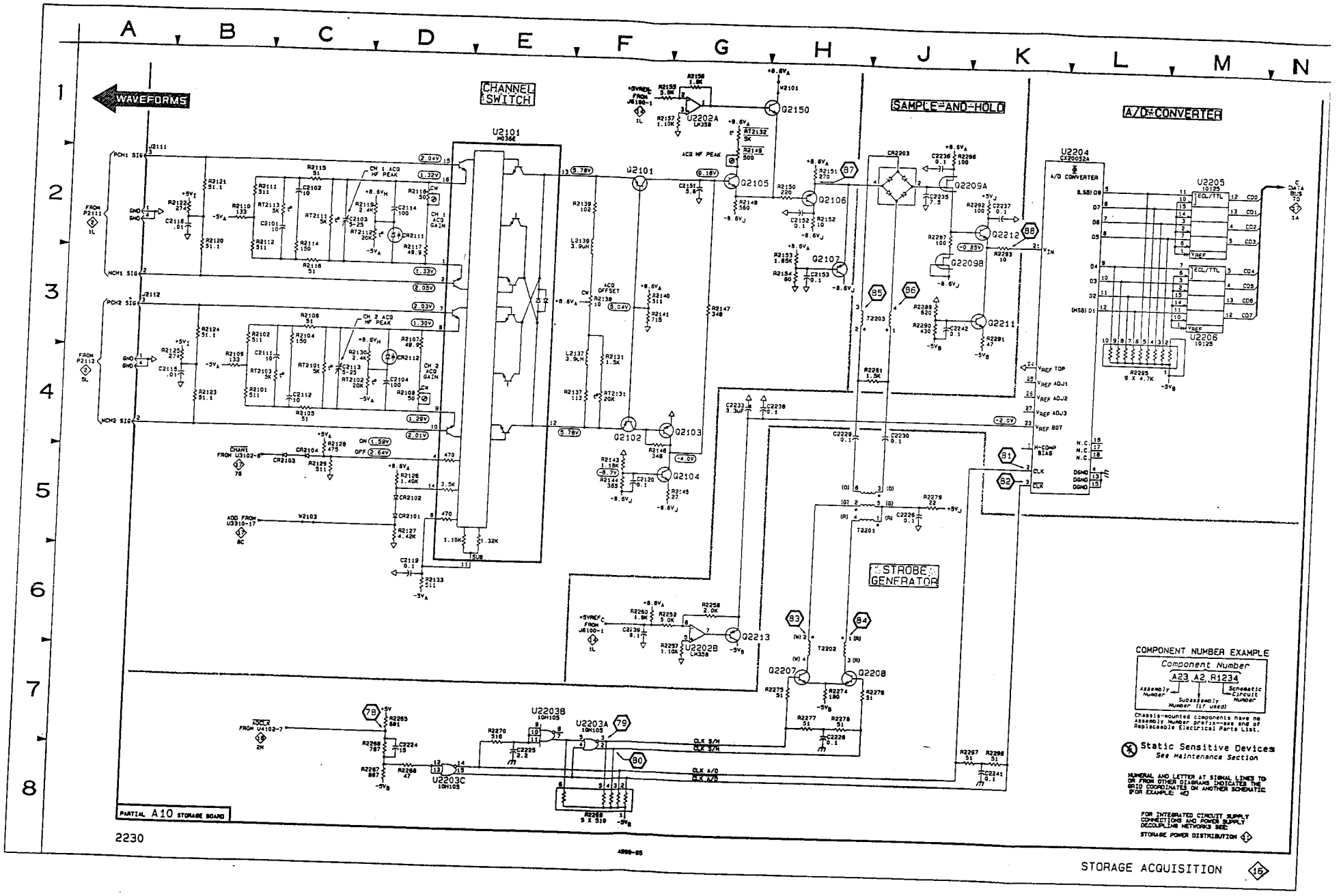




Numeral and letter at signal lines to or from other diagrams indicates the grid coordinates on another schematic (for example: 4K)

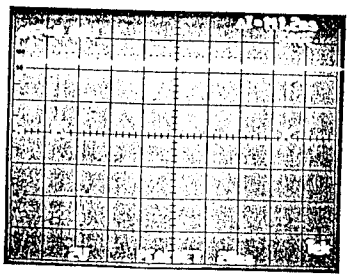
To identify any component in a schematic diagram and to locate that component on its respective circuit board.

4204-58 A


WAVEFORMS
CHANNEL SWITCH
SAMPLE-AND-HOLD
A/D CONVERTER
STROBE GENERATOR
U2101
U2202A
U2202B
U2203A
U2203B
U2203C
U2204
U2205
U2206
Q2150
Q2105
Q2106
Q2107
Q2102
Q2103
Q2104
Q2209A
Q2209B
Q2212
Q2211
Q2213
Q2207
Q2208
T2203
T2201
T2202
CH 1 ACQ HF PEAK
CH 2 ACQ HF PEAK
CH 1 ACQ GAIN
CH 2 ACQ GAIN
ACQ OFFSET
ACQ HF PEAK
CLK S/H
CLK A/D
PARTIAL A10 STORAGE BOARD
2230
STORAGE ACQUISITION
16
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no assembly number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE, 4D)
FOR INTEGRATED CIRCUIT SUPPLY CONNECTIONS AND POWER SUPPLY DECOUPLING NETWORKS SEE: STORAGE POWER DISTRIBUTION 12

WAVEFORMS FOR DIAGRAM 17

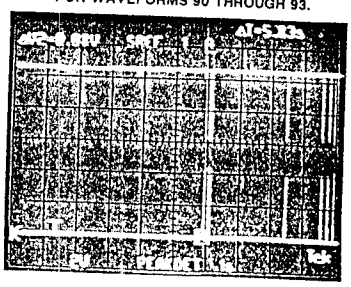
89



TEST SCOPE TRIGGERED ON U4118 PIN 6
FOR WAVEFORMS 90 THROUGH 93.

90

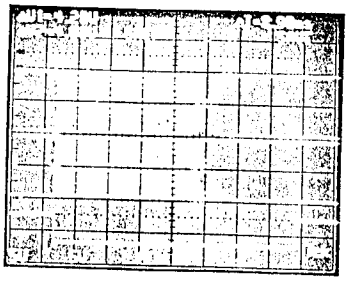
91



90

92

120

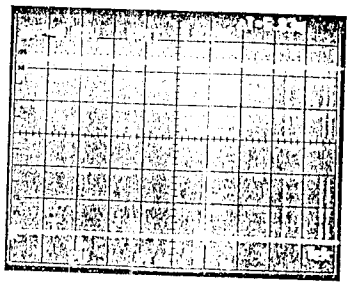


91

93

92

93

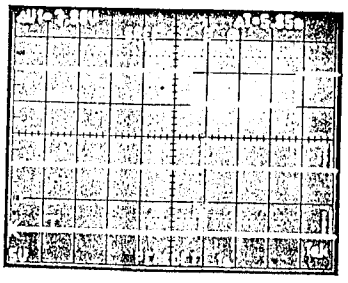


TEST SCOPE TRIGGERED ON U9111 PIN 21
FOR WAVEFORMS 94 THROUGH 105.

94

95

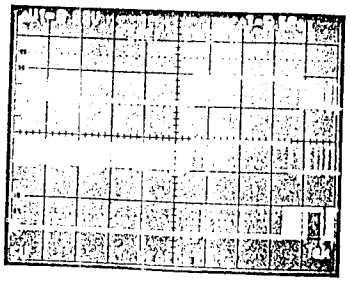
96

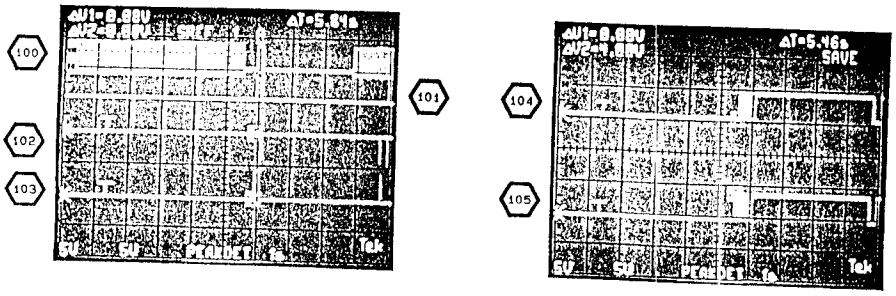


97

98

99



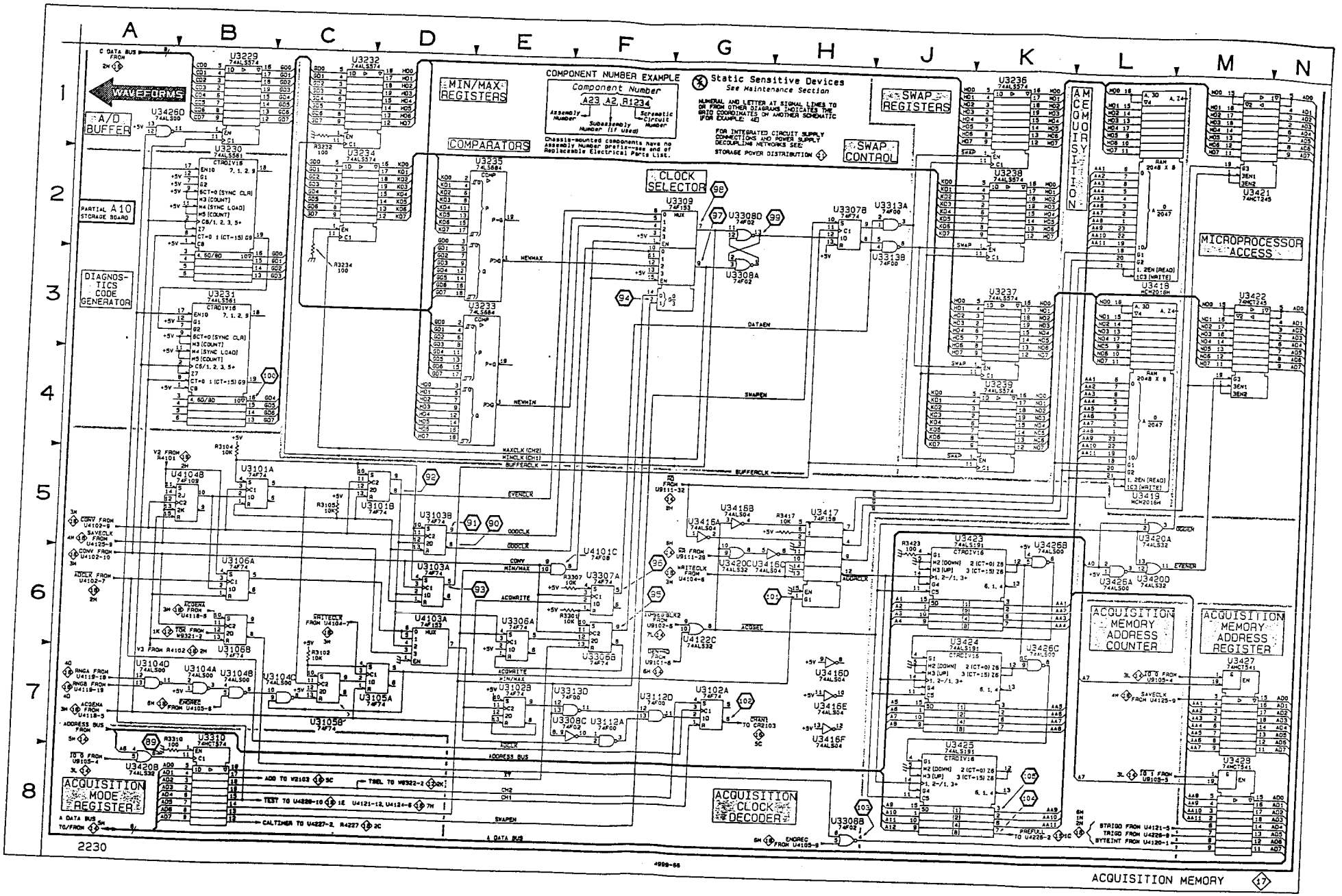

100
101
102
103
104
105
ΔT=5.46s
SAVE
Tek

ACQUISITION MEMORY DIAGRAM 17

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R3102	7C	3L
R3104	4B	5M
R3105	5C	4M
R3232	1C	4J
R3234	2C	7J
R3301	6F	4K
R3307	6F	6K
R3310	7B	6G
R3417	5H	5H
R3423	5J	6G
R4212	2G	10L
R4227	2C	9K
U3101A	5B	4M
U3101B	5D	4M
U3102A	7G	3L
U3102B	7E	3L
U3103A	6D	4L
U3103B	5D	4L
U3104A	7B	3L
U3104B	7B	3L
U3104C	7C	3L
U3104D	7B	3L
U3105A	7D	2L
U3105B	7C	2L
U3106A	6B	6M
U3106B	6B	6M
U3112A	7F	6K
U3112D	7G	6K
U3229	1B	4K
U3230	2B	7K
U3231	3B	5K
U3232	1C	4J
U3233	3E	5J
U3234	2C	7J
U3235	2E	7J
U3236	1K	4J
U3237	3K	5J
U3238	2K	7H
U3239	4K	8H
U3306A	6E	4K
U3306B	6F	4K
U3307A	6F	5K
U3307B	2H	5K
U3308A	3G	5L
U3308B	8J	5L
U3308C	7F	5L
U3308D	2G	5L
U3309	2G	4L
U3310	8B	5F
U3313A	2J	5L
U3313B	2J	5L
U3313D	7F	5L
U3416A	5G	5H
U3416B	5G	5H
U3416C	5H	5H
U3416D	6H	5H
U3416E	7H	5H
U3416F	7H	5H
U3417	5H	5H
U3418	3L	5G
U3420A	5L	5G
U3420B	8A	5G
U3420C	5G	5G
U3420D	5L	5G
U3421	2M	8G
U3422	3M	8H
U3423	5K	8G
U3424	9K	6G
U3425	7K	6F
U3426A	5L	5G
U3426B	5K	5G
U3426C	6K	5G
U3426D	1A	5G
U3427	6M	7G
U3428	7M	7F
U4101C	6F	5M
U4103A	6D	7L
U4104B	5B	7L
U4122C	6G	9H

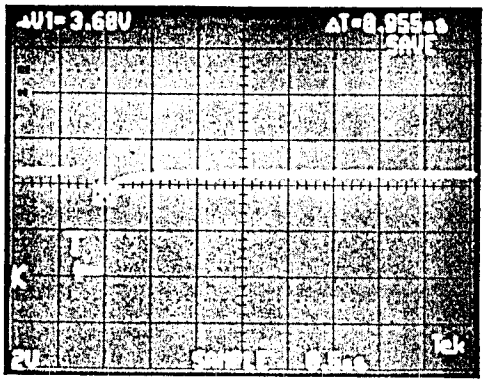
Partial A10 also shown on diagrams 11, 12, 14, 15, 16, 18 and 21.


WAVEFORMS
A/D BUFFER
PARTIAL A10 STORAGE BOARD
DIAGNOSTICS CODE GENERATOR
MIN/MAX REGISTERS
COMPARATORS
CLOCK SELECTOR
SWAP REGISTERS
SWAP CONTROL
MICROPROCESSOR ACCESS
ACQUISITION MODE REGISTER
ACQUISITION CLOCK DECODER
ACQUISITION MEMORY ADDRESS COUNTER
ACQUISITION MEMORY ADDRESS REGISTER
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Static Sensitive Devices
See Maintenance Section
2230
ACQUISITION MEMORY

WAVEFORMS FOR DIAGRAM 18

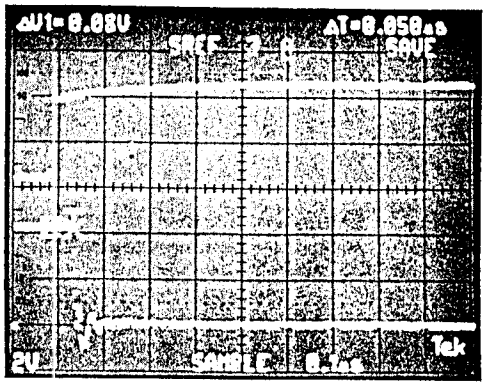
SET THE HORIZONAL MODE SWITCH TO B
AND APPLY A CAL SIGNAL TO CH 1 INPUT

106



107

102



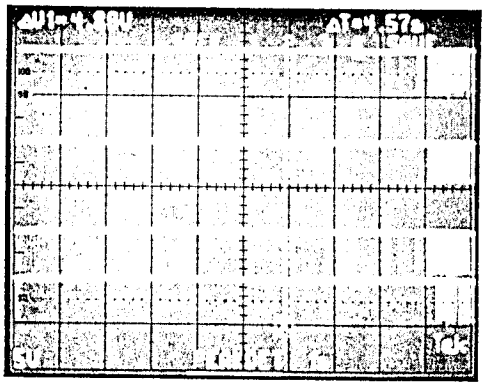
TEST SCOPE TRIGGERED ON U9111 PIN 21
FOR WAVEFORMS 108 THROUGH 111.

108

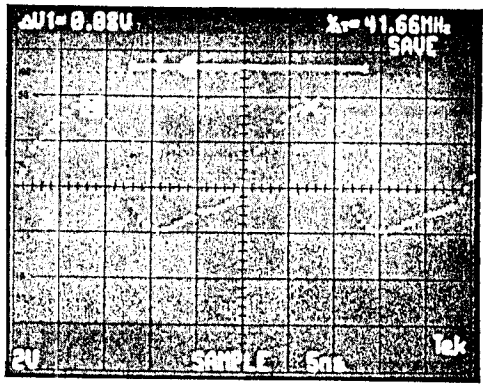
109

110

111

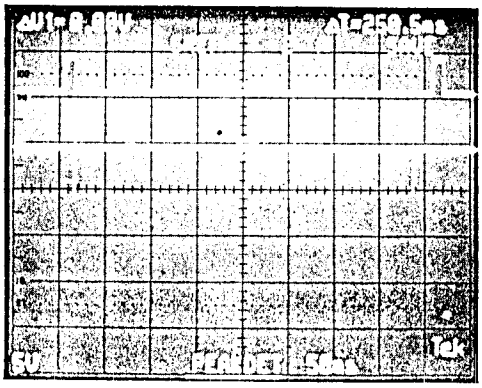


112

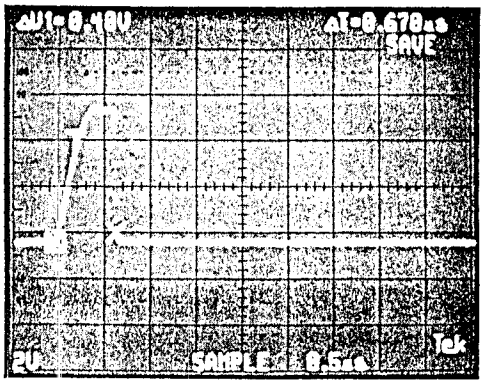


113

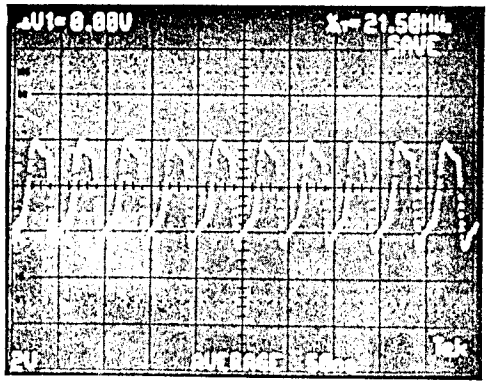
114



115

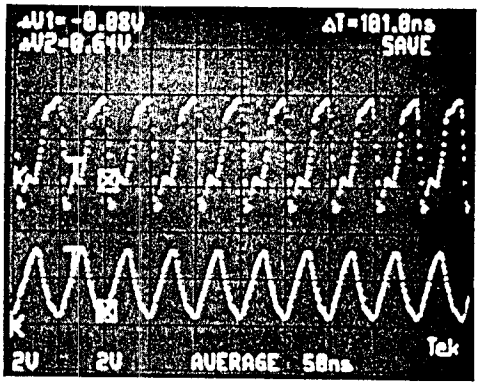


116



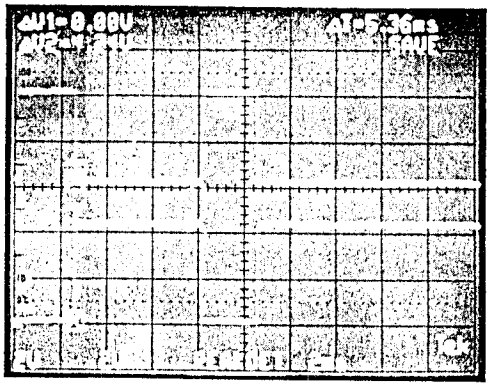
117

118



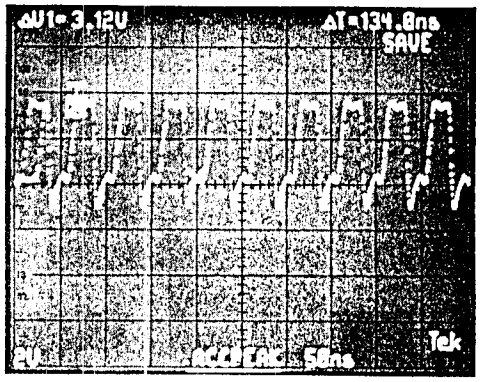
119

120



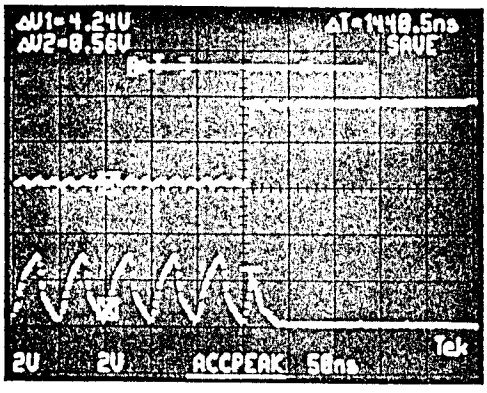
TEST SCOPE TRIGGERED ON U4105 PIN 9
FOR WAVEFORMS 121 AND 122.

121



122

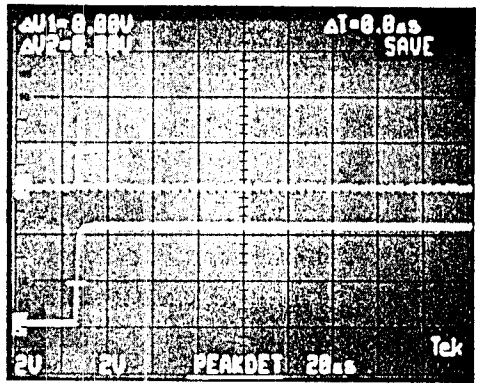
121



TEST SCOPE TRIGGERED ON U4227 PIN 10

123

U4227
PIN 10



4999-97

DIGITAL TIMEBASE DIAGRAM 18

ASSEMBLY A10

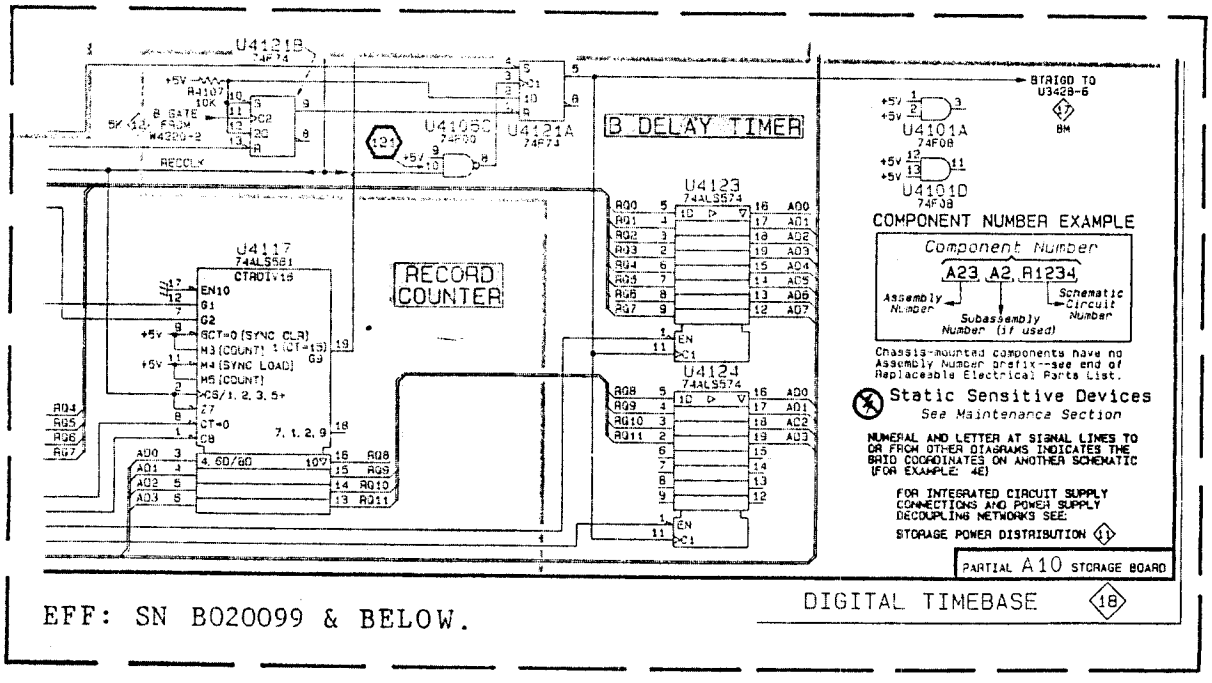
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C4101	2A	6L	R4214	2G	10L	U4118B	4M	10J
C4115	7D	9F	R4215	2G	10L	U4119	4B	9J
C4118*	3D	9J	R4216	2H	10M	U4120A	2M	9J
C4201	2G	10L	R4217	1H	10M	U4120B	4M	9J
C4202	1F	10K	R4220	2M	9J	U4120C	4M	9J
C4203	2F	10L				U4120D	5M	9J
			U3112B	3D	6K	U4121A	6K	10J
J4104	2A	6L	U3112C	3E	6K	U4121B	6H	10J
			U3113C	4D	5L	U4122A	8B	9H
Q4203	1G	10L	U4101A	6M	5M	U4122B	7B	9H
Q4204	1G	10L	U4101B	4E	5M	U4122D	7B	9H
Q4205	2G	10L	U4101D	6M	5M	U4123	7L	9G
Q4207	2F	10L	U4102A	2A	7K	U4124	8L	9H
Q4227	2C	9K	U4102B	3B	7K	U4125A	4K	8M
			U4103B	4K	7L	U4125B	4L	8M
R4101	2A	6M	U4104A	3E	7L	U4126A	4G	6M
R4102	2A	6M	U4105A	5J	9M	U4126B	4H	6M
R4103	5K	9L	U4105B	5J	9M	U4127A	5H	7M
R4104	5L	9M	U4106A	5H	8L	U4127B	2E	7M
R4105	4L	10K	U4106B	1H	8L	U4127C	1E	7M
R4106	7D	9G	U4106C	6J	8L	U4127D	5C	7M
R4107	6H	10H	U4106D	5H	8L	U4226A	1C	9K
R4108	5C	7L	U4107	5C	7K	U4226B	1F	9K
R4110	2B	6K	U4108	5D	7K	U4227	1C	9K
R4115	7D	8F	U4109	5E	7L	U4228A	2D	9L
R4119	5A	8J	U4110	6F	7L	U4228B	1E	9L
R4201	1B	10J	U4111	6G	8K	U4229	2H	9L
R4202	2E	10K	U4112	6G	8L	U4230	1K	8J
R4203	2F	10K	U4113	5B	8K	U4231A	1M	9J
R4204	1G	9L	U4114A	8B	9H	U4231B	1M	9J
R4205	1G	10L	U4114B	7B	9H	U4232A	1J	9L
R4206	1H	10L	U4114C	6A	9H	U4232B	1J	9L
R4207	1H	10L	U4114D	5A	9H			
R4208	1E	10K	U4115	8E	9G	W4201	1D	9K
R4209	1F	9L	U4116	8G	8F			
R4210	2G	10K	U4117	7H	9H	Y4100	2A	6L
R4211	2G	10K	U4118A	3C	10J			
R4213	1H	10L						

Partial A10 also shown on diagrams 11, 12, 14, 15, 16, 17 and 21.

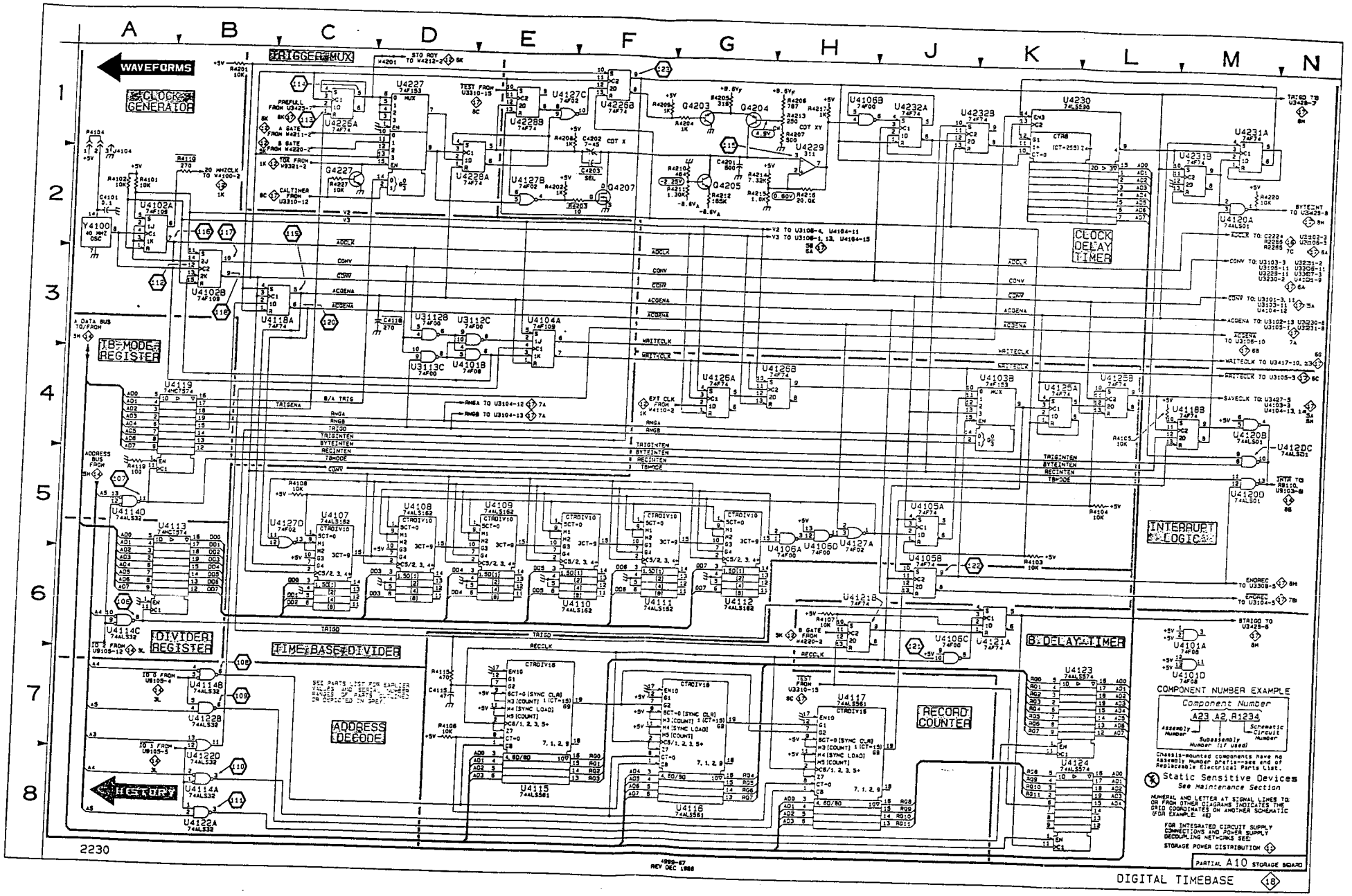
CHASSIS MOUNTED PARTS

P4104	1A	CHASSIS						

***See Parts List for serial number ranges.**



EFF: SN B020099 & BELOW.



WAVEFORMS FOR DIAGRAM 18

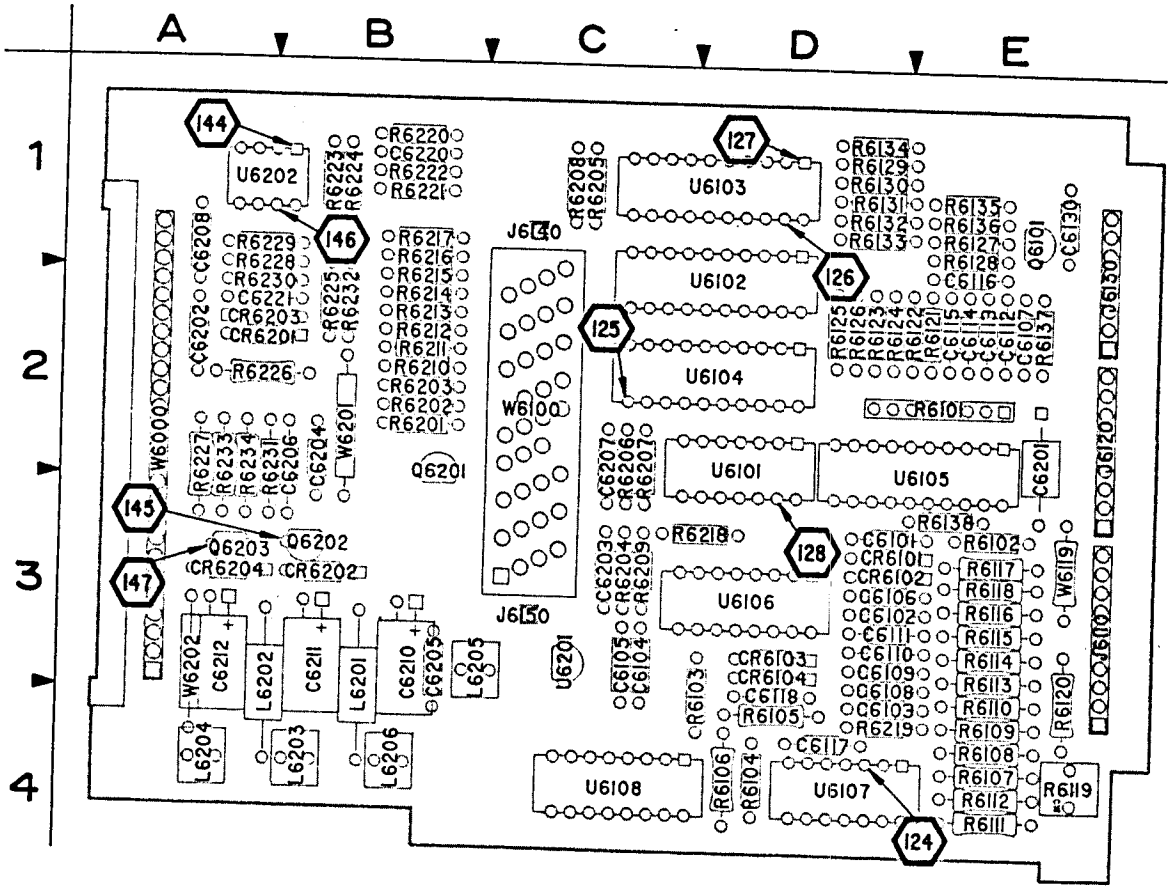
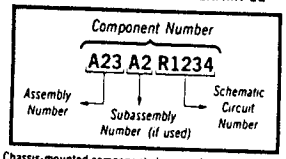


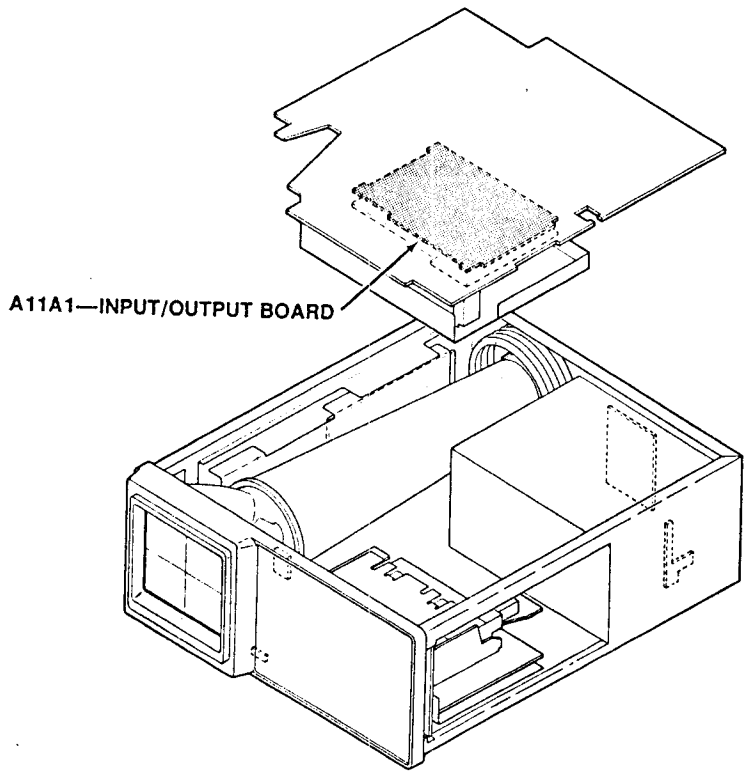
Figure 9-22. A11A1—Input/Output board.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

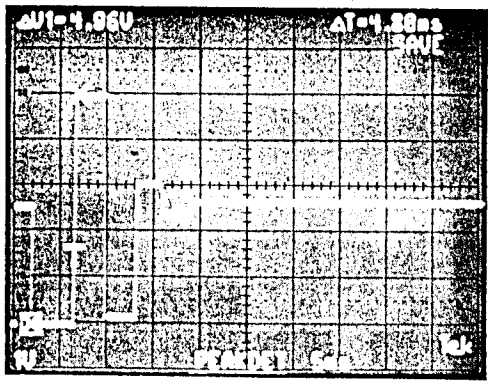


A11A1—INPUT/OUTPUT BOARD

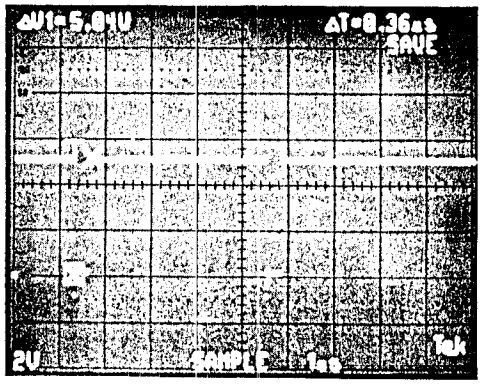
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C6101	19	R6102	19	R6219	21
C6102	19	R6102	19	R6220	21
C6103	19	R6103	19	R6221	21
C6104	19	R6104	19	R6222	21
C6105	19	R6105	19	R6223	21
C6106	19	R6106	19	R6224	21
C6107	19	R6107	19	R6225	21
C6108	19	R6108	19	R6226	21
C6109	19	R6109	19	R6227	21
C6110	19	R6110	19	R6228	21
C6111	19	R6111	19	R6229	21
C6112	19	R6112	19	R6230	21
C6113	19	R6113	19	R6231	21
C6114	19	R6114	19	R6232	21
C6115	19	R6115	19	R6233	21
C6116	19	R6116	19	R6234	21
C6117	19	R6117	19	U6101	19
C6118	19	R6118	19	U6101	19
C6130	19	R6119	19	U6101	19
C6201	21	R6120	19	U6101	19
C6202	21	R6121	19	U6101	21
C6203	21	R6122	19	U6102	19
C6204	21	R6123	19	U6102	21
C6205	21	R6124	19	U6103	19
C6206	21	R6125	19	U6103	21
C6207	21	R6126	19	U6104	19
C6208	21	R6127	19	U6104	21
C6210	21	R6128	19	U6105	19
C6211	21	R6129	19	U6105	21
C6212	21	R6130	19	U6106	19
C6220	21	R6131	19	U6106	21
C6221	21	R6132	19	U6107	19
CR6101	19	R6133	19	U6107	19
CR6102	19	R6134	19	U6107	19
CR6103	19	R6135	19	U6107	19
CR6104	19	R6136	19	U6107	21
CR6201	21	R6137	19	U6108	19
CR6202	21	R6138	19	U6108	21
CR6203	21	R6201	20	U6201	21
CR6204	21	R6202	20	U6202	21
J6110	19	R6203	20	U6202	21
J6120	19	R6204	19	W6000	20
J6130	19	R6205	19	W6000	20
J6140	21	R6206	19	W6000	20
J6150	21	R6207	19	W6000	20
L6201	21	R6208	19	W6000	20
L6202	21	R6209	19	W6000	20
L6203	21	R6210	19	W6000	21
L6204	21	R6211	19	W6100	19
L6205	21	R6212	19	W6100	20
L6206	21	R6213	19	W6100	21
Q6101	19	R6214	19	W6119	19
Q6201	19	R6215	19	W6201	21
Q6202	21	R6216	19	W6202	21
Q6203	21	R6217	19		
R6101	19	R6218	19		

WAVEFORMS FOR DIAGRAM 19

124



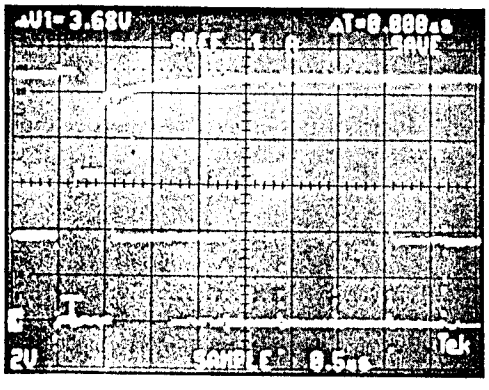
125



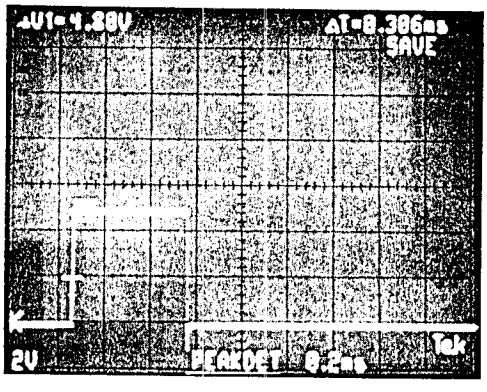
TEST SCOPE TRIGGERED ON U6103 PIN 1
FOR WAVEFORMS 126 AND 127.

127

126



128



STATUS ADC AND BUS INTERFACE DIAGRAM 19

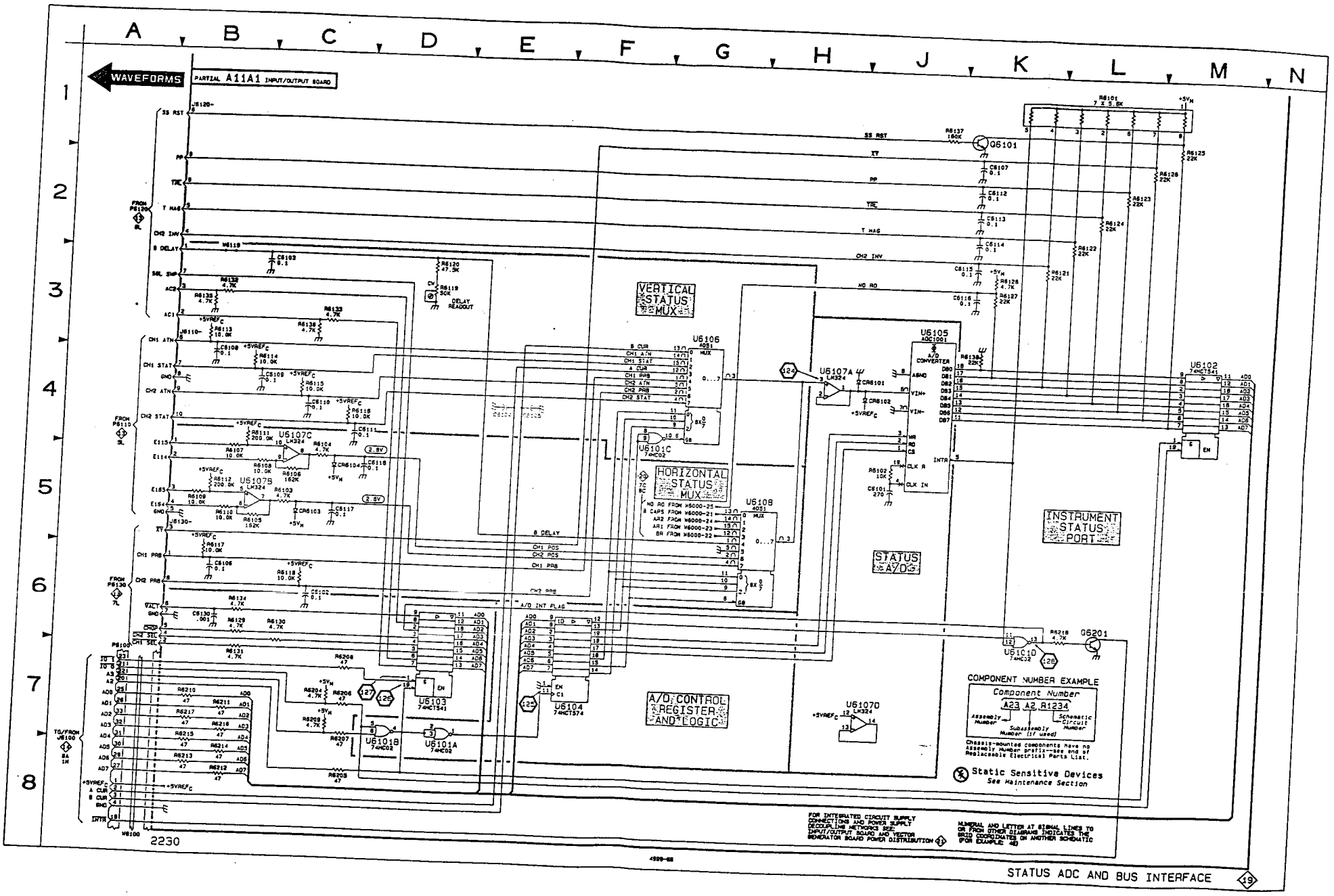
ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C6101	5J	3D	R6103	5C	3D	R6138	3K	3E
C6102	6C	3D	R6104	5C	4D	R6204	7C	3C
C6103	3C	4D	R6105	5B	4D	R6205	8C	1C
C6104	4E	3C	R6106	5C	4D	R6206	7C	2C
C6105	4E	3C	R6107	5B	4E	R6207	7C	2C
C6106	6B	3D	R6108	5C	4E	R6208	7C	1C
C6107	1K	2E	R6109	5B	4E	R6209	7C	3C
C6108	4B	3D	R6110	5B	4E	R6210	7B	2B
C6109	4C	3D	R6111	4B	4E	R6211	7B	2B
C6110	4C	3D	R6112	5B	4E	R6212	8B	2B
C6111	4C	3D	R6113	3B	3E	R6213	8B	2B
C6112	2K	2E	R6114	4B	3E	R6214	8B	2B
C6113	2K	2E	R6115	4C	3E	R6215	7B	2B
C6114	2K	2E	R6116	4C	3E	R6216	7B	1B
C6115	2K	2E	R6117	6B	3E	R6217	7B	1B
C6116	3K	2E	R6118	6C	3E	R6218	6L	3D
C6117	5C	4E	R6119	3D	4E			
C6118	5D	4D	R6120	3D	3E	U6101A	7D	2D
C6130	6B	1E	R6121	2K	2E	U6101B	7D	2D
			R6122	2L	2E	U6101C	4F	2D
CR6101	4J	3E	R6123	2L	2D	U6101D	6K	2D
CR6102	4J	3E	R6124	2L	2D	U6102	3M	2C
CR6103	5C	3D	R6125	1M	2D	U6103	7D	1C
CR6104	5C	3D	R6126	1L	2D	U6104	7F	2C
			R6127	3K	1E	U6105	3J	2D
J6110	3B	4E	R6128	3K	1E	U6106	3G	3D
J6120	1B	3E	R6129	6B	1D	U6107A	4H	4D
J6130	5B	2E	R6130	6C	1D	U6107B	5B	4D
			R6131	7B	1D	U6107C	4C	4D
Q6101	1K	1E	R6132	3B	1D	U6107D	7J	4D
Q6201	6L	2B	R6133	3C	1D	U6108	5H	4C
			R6134	6B	1D			
R6101	1L	2E	R6135	3B	1E	W6100	8A	3C
R6102	5J	3E	R6136	3C	1E	W6119	2B	3E
R6102	6C	3E	R6137	1J	2E			

Partial A11 also shown on diagrams 20 and 21.

CHASSIS MOUNTED PARTS

P6100	7A	CHASSIS						



WAVEFORMS FOR DIAGRAM 16

WAVEFORMS FOR DIAGRAM 17

WAVEFORMS FOR DIAGRAM 18

A11A1—INPUT/OUTPUT BOARD

FIG. 9-22

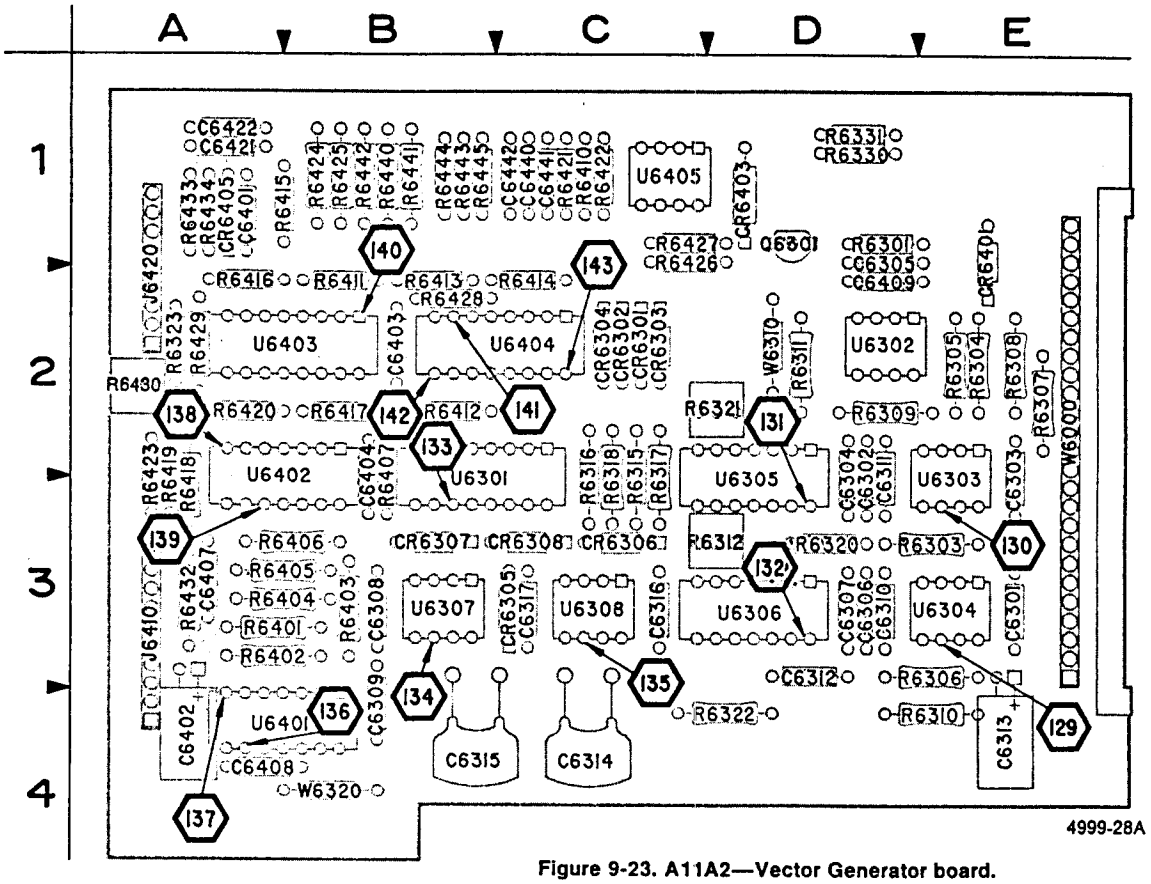
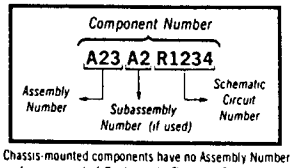


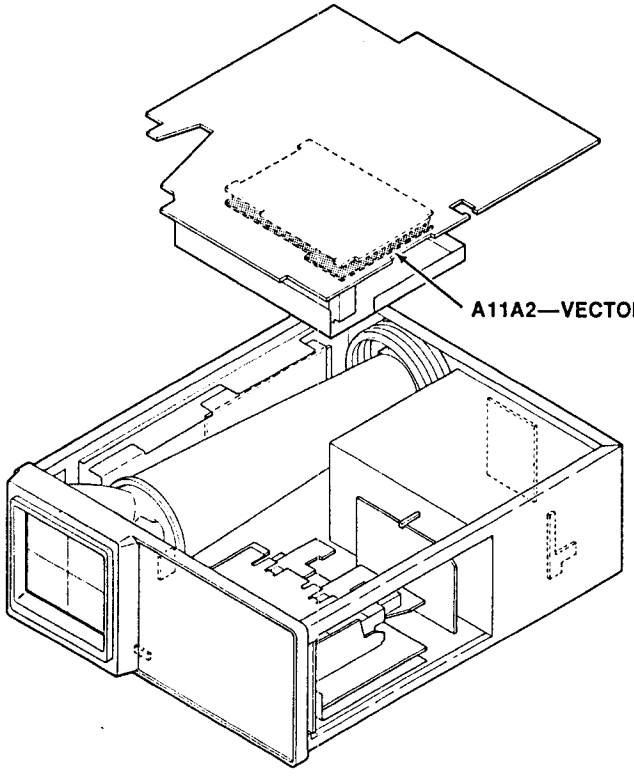
Figure 9-23. A11A2—Vector Generator board.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



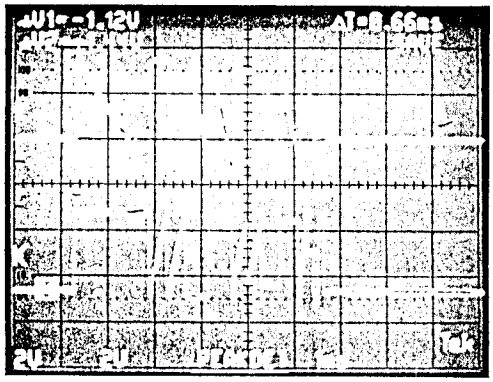
A11A2—VECTOR GENERATOR BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C6301	21	Q6301	20	R6425	20
C6302	21			R6426	20
C6303	21	R6301	21	R6427	20
C6304	21	R6303	20	R6428	20
C6305	21	R6304	20	R6429	20
C6306	21	R6305	20	R6430	20
C6307	21	R6306	20	R6432	20
C6308	21	R6307	20	R6433	20
C6309	21	R6308	20	R6434	20
C6310	20	R6309	20	R6440	20
C6311	20	R6310	20	R6441	20
C6312	20	R6311	20	R6442	20
C6313	21	R6312	20	R6443	20
C6314	20	R6315	20	R6444	20
C6315	20	R6316	20	R6445	20
C6316	20	R6317	20		
C6317	20	R6318	20	U6301	20
C6401	20	R6320	20	U6301	21
C6402	20	R6321	20	U6302	21
C6403	21	R6322	20	U6303	20
C6404	21	R6323	20	U6303	21
C6407	20	R6330	20	U6304	20
C6408	20	R6331	20	U6304	21
C6409	21	R6401	20	U6305	20
C6421	20	R6402	20	U6305	21
C6422	20	R6403	20	U6306	20
C6440	20	R6404	20	U6306	21
C6441	20	R6405	20	U6307	20
C6442	20	R6406	20	U6307	21
		R6407	20	U6308	20
CR6301	20	R6410	21	U6308	21
CR6302	20	R6411	20	U6401	20
CR6303	20	R6412	20	U6402	20
CR6304	20	R6413	20	U6403	20
CR6305	20	R6414	20	U6404	20
CR6306	20	R6415	20	U6404	21
CR6307	20	R6416	20	U6405	20
CR6308	20	R6417	20	U6405	21
CR6401	20	R6418	20		
CR6403	20	R6419	20	W6000	20
CR6405	20	R6420	20	W6000	21
		R6421	20	W6310	20
J6410	20	R6422	20	W6320	20
J6420	20	R6423	20		
		R6424	20		

WAVEFORMS FOR DIAGRAM 20

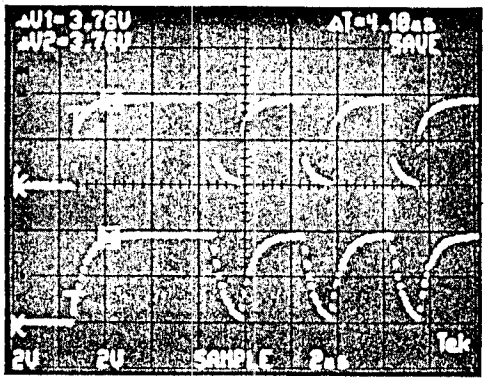
SET WAVEFORM REFERENCE/MENU SELECT SWITCH TO MENU SELECT
AND SELECT BOX FOR WAVEFORMS 129 THROUGH 139

129



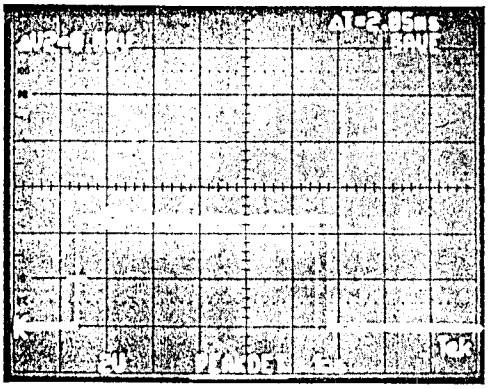
130

131

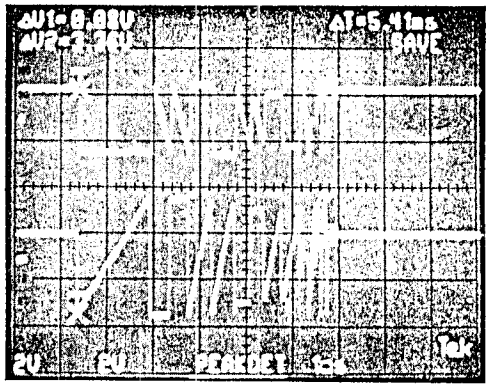


132

133

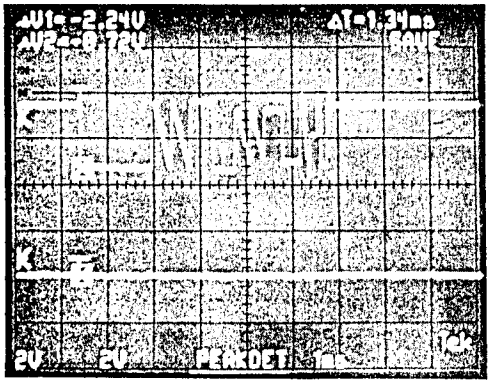


134



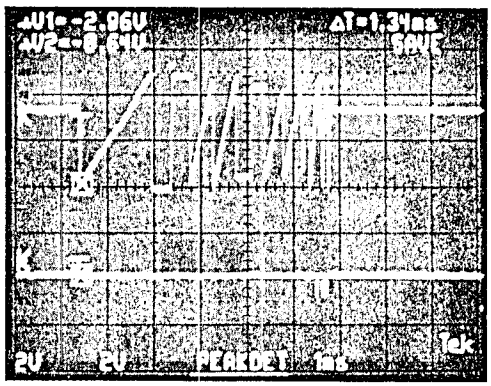
135

136



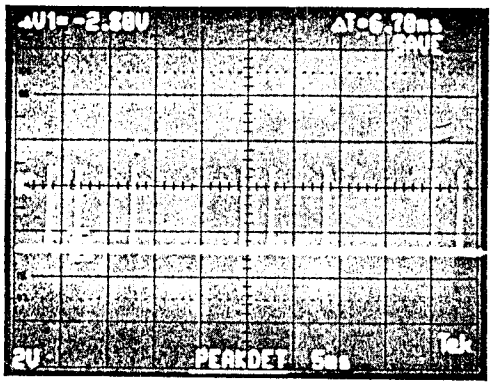
137

138

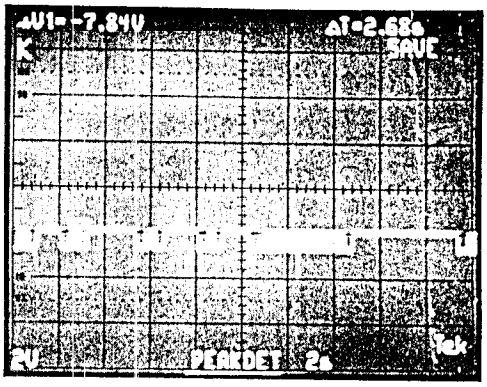


139

140

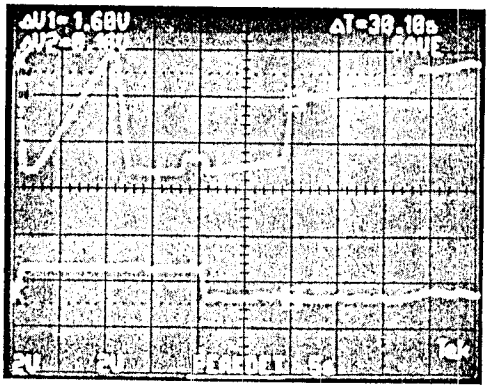


141



142

143



VECTOR GENERATOR DIAGRAM 20

ASSEMBLY A11A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R6201	5C	2B	W6000	2D	3A	W6C00	7D	3A
R6202	2C	2B	W6000	3D	3A	W6000	8D	3A
R6203	4C	2B	W6000	4D	3A	W6100	6B	3C
			W6000	5D	3A			

Partial A11A1 also shown on diagrams 19 and 21.

ASSEMBLY A11A2

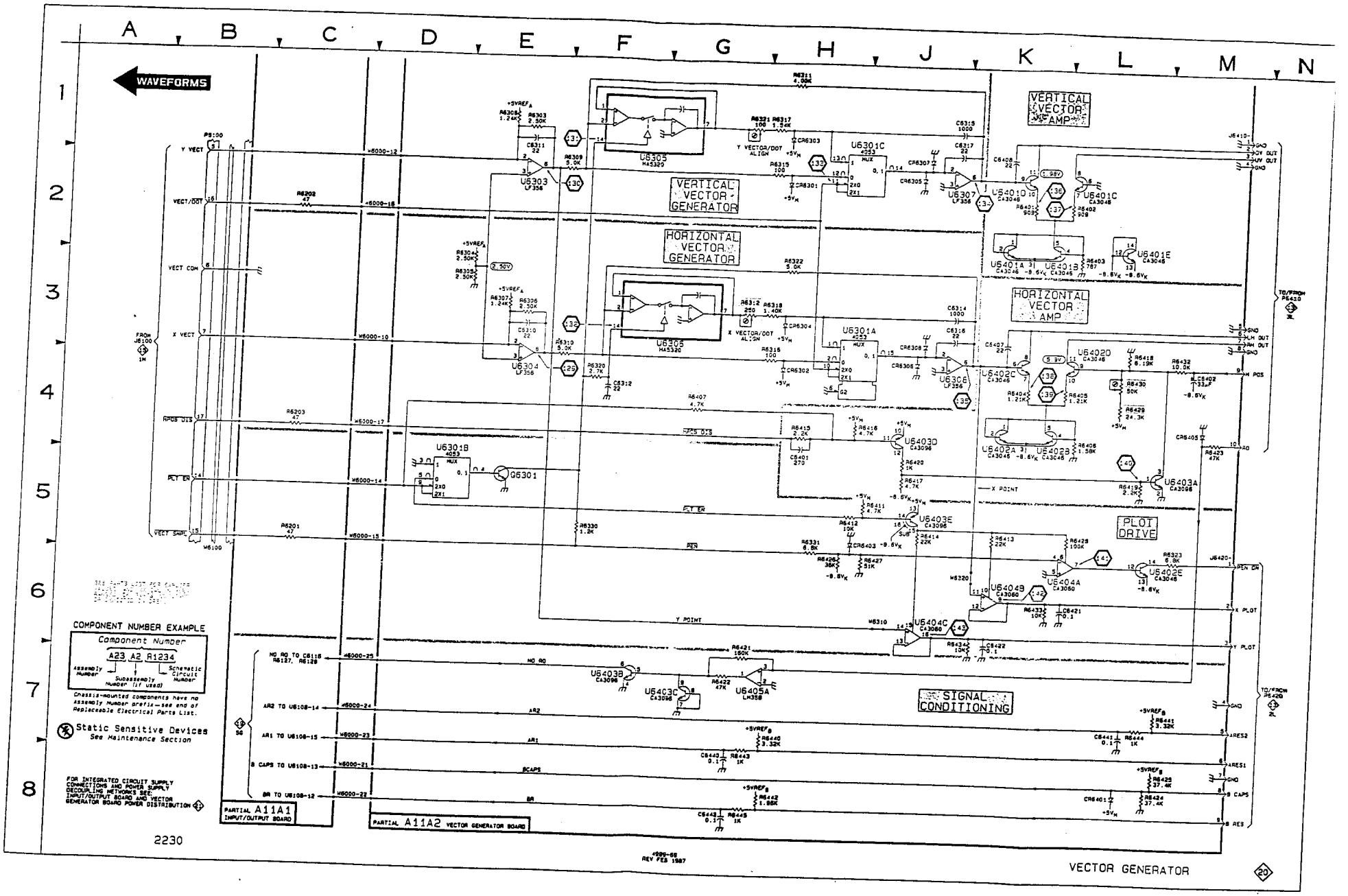
C6310	3E	3D	R6311	1H	2D	R6440	7H	1B
C6311	1E	3D	R6312	3G	3C	R6441	7M	1B
C6312	4F	3D	R6315	2H	3C	R6442	8H	1B
C6314	3J	3C	R6316	3H	3C	R6443	7G	1B
C6315	1J	3C	R6317	1H	3C	R6444	7L	1B
C6316	3J	3C	R6318	3H	3C	R6445	8G	1B
C6317	1J	3C						
			R6320	4F	3D			
C6401	4H	1A	R6321	1G	2C			
C6402	4M	3A	R6322	2H	4D	U6301A	3H	3B
C6407	3K	3A	R6323	5M	2A	U6301B	4D	3B
C6408	1K	4A	R6330	5F	1D	U6301C	1H	3B
C6421	6L	1A	R6331	5H	1D	U6303	2E	3E
C6422	6K	1A	R6401	2K	3A	U6304	4E	3E
C6440	7G	1C	R6402	2L	3A	U6305	1F	3D
C6441	7L	1C	R6403	2L	3B	U6306	3G	3D
C6442	8G	1C	R6404	4K	3B	U6307	2J	3B
			R6405	4L	3B	U6308	3J	3C
CR6301	2H	2C	R6406	4L	3B	U6401A	2K	4B
CR6302	3H	2C	R6407	4G	3B	U6401B	2K	4B
CR6303	1H	2C	R6411	5J	2B	U6401C	2L	4B
CR6304	3H	2C	R6412	5H	2B	U6401D	2K	4B
CR6305	2J	3C	R6413	5K	2B	U6401E	2L	4B
CR6306	3J	3C	R6414	5J	2C	U6402A	4K	3B
CR6307	1J	3C	R6415	4H	1B	U6402B	4K	3B
CR6308	3J	3C	R6416	4J	2A	U6402C	4K	3B
CR6401	8L	2E	R6417	5J	2B	U6402D	3L	3B
CR6403	5J	2D	R6418	3L	3A	U6402E	5L	3B
CR6405	4M	2A	R6419	5L	3A	U6403A	5M	2B
			R6420	4J	2A	U6403B	7F	2B
J6410	1M	4A	R6421	6G	1C	U6403C	7G	2B
J6420	5M	2A	R6422	7G	1C	U6403D	4J	2B
			R6423	4M	3A	U6403E	5J	2B
Q6301	5E	1D	R6424	8M	1B	U6404A	6L	2C
			R6425	8M	1B	U6404B	6K	2C
R6303	1E	3E	R6426	5H	2C	U6404C	6J	2C
R6304	2D	2E	R6427	5J	1C	U6405A	7H	1C
R6305	3D	2E	R6428	5L	2B			
R6306	3E	3E	R6429	4L	2A	W6000	2D	3E
R6307	3E	2E	R6430*	4L	2A	W6000	3D	3E
R6308	1E	2E	R6432	3L	3A	W6000	4D	3E
R6309	2E	2D	R6433	6K	1A	W6000	5D	3E
R6310	3F	4E	R6434	6K	1A	W6000	7D	3E
						W6000	8D	3E
						W6310	6J	2D
						W6320	6K	4B

Partial A11A2 also shown on diagram 21.

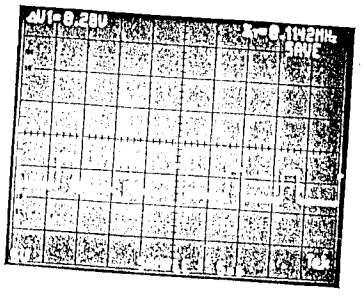
CHASSIS MOUNTED PARTS

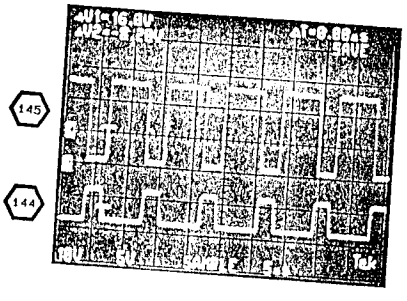
P6100	1B	CHASSIS						

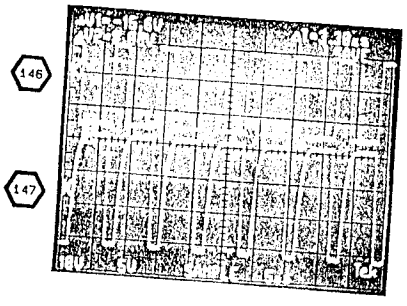
*See Parts List for serial number ranges.


WAVEFORMS
VERTICAL VECTOR GENERATOR
HORIZONTAL VECTOR GENERATOR
VERTICAL VECTOR AMP
HORIZONTAL VECTOR AMP
PLOT DRIVE
SIGNAL CONDITIONING
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
FOR INTEGRATED CIRCUIT SUPPLY CONNECTIONS AND POWER SUPPLY DECOUPLING NETWORKS SEE INPUT/OUTPUT BOARD AND VECTOR GENERATOR BOARD POWER DISTRIBUTION
PARTIAL A11A1 INPUT/OUTPUT BOARD
PARTIAL A11A2 VECTOR GENERATOR BOARD
2230
REV FEB 1987
VECTOR GENERATOR
20

WAVEFORMS FOR DIAGRAM 21







INPUT/OUTPUT & VECTOR GENERATOR BOARDS
POWER DISTRIBUTION DIAGRAM 21

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J6100	3A	10D						

Partial A10 also shown on diagrams 11, 12, 14, 15, 16, 17 and 18.

ASSEMBLY A11A1

C6201	1H	2E	L6201	4D	3B	R6231	4F	2B
C6202	1J	2A	L6202	5F	3B	R6232	5F	2B
C6203	6B	3C	L6203	6J	4B	R6233	5F	2A
C6204	6C	2B	L6204	7J	4A	R6234	5F	2A
C6205	3B	3B	L6205	3J	3C			
C6206	3C	2B	L6206	2J	4B	U6101	4H	2D
C6207	4G	2C				U6102	4H	2C
C6208	4H	1A	Q6202	5D	3B	U6103	4H	1C
C6210	5B	3B	Q6203	5F	3A	U6104	5H	2C
C6211	4E	3B				U6105	1F	2D
C6212	5G	3A	R6219	2E	4D	U6106	5J	3D
C6220	5C	1B	R6220	4C	1B	U6107	5B	4D
C6221	5E	2A	R6221	4D	1B	U6108	5J	4C
			R6222	5D	1B	U6201	4G	3C
CR6201	5D	2B	R6223	4D	1B	U6202B	4E	1B
CR6202	4D	3B	R6224	4D	1B	U6202	5C	1B
CR6203	5F	2A	R6225	5D	2B			
CR6204	5F	3B	R6226	5E	2A	W6000	1J	3A
			R6227	5E	2A	W6100	6B	3C
J6140	4B	1C	R6228	4E	2A	W6201	1H	2B
J6150	4B	3C	R6229	4E	1A	W6202	2J	3A
			R6230	5E	2A			

Partial A11A1 also shown on diagrams 19 and 20.

ASSEMBLY A11A2

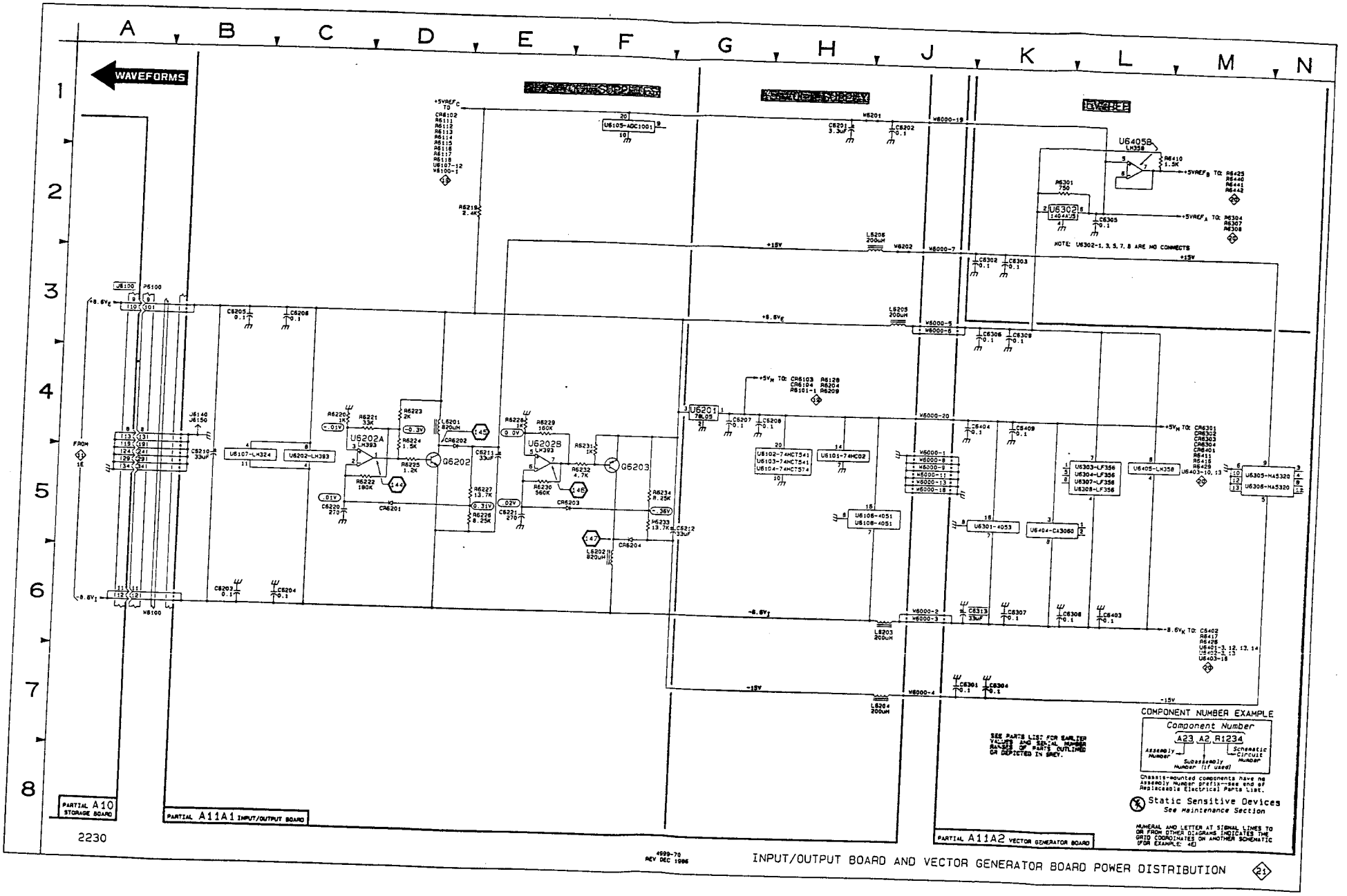
C6301	7K	3E	C6403	6L	2B	U6304	5K	3E
C6302	2K	3D	C6404	4K	3B	U6305	4N	3D
C6303	2K	3E	C6409	4K	2D	U6306	5N	3D
C6304	7K	3D				U6307	5K	3B
C6305	2L	2D	R6301	2K	1D	U6308	5K	3C
C6306	3K	3D	R6410	1L	1C	U6404	5K	2C
C6307	6K	3D				U64058	1L	1C
C6308	6L	3B	U6301	5K	3B	U6405	4L	1C
C6309	3K	4B	U6302	2K	2E			
C6313*	6K	3E	U6303	4L	3E	W6000	1J	3E

Partial A11A2 also shown on diagram 20

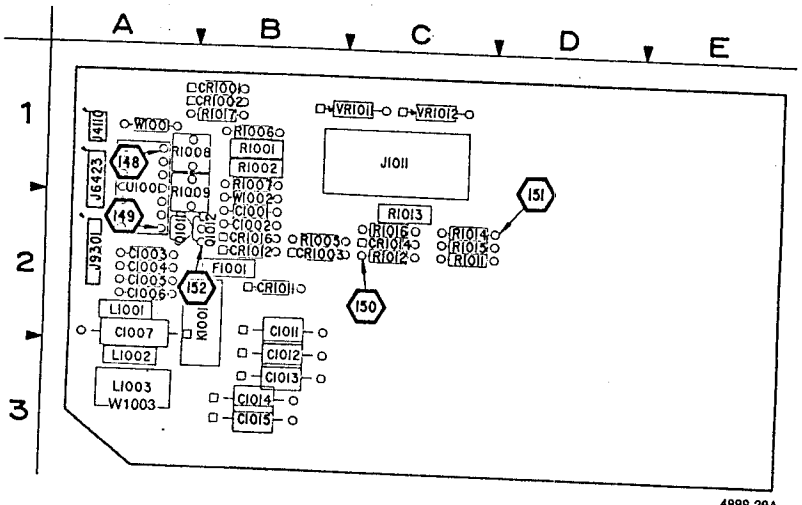
CHASSIS MOUNTED PARTS

P6100	3A	CHASSIS						

*See Parts List for serial number ranges.



WAVEFORMS FOR DIAGRAM 16
A11A2—VECTOR GENERATOR BOARD
WAVEFORMS FOR DIAGRAM 17
WAVEFORMS FOR DIAGRAM 21
WAVEFORMS FOR DIAGRAM 14
WAVEFORMS FOR DIAGRAM 18
WAVEFORMS FOR DIAGRAM 15
A11A1—INPUT/OUTPUT



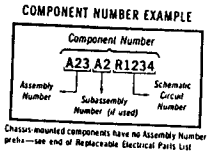
4999-29A

Figure 9-24. A20—XY Plotter board.

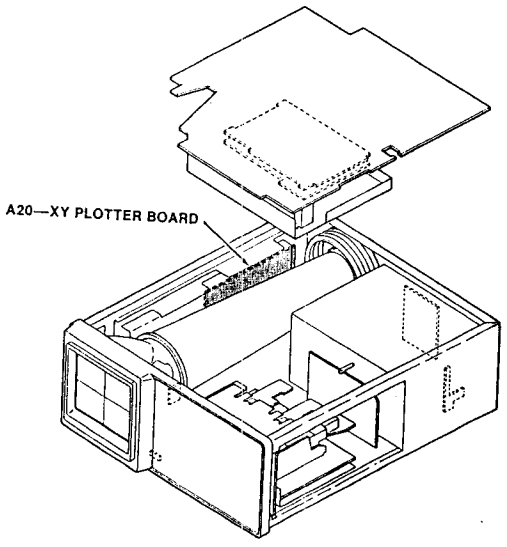
A20—XY PLOTTER BOARD FIG. 9-24

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



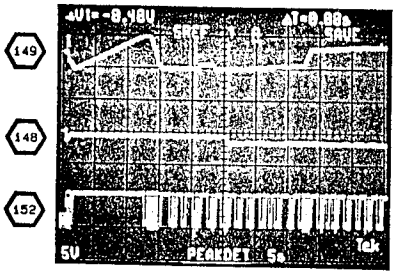
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

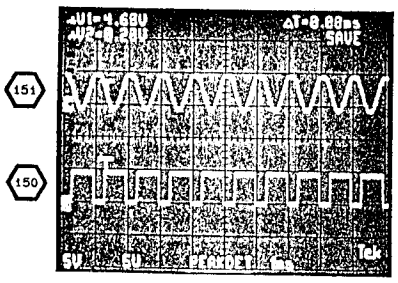


A20—XY PLOTTER BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C1001	22	CR1015	22	R1002	22
C1002	22			R1005	22
C1003	22	F1001	22	R1011	22
C1004	22			R1012	22
C1005	22	J1011	22	R1013	22
C1006	22	J4110	22	R1014	22
C1007	22	J6423	22	R1015	22
C1011	22	J9301	22	R1016	22
C1012	22			R1017	22
C1013	22	K1001	22		
C1014	22			U1001	22
C1015	22	L1001	22		
		L1002	22	VR1011	22
CR1001	22	L1003	22	VR1012	22
CR1002	22				
CR1003	22	Q1011	22	W1001	22
CR1011	22	Q1012	22	W1002	22
CR1012	22			W1003	22
CR1014	22	R1001	22		

WAVEFORMS FOR DIAGRAM 22





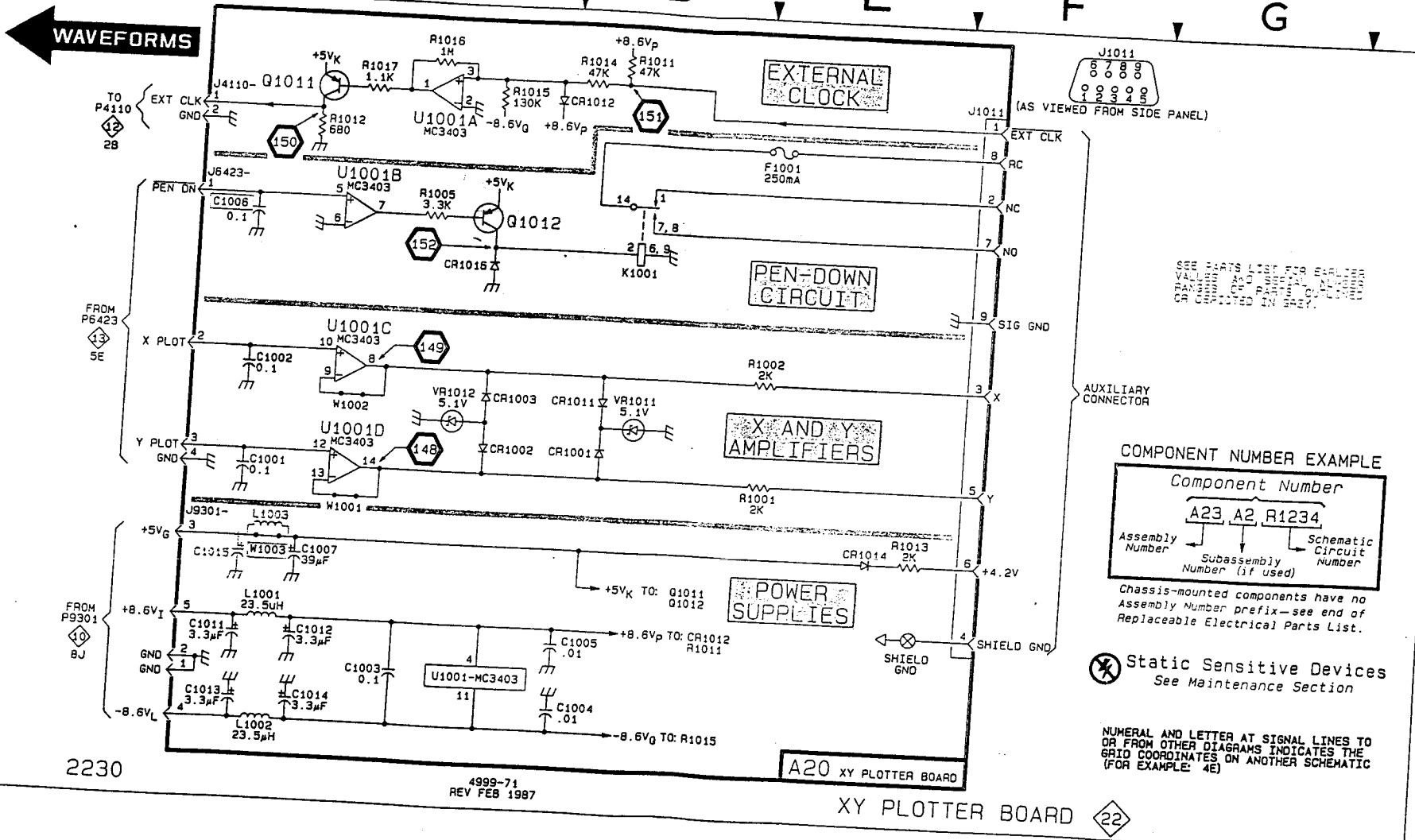
4999-78

XY PLOTTER BOARD DIAGRAM 22

ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1001	3B	2B	F1001	1E	2B	R1012	1B	2C
C1002	2B	2B				R1013	3E	2C
C1003	4C	2A	J1011	1F	1C	R1014	1D	2C
C1004	4D	2A	J4110	1B	1A	R1015	1C	2C
C1005	4D	2A	J6423	1B	1A	R1016	1C	2C
C1006	2B	2A	J9301	3B	2A	R1017	1B	1B
C1007	3B	2A						
C1011	4B	2B	K1001	2D	2B	U1001A	1C	1A
C1012	4B	3B				U1001B	1B	1A
C1013	4B	3B	L1001	4B	2A	U1001C	2B	1A
C1014	4B	3B	L1002	4B	3A	U1001D	3B	1A
C1015*	3B	3B	L1003*	3B	3A	U1001	4C	1A
CR1001	3D	1B	Q1011	1B	2A	VR1011	2D	1C
CR1002	3C	1B	Q1012	2C	2B	VR1012	2C	1C
CR1003	2C	2B						
CR1011	2D	2B	R1001	3E	1B	W1001	3B	1A
CR1012	1D	2B	R1002	2E	1B	W1002	3B	2B
CR1014	3E	2C	R1005	1C	2B	W1003*	3B	3A
CR1016	2C	2B	R1011	1D	2C			

*See Parts List for serial number ranges.


WAVEFORMS
EXTERNAL CLOCK
PEN-DOWN CIRCUIT
X AND Y AMPLIFIERS
POWER SUPPLIES
Q1011
Q1012
U1001A MC3403
U1001B MC3403
U1001C MC3403
U1001D MC3403
U1001-MC3403
K1001
F1001 250mA
J1011
(AS VIEWED FROM SIDE PANEL)
EXT CLK
RC
NC
NO
SIG GND
X
Y
+4.2V
SHIELD GND
AUXILIARY CONNECTOR
TO P4110
FROM P6423
FROM P9301
X PLOT
Y PLOT
PEN DN
+5V_K
+8.6V_P
-8.6V_G
+5V_G
+8.6V_I
-8.6V_L
GND
SHIELD GND
+5V_K TO: Q1011 Q1012
+8.6V_P TO: CR1012 R1011
-8.6V_G TO: R1015
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OMITTED OR CHANGED IN REV.
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)
A20 XY PLOTTER BOARD
2230
4999-71
REV FEB 1987
XY PLOTTER BOARD 22

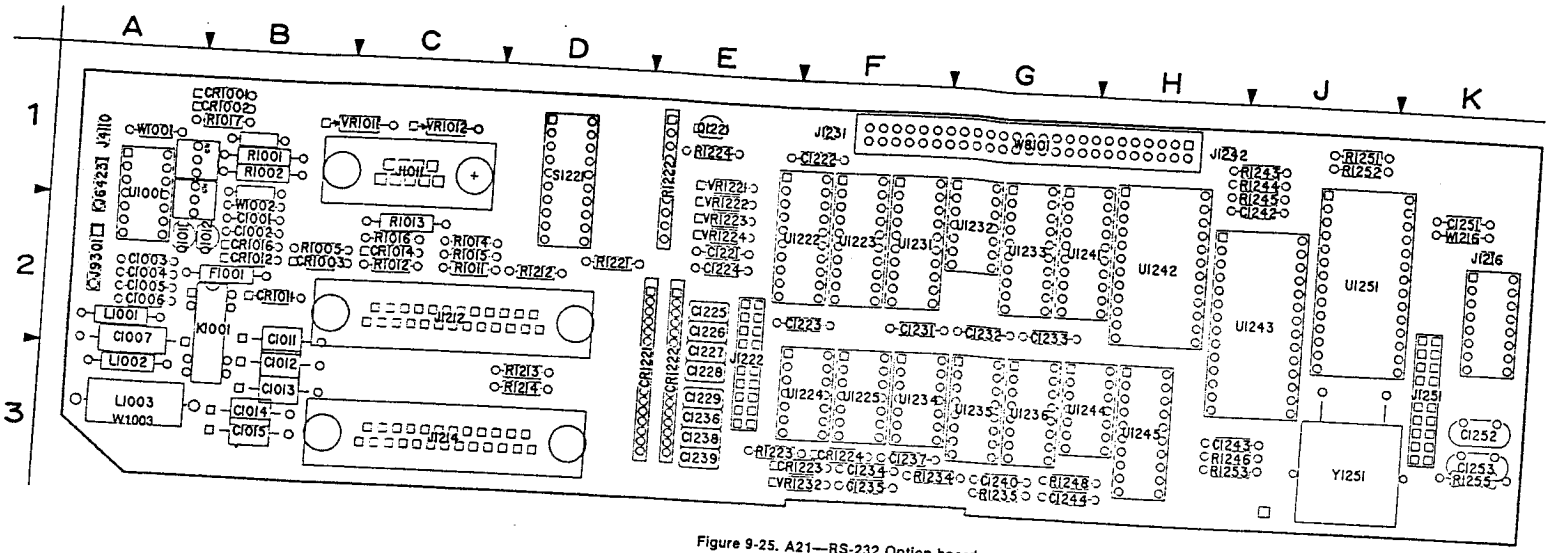
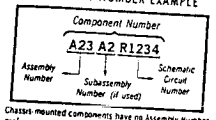


Figure 9-25. A21—RS-232 Option board.

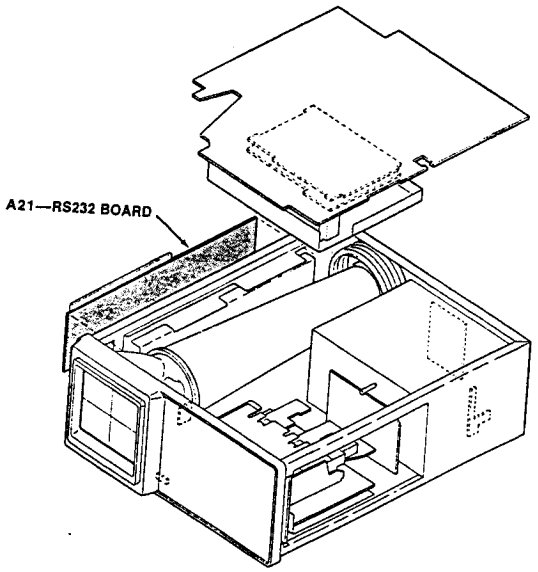
4999-30A

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



REV FEB 1987

A21—RS-232 OPTION BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C1001	23	C1251	23	Q1011	23		
C1002	23	C1252	23	Q1012	23	U1001	23
C1003	23	C1253	23	Q1221	23	U1222	23
C1004	23					U1223	23
C1005	23	CR1001	23	R1001	23	U1224	23
C1006	23	CR1002	23	R1002	23	U1225	23
C1007	23	CR1003	23	R1005	23	U1231	23
C1011	23	CR1011	23	R1011	23	U1232	23
C1012	23	CR1012	23	R1012	23	U1233	23
C1013	23	CR1014	23	R1013	23	U1234	23
C1014	23	CR1016	23	R1014	23	U1235	23
C1015	23	CR1221	23	R1015	23	U1236	23
C1221	23	CR1222	23	R1016	23	U1241	23
C1222	23	CR1223	23	R1017	23	U1242	23
C1223	23	CR1224	23	R1212	23	U1243	23
C1224	23			R1213	23	U1244	23
C1225	23	F1001	23	R1214	23	U1245	23
C1226	23			R1221	23	U1251	23
C1227	23	J1011	23	R1222	23		
C1228	23	J1212	23	R1223	23	VR1011	23
C1229	23	J1214	23	R1224	23	VR1012	23
C1231	23	J1216	23	R1234	23	VR1221	23
C1232	23	J1222	23	R1235	23	VR1222	23
C1233	23	J1251	23	R1243	23	VR1223	23
C1234	23	J4110	23	R1244	23	VR1224	23
C1235	23	J6423	23	R1245	23	VR1232	23
C1236	23	J9301	23	R1246	23		
C1237	23			R1248	23	W1001	23
C1238	23	K1001	23	R1251	23	W1002	23
C1239	23			R1252	23	W1003	23
C1240	23	L1001	23	R1253	23	W1216	23
C1242	23	L1002	23	R1255	23	W8101	23
C1243	23	L1003	23				
C1244	23			S1221	23	Y1251	23

RS-232 OPTION BOARD DIAGRAM 23

ASSEMBLY A21

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1001	8J	2B	CR1003	8K	2B	R1017	7L	1B	U1234A	6F	3F
C1002	8J	2B	CR1011	8L	2B	R1212	2K	2D	U1234B	3J	3F
C1003	8B	2A	CR1012	7M	2B	R1213	2K	3D	U1234C	6D	3F
C1004	8C	2A	CR1014	8M	2C	R1214	3K	3D	U1234D	4B	3F
C1005	8C	2A	CR1016	7K	2B	R1221	5L	2D	U1234	8F	3F
C1006	7J	2A	CR1221	1L	2E	R1222	5L	1E	U1235	5E	3G
C1007	7B	2A	CR1222	3L	2E	R1223	4J	3E	U1235	7F	3G
C1011	8B	2B	CR1223	8D	3F	R1224	5K	1E	U1236	6G	3G
C1012	8B	3B	CR1224	8D	3F	R1234	5B	3G	U1236	8F	3G
C1013	8B	3B				R1235	6C	3G	U1241	2B	1G
C1014	8B	3B	F1001	7M	2B	R1243	4B	1J	U1241	8E	1G
C1015*	7B	3B				R1244	3B	1J	U1242	1F	1H
C1221	3K	2E	J1011	7M	1C	R1245	3B	1J	U1242	7D	1H
C1222	7C	1F	J1212	3M	2C	R1246	5F	3J	U1243	3F	1J
C1223	7C	2F	J1214	1M	3C	R1248	6E	3G	U1243	7C	1J
C1224	1K	2E	J1216	4C	1K	R1251	4B	1J	U1244A	6D	3H
C1225	3K	2E	J1222	1D	2E	R1252	4B	1J	U1244B	7D	3H
C1226	3K	2E	J1251	2D	2K	R1253	2E	3J	U1244C	7F	3H
C1227	2K	2E	J4110	7J	1A	R1255	2G	3K	U1244D	3K	3H
C1228	3K	2E	J6423	7J	1A				U1244E	5C	3H
C1229	2K	3E	J9301	8J	2A	S1221	5M	1D	U1244F	3G	3H
C1231	7C	2F							U1244	8F	3H
C1232	7C	1G	K1001	7M	2B	U1001A	7L	1A	U1245	6E	3H
C1233	7C	1G				U1001B	7K	1A	U1245	8E	3H
C1234	8D	3F	L1001	8B	2A	U1001C	7J	1A	U1251	1H	1J
C1235	8D	3F	L1002	8B	3A	U1001D	8K	1A	U1251	7D	1J
C1236	2K	3E	L1003*	7B	3A	U1001	8C	1A			
C1237	8D	3F				U1222	6J	2F	VR1011	8L	1C
C1238	2K	3E	Q1011	7K	2A	U1222	7E	2F	VR1012	8K	1C
C1239	1J	3E	Q1012	7K	2B	U1223	5H	2F	VR1221	1L	1E
C1240	7C	3G	Q1221	5K	1E	U1223	8E	2F	VR1222	1L	1E
C1242	7C	1J				U1224	2J	3F	VR1223	4L	1E
C1243	7C	3J	R1001	8L	1B	U1224	8D	3F	VR1224	3L	2E
C1244	7C	3G	R1002	8L	1B	U1225	1J	3F	VR1232	8D	3F
C1251	7C	1K	R1005	7K	2B	U1225	8D	3F			
C1252	2G	3K	R1011	7M	2C	U1231	1B	2F	W1001	8K	1A
C1253	3G	3K	R1012	7L	2C	U1231	8E	2F	W1002	8K	2B
			R1013	8M	2C	U1232A	7F	1G	W1003*	7B	3A
CR1001	8L	1B	R1014	7M	2C	U1232	7F	1G	W1216	4B	1K
CR1002	8K	1B	R1015	7M	2C	U1233	3B	1G	W8101	1A	1G
			R1016	6L	2C	U1233	8E	1G			
									Y1251	2G	3J

CHASSIS MOUNTED PARTS

P8100	1A	CHASSIS									

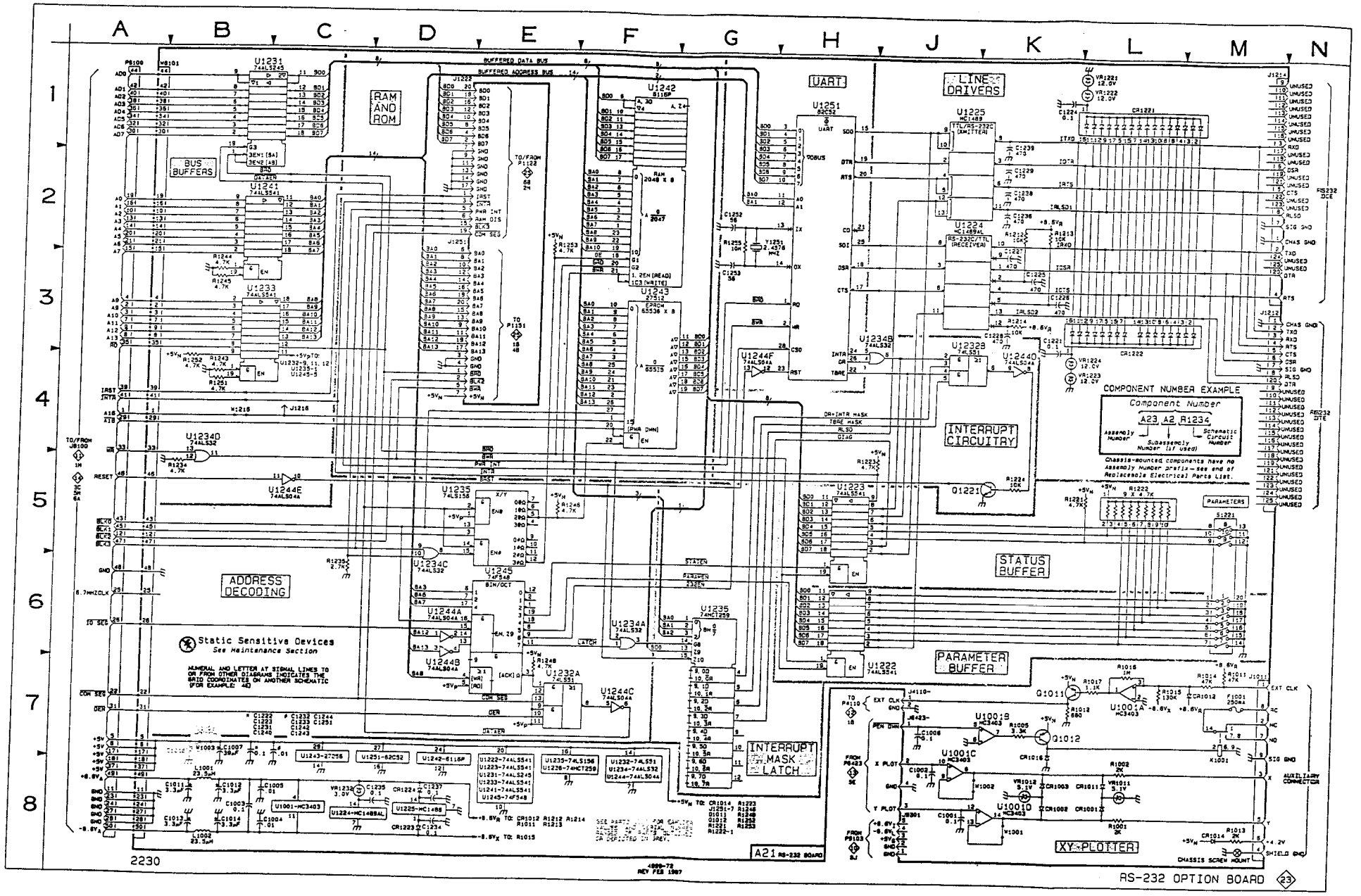
*See Parts List for serial number ranges.

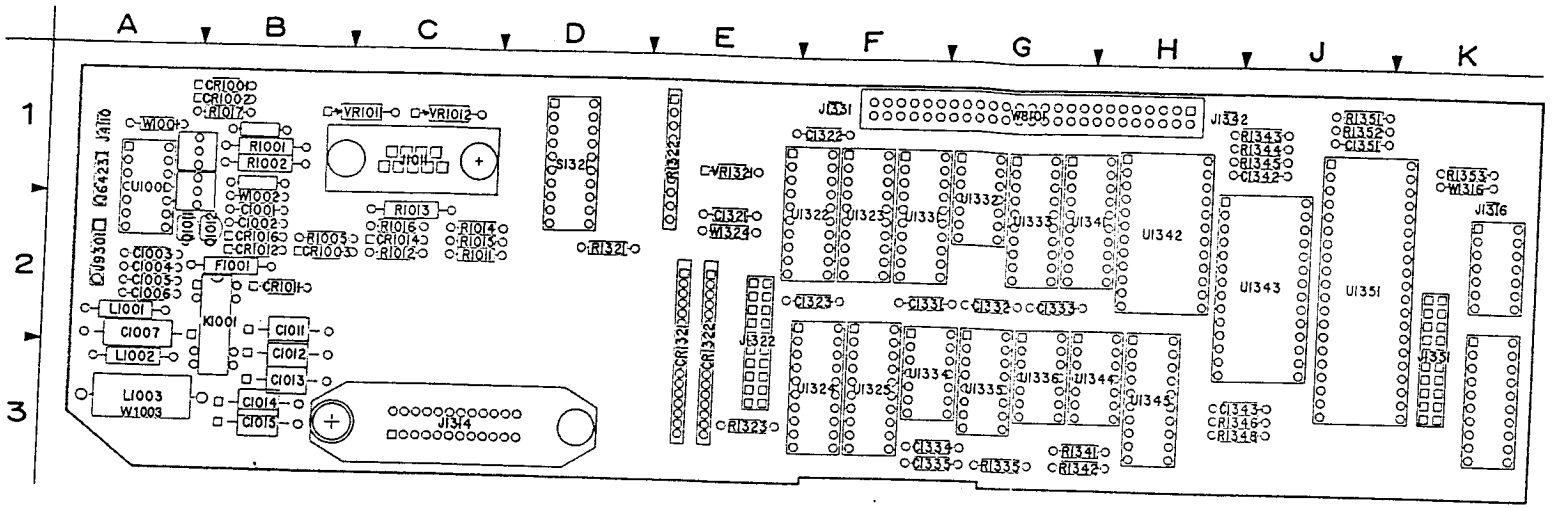
A11A2—VECTOR GENERATOR BOARD

WAVEFORMS FOR DIAGRAM 21

A20—XY PLOTTER BOARD FIG. 9-24

A21—RS-232 OPTION BOARD FIG. 9-25




A
B
C
D
E
F
G
H
J
K
1
2
3
W100
CR1001
CR1002
R1017
VR1011
VR1012
R1001
R1002
W1002
C1001
C1002
C1016
CR1012
R1005
CR1003
R1013
R1016
CR1014
R1014
R1015
R1012
R1011
C1003
C1004
C1005
C1006
F1001
CR101
L1001
C1007
L1002
K1001
C1011
C1012
C1013
C1014
C1015
L1003
W1003
J1314
R1321
CR1322
CR1321
CR1316
VR1321
C1321
W1324
C1322
C1323
J1322
J1351
J4110
J6423
J9301
J1331
W8101
J1332
C1331
C1332
C1333
C1334
C1335
C1342
C1343
C1351
R1351
R1352
C1351
R1343
R1344
R1345
R1346
R1348
R1342
R1341
R1335
C1334
C1335
R1353
W1316
J1316
U1322
U1323
U1331
U1332
U1333
U1334
U1335
U1336
U1341
U1342
U1343
U1344
U1345
U1351
U1342
U1343
U1351
C1343
C1346
C1348
U1324
U1325
U1344
C1341
C1342
R1341
R1342
C1341
C1342
C1343
C1344
C1345
C1346
C1347
C1348
C1349
C1350
C1351
C1352
C1353
C1354
C1355
C1356
C1357
C1358
C1359
C1360
C1361
C1362
C1363
C1364
C1365
C1366
C1367
C1368
C1369
C1370
C1371
C1372
C1373
C1374
C1375
C1376
C1377
C1378
C1379
C1380

GPIB OPTION BOARD DIAGRAM 24

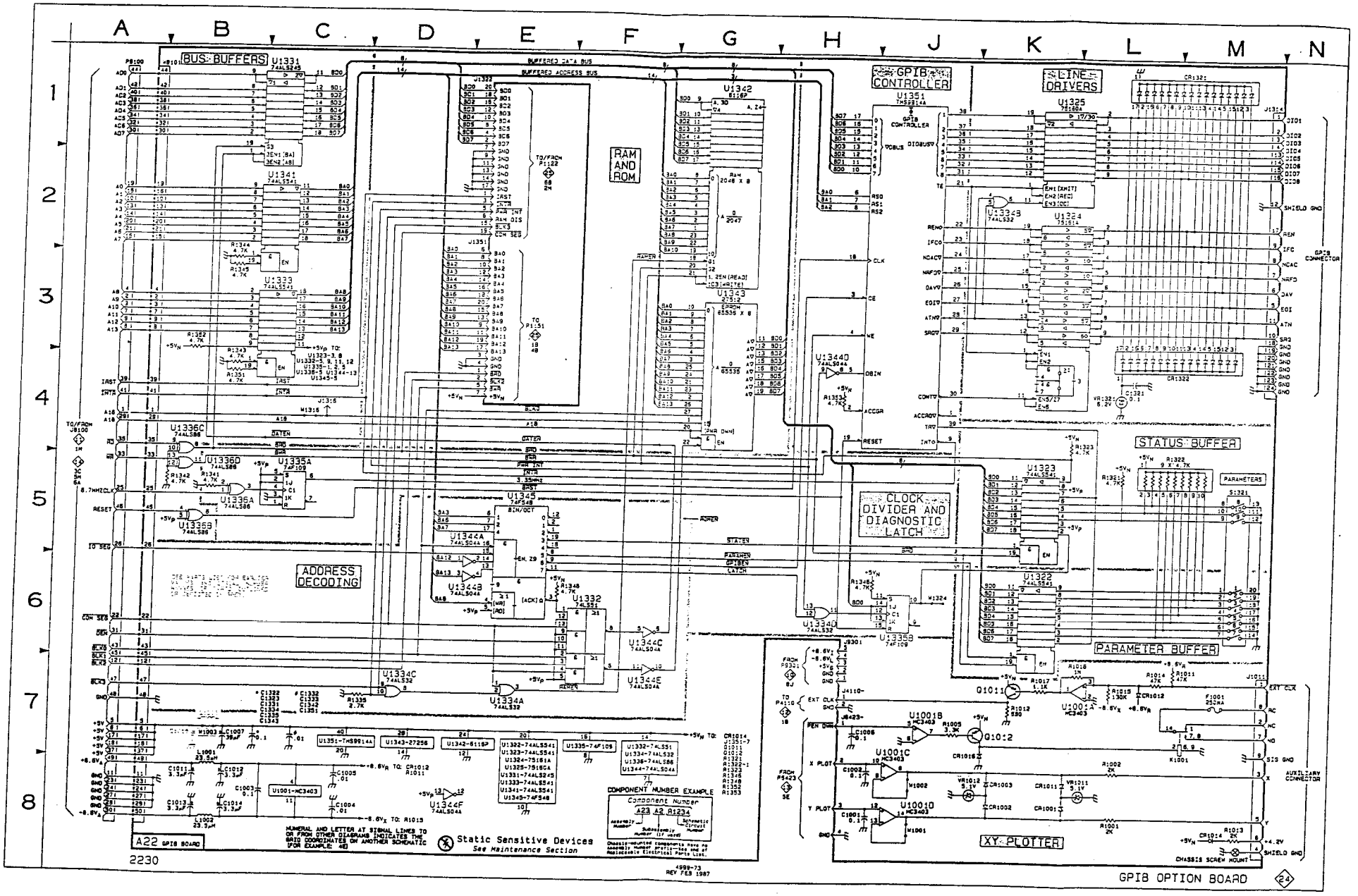
ASSEMBLY A22

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1001	8J	2B	J1011	7M	1C	R1344	2B	1J	U1335B	6J	3G
C1002	7J	2B	J1314	1M	3C	R1345	3B	1J	U1335	7F	3G
C1003	8C	2A	J1316	4C	1K	R1346	6J	3J	U1336A	5B	3G
C1004	8C	2A	J1322	1E	2E	R1348	6F	3J	U1336B	5B	3G
C1005	8C	2A	J1351	2E	2K	R1351	4B	1J	U1336C	4B	3G
C1006	7H	2A	J4110	7H	1A	R1352	3B	1J	U1336D	5B	3G
C1007	7B	2A	J6423	7H	1A	R1353	4H	1K	U1336	7F	3G
C1011	8B	2B	J9301	6H	2A				U1341	2C	2G
C1012	8B	3B				S1321	5M	1D	U1341	8E	2G
C1013	8B	3B	K1001	7M	2B				U1342	1G	2H
C1014	8B	3B				U1001A	7L	1A	U1342	7E	2H
C1015*	7B	3B	L1001	7B	2A	U1001B	7J	1A	U1343	3G	2J
C1321	4L	2E	L1002	8B	3A	U1001C	7J	1A	U1343	7D	2J
C1322	7C	1F	L1003*	7B	3A	U1001D	8J	1A	U1344A	5E	3H
C1323	7C	2F				U1001	8C	1A	U1344B	6E	3H
C1331	7C	2F	Q1011	7K	2A	U1322	6K	2F	U1344C	6F	3H
C1332	7C	2G	Q1012	7K	2B	U1322	7E	2F	U1344D	3H	3H
C1333	7C	2G				U1323	5K	2F	U1344E	7F	3H
C1334	7C	3F	R1001	7L	1B	U1323	7E	2F	U1344F	8D	3H
C1335	7C	3F	R1002	8L	1B	U1324	2K	3F	U1344	8F	3H
C1342	7C	1J	R1005	7J	2B	U1324	7E	3F	U1345	5E	3H
C1343	7C	3J	R1011	7M	2C	U1325	1K	3F	U1345	8E	3H
C1351	7C	1J	R1012	7K	2C	U1325	8E	3F	U1351	1J	2J
			R1013	8M	2C	U1331	1C	2F	U1351	7C	2J
CR1001	8K	1B	R1014	7L	2C	U1331	8E	2F			
CR1002	8K	1B	R1015	7L	2C	U1332	6F	1G	VR1011	8L	1C
CR1003	8K	2B	R1016	7L	2C	U1332	7F	1G	VR1012	8K	1C
CR1011	8K	2B	R1017	7K	1B	U1333	3C	2G	VR1321	4L	1E
CR1012	7L	2B	R1321	5L	2D	U1333	8E	2G			
CR1014	8M	2C	R1322	4M	1E	U1334A	7E	3F	W1001	8J	1A
CR1016	7K	2B	R1323	4L	3E	U1334B	2K	3F	W1002	8J	2B
CR1321	1M	2E	R1335	7D	3G	U1334C	7D	3F	W1003*	7B	3A
CR1322	4M	2E	R1341	5B	3G	U1334D	6H	3F	W1316	4C	1K
			R1342	5B	3G	U1334	7F	3F	W1324	6J	2E
F1001	7M	2B	R1343	4B	1J	U1335A	5C	3G	W8101	1A	1G

CHASSIS MOUNTED PARTS

P8100	1A	CHASSIS									

***See Parts List for serial number ranges.**


BUS BUFFERS
GPIB CONTROLLER
LINE DRIVERS
RAM AND ROM
ADDRESS DECODING
CLOCK DIVIDER AND DIAGNOSTIC LATCH
STATUS BUFFER
PARAMETER BUFFER
XY PLOTTER
A22 GPIB BOARD
2230
Static Sensitive Devices
See Maintenance Section
GPIB OPTION BOARD
24

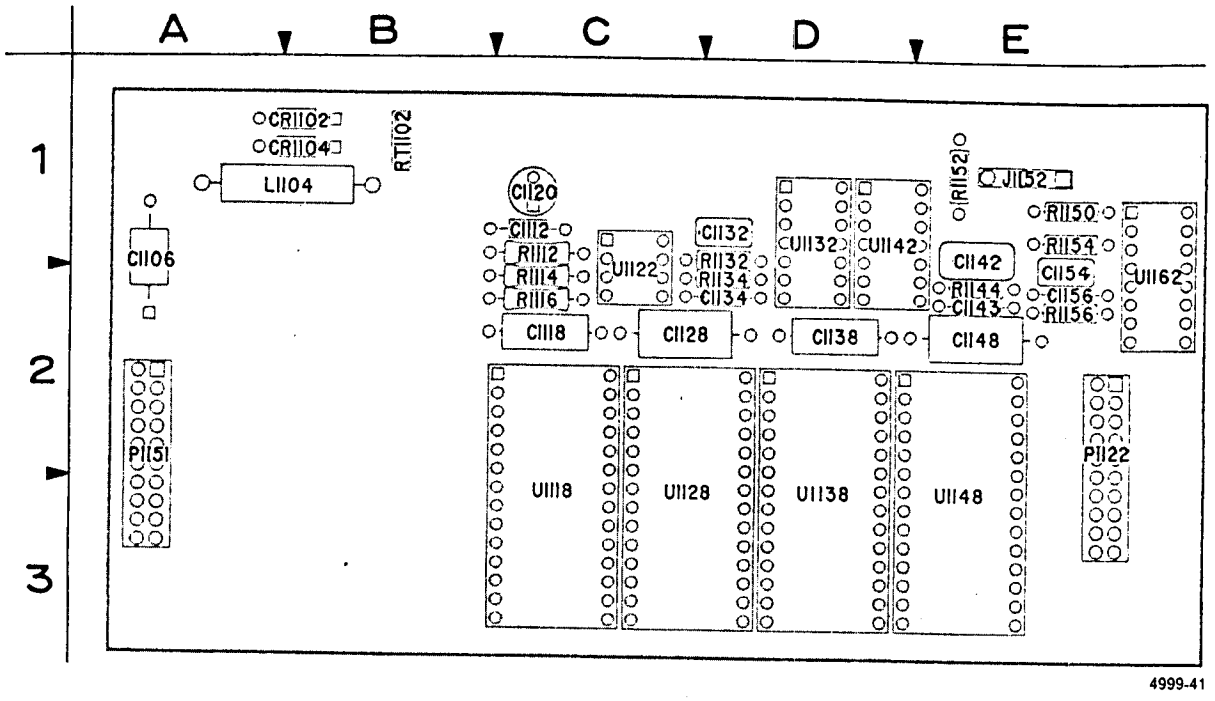
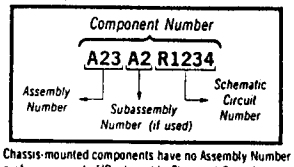


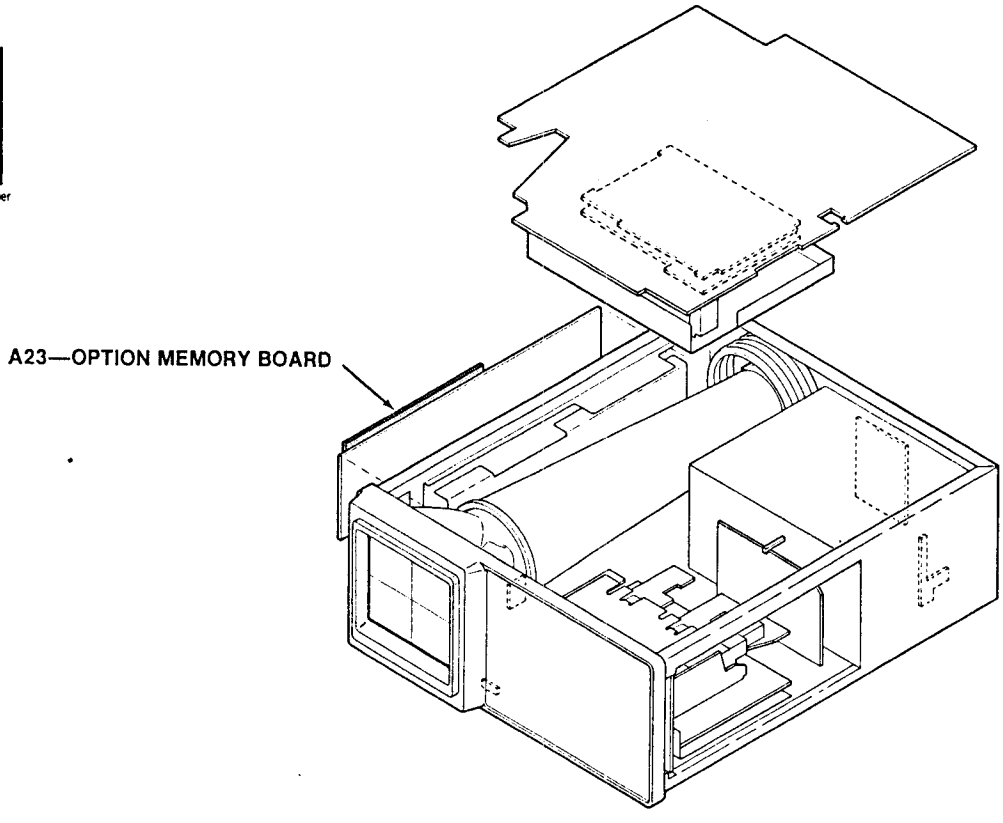
Figure 9-27. A23—Option Memory board.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of 'Replaceable Electrical Parts List.



A23—OPTION MEMORY BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C1106	25	CR1104	25	R1150	25	U1132	25
C1112	25	J1152	25	R1152	25	U1132	25
C1118	25	L1104	25	R1154	25	U1132	25
C1120	25	P1122	25	R1156	25	U1138	25
C1128	25	P1122	25	RT1102	25	U1138	25
C1132	25	P1151	25	U1118	25	U1142	25
C1134	25	P1151	25	U1118	25	U1142	25
C1138	25	R1112	25	U1122	25	U1142	25
C1142	25	R1114	25	U1128	25	U1148	25
C1143	25	R1116	25	U1128	25	U1148	25
C1148	25	R1132	25	U1132	25	U1162	25
C1154	25	R1132	25	U1132	25	U1162	25
C1156	25	R1134	25	U1132	25		
CR1102	25	R1144	25	U1132	25		

OPTION MEMORY DIAGRAM 25

ASSEMBLY A23

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1106	1B	1A	P1122	2M	2E	U1122	1E	2C
C1112	1D	1C	P1122	6B	2E	U1128	3E	3C
C1118	1F	2C	P1151	1B	2A	U1128	6K	3C
C1120	1C	1C	P1151	4B	2A	U1132B	2G	1D
C1128	2E	2C				U1132C	3H	1D
C1132	2G	1D	R1112	1C	1C	U1132D	3J	1D
C1134	1F	2D	R1114	1C	2C	U1132E	3J	1D
C1138	2E	2D	R1116	2C	2C	U1132F	3K	1D
C1142	3J	1E	R1132	2G	1D	U1132	3F	1D
C1143	1F	2E	R1134	1G	2D	U1138	3D	3D
C1148	2D	2E	R1144	3H	2E	U1138	6H	3D
C1154	3K	1E	R1150	1K	1E	U1142A	2K	1D
C1156	1F	2E	R1152	1K	1E	U1142B	2K	1D
			R1154	3J	1E	U1142D	3K	1D
CR1102	2C	1B	R1156	3K	2E	U1142	1F	1D
CR1104	2C	1B				U1148	3D	3E
			RT1102	3B	1B	U1148	6F	3E
J1152	2B	1E				U1162	1F	1E
			U1118	3F	3C	U1162	5C	1E
L1104	1C	1A	U1118	6M	3C			

CHASSIS MOUNTED PARTS

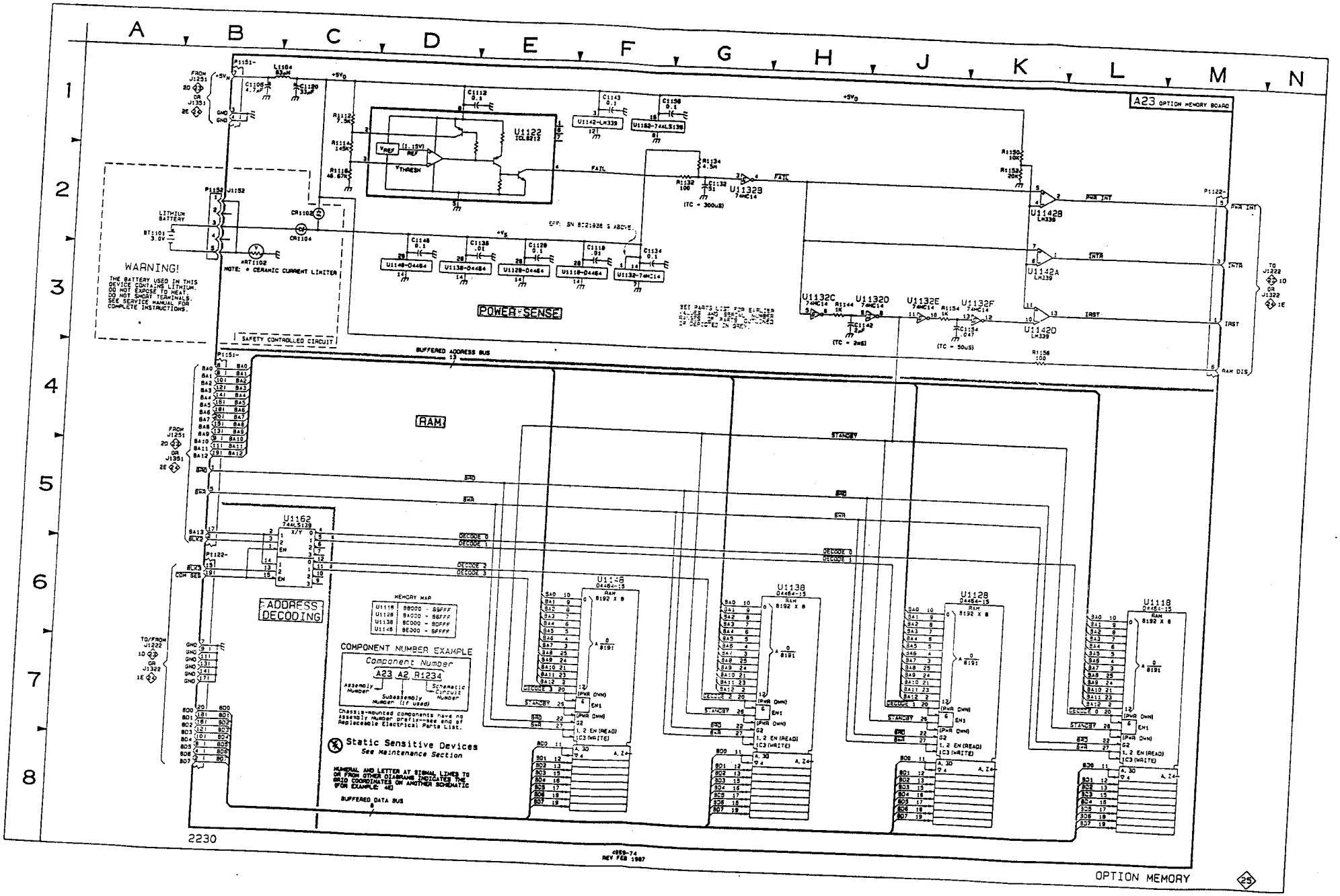
BT1101	2A	CHASSIS	P1152	2A	CHASSIS			

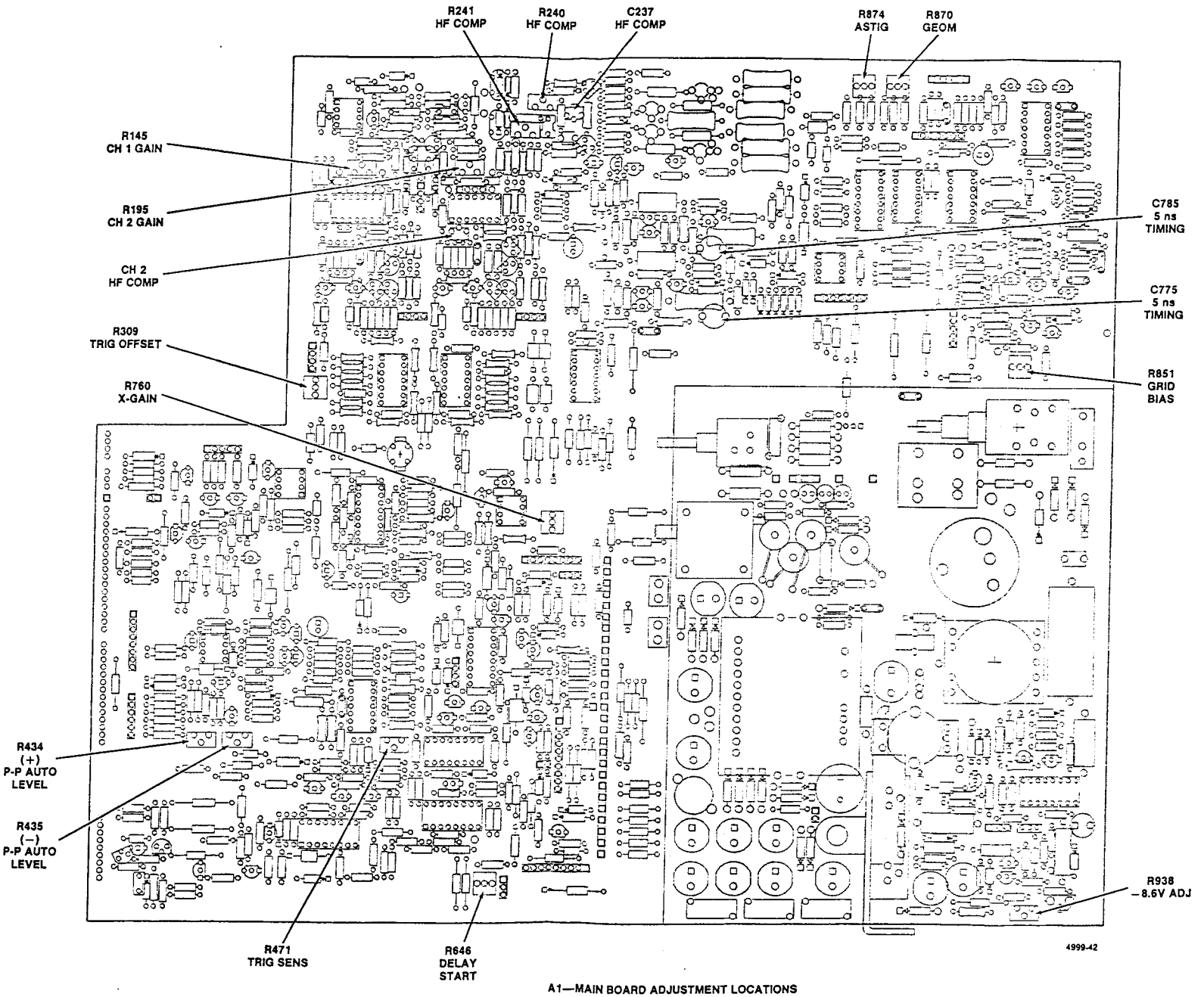
A22—GPIB OPTION BOARD

A23—OPTION MEMORY BOARD

FIG. 9-27

A20—XY PLOTTER BOARD





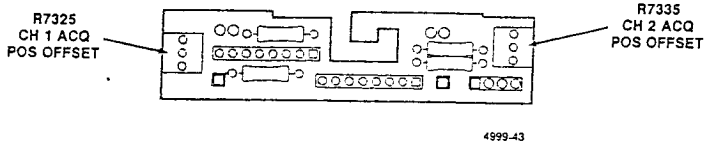
A1—MAIN BOARD ADJUSTMENT LOCATIONS

A22—GPIB OPTION BOARD

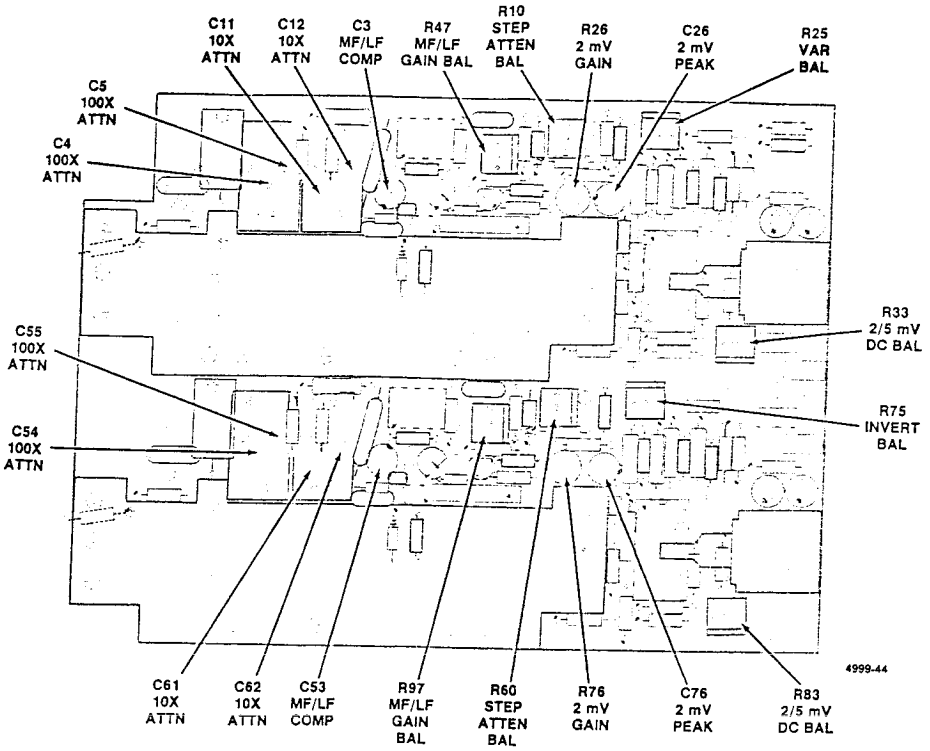
A23—OPTION MEMORY BOARD
FIG. 9-27

A22—GPIB OPTION BOARD

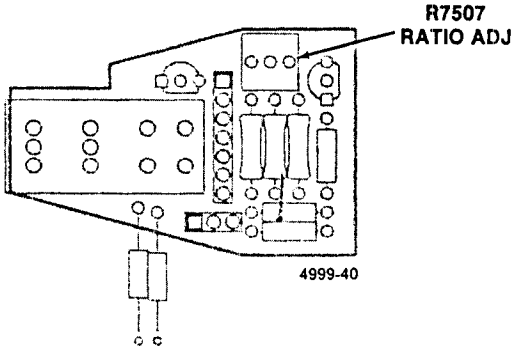
A23—OPTION MEMORY BOARD
FIG. 9-27



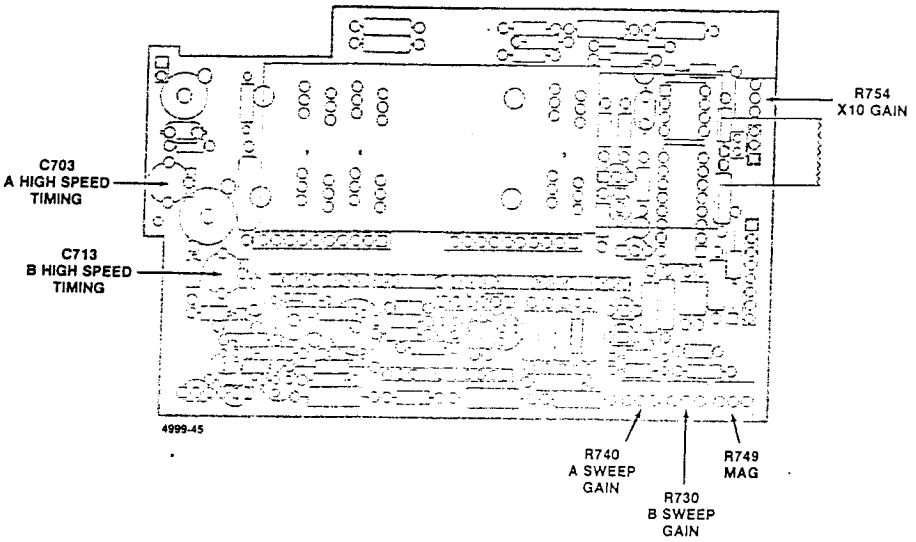
A17—POSITION INTERFACE ADJUSTMENT LOCATIONS



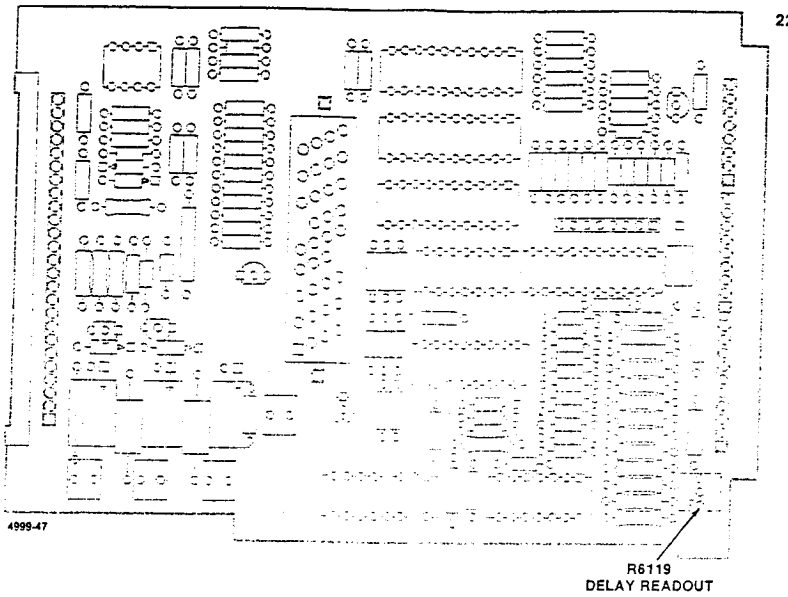
A2—ATTENUATOR BOARD ADJUSTMENT LOCATIONS



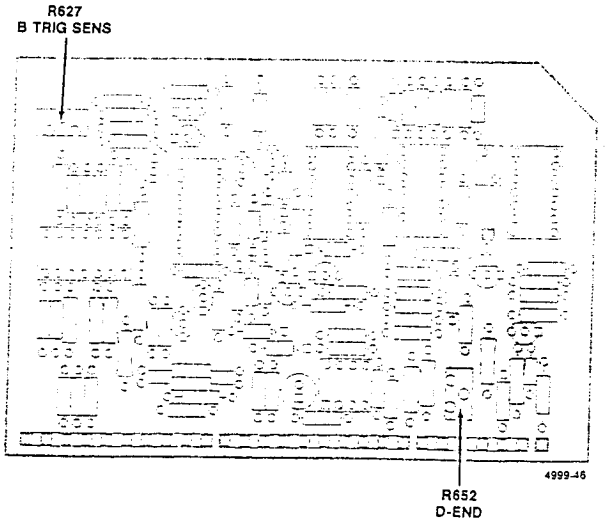
A16—SWEEP REFERENCE ADJUSTMENT LOCATION



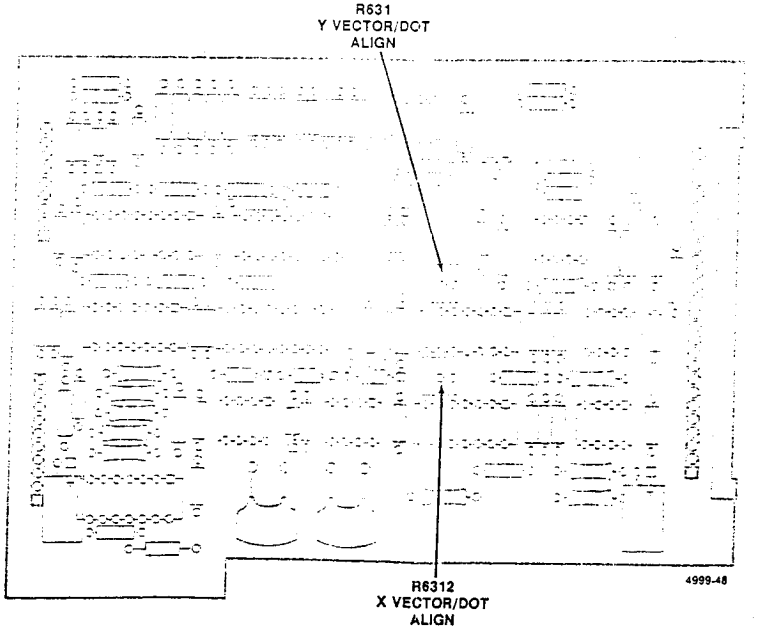
A4—TIMING BOARD ADJUSTMENT LOCATIONS



A11A1—INPUT/OUTPUT ADJUSTMENT LOCATION

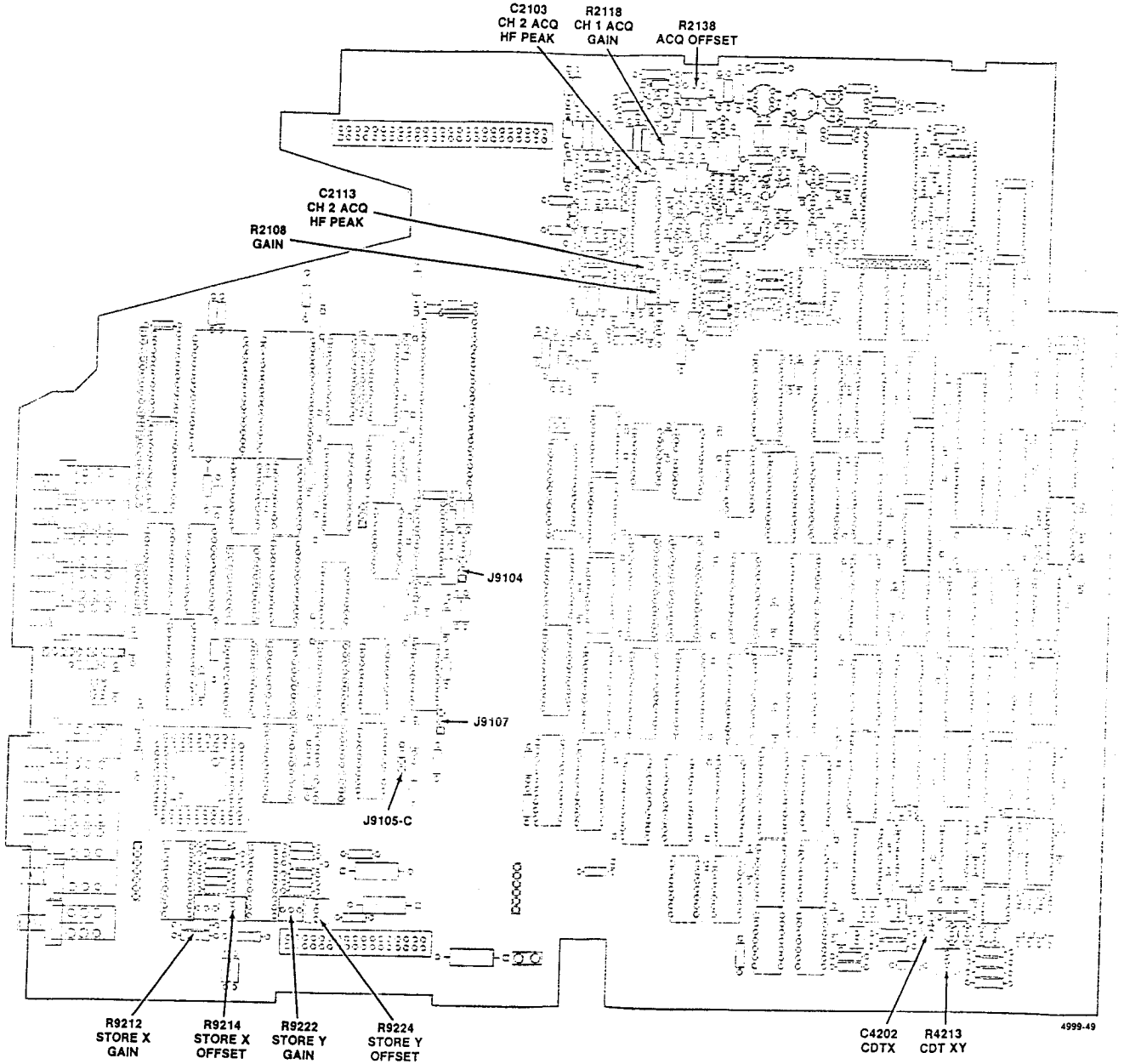


A5—ALT SWEEP LOGIC BOARD ADJUSTMENT LOCATIONS



A11A2—VECTOR GENERATOR ADJUSTMENT LOCATIONS

WAVEFORMS FOR DIAGRAM 11
A11A2—VECTOR GENERATOR
A23—OPTION MEMORY BOARD
FIG. 9-27
A20—XY PLOTTER BOARD
A8—LINE FILTER, A16—THERMAL
WAVEFORMS FOR DIAGRAM 16



A10—STORAGE BOARD ADJUSTMENT LOCATIONS

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5	*Name & Description*
Assembly and/or Component	
Attaching parts for Assembly and/or Component	
	**** END ATTACHING PARTS ****
Detail Part of Assembly and/or Component	
Attaching parts for Detail Part	
	**** END ATTACHING PARTS ****
Parts of Detail Part	
Attaching parts for Parts of Detail Part	
	**** END ATTACHING PARTS ****

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

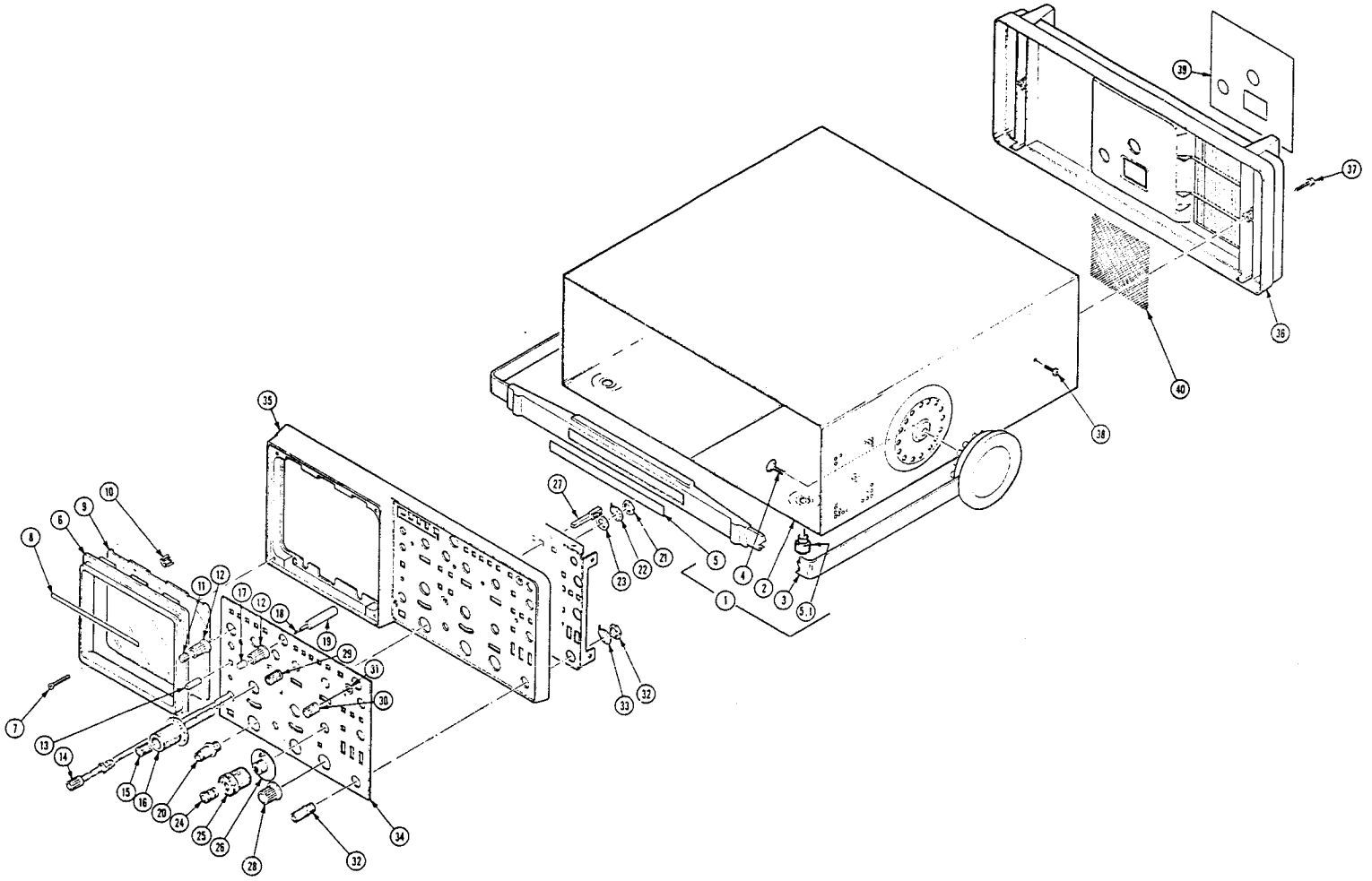
"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

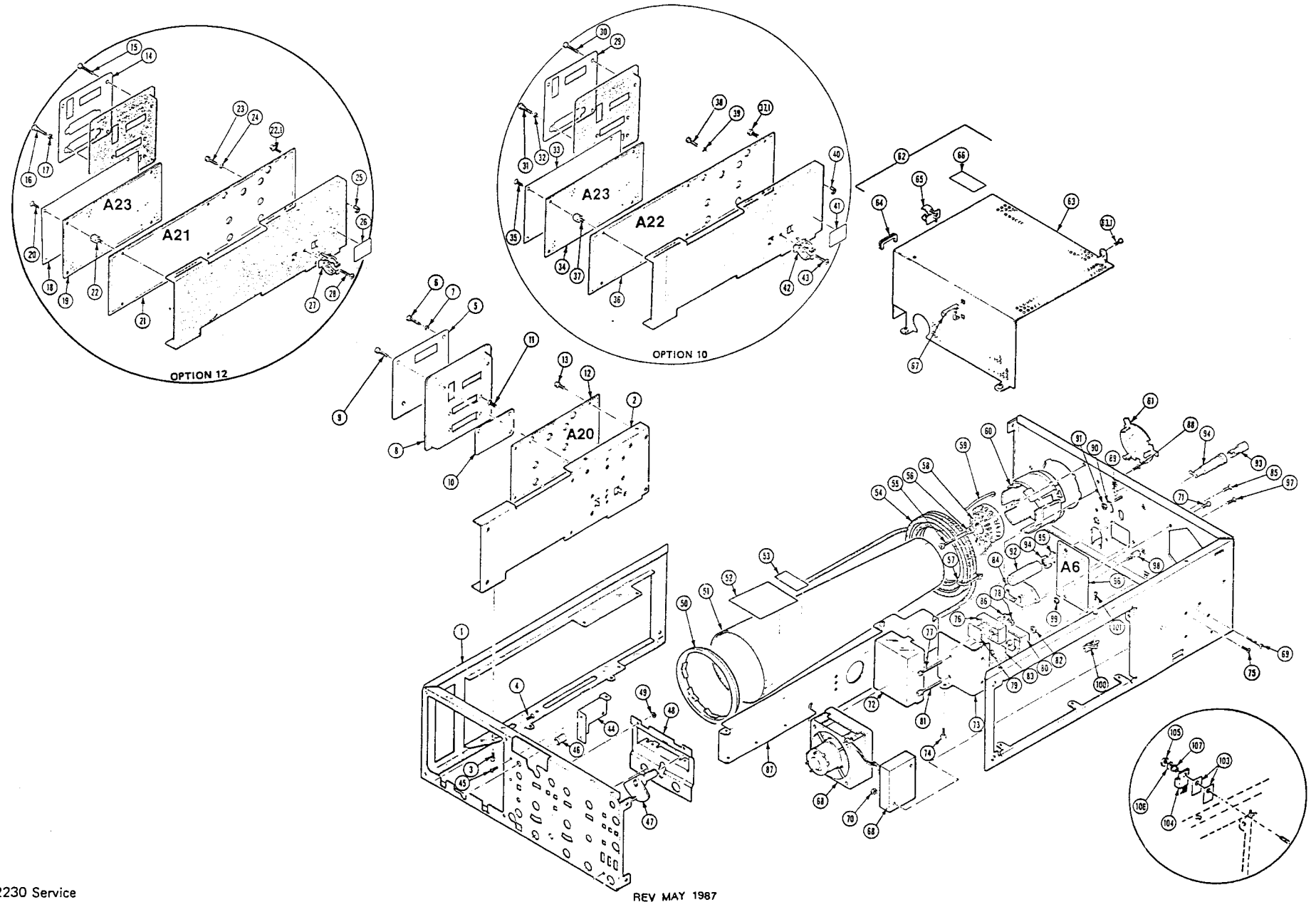
CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Manufacturer	Address	City, State, Zip Code
GENERAL ELECTRIC CO FOOD SERVICE EQUIPMENT BUSINESS DEPT	14TH AND ARNOLD STS	CHICAGO HEIGHTS IL 60411
TEXTRON INC CAMCAR DIV SEMS PRODUCTS UNIT	1818 CHRISTINA ST	ROCKFORD IL 61108
PANDUIT CORP	17301 RIDGELAND	TINLEY PARK IL 60477
RICHCO PLASTIC CO	5825 N TRIPP AVE	CHICAGO IL 60646
NELSON NAME PLATE CO	3191 CASITAS	LOS ANGELES CA 90039
BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
FREEWAY CORP	9301 ALLEN DR	CLEVELAND OH 44125
THERMALLOY CO INC	2021 W VALLEY VIEW LANE P O BOX 34829	DALLAS TX 75234
BELDEN CORP ELECTRONIC DIV	2200 US HWY 27 SOUTH P O BOX 1980	RICHMOND IN 47374
CHOMERICS INC	77 DRAGON COURT	WOBURN MA 01801
G M NAMEPLATE INC	2040 15TH AVE WEST	SEATTLE WA 98119
AMUNEAL MFG CORP	4737 DARRAH	PHILADELPHIA PA 19124
SPECIALTY CONNECTOR CO INC	2620 ENDRESS PLACE P O BOX D	GREENWOOD IN 46142
BELDEN CORP	2000 S BATAVIA AVE	GENEVA IL 60134
BUSSMANN MFG CO	114 OLD STATE RD	ST LOUIS MO 63178
MCGRAW EDISION CO	PO BOX 14460 ·	
FISCHER SPECIAL MFG CO	446 MORGAN ST	CINCINNATI OH 45206
KMC STAMPING DIV. OF KICKHAEFER MFG. CO.	1219 S. PART ST.	PORT WASHINGTON, WI 53074
SHAKEPROOF DIV OF ILLINOIS TOOL WORKS	SAINT CHARLES RD	ELGIN IL 60120
ILLINOIS TOOL WORKS INC SHAKEPROOF DIVISION	ST CHARLES ROAD	ELGIN IL 60120
TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
ELECTRICAL SPECIALITY CO SUBSIDIARY OF BELDEN CORP	213 E HARRIS AVE	SOUTH SAN FRANCISCO CA 94080
MICRODOT MANUFACTURING INC GREER-CENTRAL DIV	3221 W BIG BEAVER RD	TROY MI 48098
ELCO INDUSTRIES INC	1101 SAMUELSON RD	ROCKFORD IL 61101
MICRODOT MFG INC CENTRAL SCREW- KEENE DIV	149 EMERALD ST	KEENE NH 03431
SEASTROM MFG CO INC	701 SONORA AVE	GLENDALE CA 91201
MALLORY CAPACITOR CO DIV P R MALLORY AND CO INC	4760 KENTUCKY AVE P O BOX 372	INDIANAPOLIS IN 46206
TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61101
FELLER ASA ADOLF AG C/O PANEL COMPONENTS CORP	355 TESCONI CIRCLE	SANTA ROSA CA 95401
SCHURTER AG H C/O PANEL COMPONENTS CORP	2015 SECOND STREET	BERKELEY CA 94170
BADGLEY MFG CO	1620 NE ARGYLE	PORTLAND OR 97211
NORTHWEST FASTENER SALES INC	7923 SW CIRRUS DRIVE	BEAVERTON OR 97005
LEWIS SCREW CO	4114 S PEORIA	CHICAGO IL 60609
H SCHURTER AG DIST PANEL COMPONENTS	2015 SECOND STREET	BERKELEY CA 94170
EYELEMATIC MFG	BOX N SEEMAR RD	WATERTOWN CT 06795
NORTHWEST FOURSLIDE INC	5858 WILLOW LANE	LAKE OSWEGO OR 97034
PARSONS MFG CORP	1055 OBRIEN	MENLO PARK CA 94025
PATELEC-CEM (ITALY)	10156 TORINO	VAICENTALLO 62/45S ITALY
CAMCAR/TEXTRON	516 18TH AVE	ROCKFORD IL 61101
HERD MFG	9227 CLINTON RD	CLEVELAND OH 44144

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	644-0536-00			1	CABINET ASSY:	80009	644-0536-00
-2	437-0331-01			1	.CABINET,SCOPE:W/FEET	80009	437-0331-01
	348-0659-00			2	..FOOT,CABINET:BLACK POLYURETHANE	80009	348-0659-00
-3	367-0289-00			1	.HANDLE,CARRYING:13.855,SST (ATTACHING PARTS)	80009	367-0289-00
-4	212-0144-00			2	.SCREW,TPG,TF:8-16 X 0.562,PLATITE,SPCL HD (END ATTACHING PARTS)	93907	225-38131-012
-5	334-5965-00			1	.MARKER,IDENT:MKD TEKTRONIX	80009	334-5965-00
-5.1	348-0659-01	B010100	B011319	2	.FOOT,CABINET:BLACK POLYURETHANE	80009	348-0659-01
	348-0659-00	B011320		2	.FOOT,CABINET:BLACK POLYURETHANE	80009	348-0659-00
-6	426-1765-02			1	FRAME,CRT:POLYCARBONATE,GRAY (ATTACHING PARTS)	80009	426-1765-02
-7	211-0690-00			2	SCREW,MACHINE:6-32 X 0.875,PNH,STL (END ATTACHING PARTS)	83385	ORDER BY DESCR
-8	334-5966-00			1	MARKER,IDENT:MKD 2230 DGTL STOR SCOPE	80009	334-5966-00
	334-6213-00			1	MARKER,IDENT:MKD 2230 DGTL STOR SCOPE (OPTION 10,12 ONLY)	80009	334-6213-00
-9	337-2775-00			1	SHLD,IMPLOSION:FILTER,BLUE 2211/2213/2215	80009	337-2775-00
-10	348-0660-00			4	CUSHION,CRT:POLYURETHANE	80009	348-0660-00
-11	366-2087-00	B010100	B010339	2	KNOB:GRAY,0.14 ID X 0.28 OD X 0.32 H	80009	366-2087-00
	366-1391-02	B010340	B021268	1	KNOB:LT GY,0.081 ID X 0.28 OD X 0.32 H	80009	366-1391-02
	366-1391-04	B021269		1	KNOB:GRAY,0.3 OD X 0.14 ID X 0.32 H	80009	366-1391-04
-12	366-1879-01			3	KNOB:GRAY 0.5 OD X 0.531 H PLSTC	80009	366-1879-01
-13	366-0573-00			10	PUSH BUTTON:IVORY GY,0.186 SQ X 0.48 H	80009	366-0573-00
-14	384-1575-00			1	EXTENSION SHAFT:8.805 L,W/KNOB,PLASTIC	80009	384-1575-00
-15	366-0575-00			2	KNOB:GRAY,CAL,0.127 ID X 0.392 OD X 0.4 H	80009	366-0575-00
-16	366-2148-01			2	KNOB:GY,VOLTS/DIV,0.72 OD,0.79 HW/0.25 DIA	80009	366-2148-01
-17	366-1059-00			1	PUSH BUTTON:GRAY,0.227 OD X 0.3	80009	366-1059-00
-18	214-3697-00			1	PIN,STR,HEADED:0.075 DIA X 1.27 L,AL	80009	214-3697-00
-19	384-1669-00			1	EXTENSION SHAFT:0.312 OD X 1.58 L,AL	80009	384-1669-00
	210-1027-00	B010100	B020464	1	WASHER,FLAT:0.252 ID X 0.406 OD	80009	210-1027-00
	210-0905-00	B020465		1	WASHER,FLAT:0.256 ID X 0.438 OD X 0.05,BRS	83385	ORDER BY DESCR
-20	----- -----			2	CONN,RCPT,ELEC:BNC (SEE J9100,J9510 REPL) (ATTACHING PARTS)		
-21	220-0497-00			2	NUT,PLAIN,HEX:0.5-28 X 0.562 HEX,BRS CD PL	80009	220-0497-00
-22	210-0241-00			2	TERMINAL,LUG:0.515 ID,PLAIN,STL CD PL	80009	210-0241-00
-23	210-1039-00			2	WASHER,LOCK:0.521 ID,INT,0.025 THK,SST (END ATTACHING PARTS)	24931	ORDER BY DESCR
-24	366-0576-00			1	KNOB:MED GRAY,CAL,0.083 X 0.45 X 0.456	80009	366-0576-00
-25	366-1840-03	B010100	B010445	1	KNOB:GY,TIME/DIV,0.127 X 0.855 X 0.844	80009	366-1840-03
	366-1840-04	B010446		1	KNOB:GY,TIME/DIV,0.127 X 0.855 X 0.844	80009	366-1840-04
	213-0153-00	B010446		2	SETSCREW:5-40 X 0.125,STL	TK0392	ORDER BY DESCR
-26	366-1850-00			1	KNOB:CLEAR,0.252 ID X 1.2 OD X 0.383 H	80009	366-1850-00
-27	366-0574-00			11	PUSH BUTTON:IVORY GY,1.445 H,POLYCARBONATE	80009	366-0574-00
-28	366-2020-01			1	KNOB:0.252 X 0.581 X 0.612 W/SET SCREW	80009	366-2020-01
-29	366-2049-01			5	KNOB:GY,0.172 ID X 0.41 OD X 0.496 H W/BAR	80009	366-2049-01
-30	366-1146-00			2	KNOB:GY,0.127 ID X 0.392 OD X 0.466 H	80009	366-1146-00
-31	210-0940-00			2	WASHER,FLAT:0.25 ID X 0.375 OD X 0.02,STL	12327	ORDER BY DESCR
-32	----- -----			1	CONN,RCPT,ELEC: (SEE J9376 REPL)		
-33	210-0255-00			1	TERMINAL,LUG:0.391 ID,LOCKING,BRS CD PL	12327	ORDER BY DESCR
-34	333-3161-00			1	PANEL,FRONT:	80009	333-3161-00
-35	386-4850-02			1	SUBPANEL,FRONT:	80009	386-4850-02
-36	200-2538-09			1	COVER,REAR:W/MARKERS	80009	200-2538-09
	343-1278-00	B010624		2	RTNR,POWER CORD:POLYCARBONATE GRAY (ATTACHING PARTS)	80009	343-1278-00
-37	211-0691-00	B010100	B010623	2	SCREW,MACHINE:6-32 X 0.625,PNH,STL	93907	ORDER BY DESCR
	211-0712-00	B010624		2	SCR,ASSEM WSHR:6-32 X 1.25,PNH,STL,TORX (END ATTACHING PARTS)	01536	ORDER BY DESCR
-38	213-0882-00			1	SCREW,TPG,TR:6-32 X 0.437 TAPTITE,PNH,STL (END ATTACHING PARTS)	83385	ORDER BY DESCR
					REAR COVER INCLUDES:		
-39	334-5964-00			1	.MARKER,IDENT:MKD CAUTION	80009	334-5964-00
	334-6265-00			1	MARKER,IDENT:MKD CAUTION (UNITED KINGDOM ONLY)	80009	334-6265-00
	334-6294-00			1	MARKER,IDENT:MKD CAUTION (SONY/TEK ONLY)	80009	334-6294-00

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
1-40	200-3130-00			1		COVER,FAN:ALUMINUM	80009	200-3130-00





REV MAY 1987

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-1	441-1571-00			1	CHASSIS,SCOPE:FRONT,L FRAME	80009	441-1571-00
-2	441-1591-00			1	CHASSIS,SCOPE:SIDE	80009	441-1591-00
					(ATTACHING PARTS)		
-3	211-0325-00			2	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
-4	211-0379-00			2	SCREW,MACHINE:4-40 X 0.312,FLH,CD PL,T-9	80009	211-0379-00
					(END ATTACHING PARTS)		
-5	334-5962-00			1	OVERLAY,PANEL:SIDE,PLOTTER STD	80009	334-5962-00
-6	129-1083-00	B010100	B012283	2	SPACER,POST:0.13 L,4-40,STEEL,0.2 OD	80009	129-1083-00
	129-1083-01	B012284		2	SPACER,POST:0.2 L,4-40,STEEL,0.188 HEX	80009	129-1083-01
-7	210-1307-00	B010855	B012283	2	WASHER,LOCK:0.115 ID,SPLIT,0.025 THK	86928	A384-25N
-8	386-5209-00			1	SUBPANEL,SIDE:	80009	386-5209-00
					(ATTACHING PARTS)		
-9	211-0371-00			4	SCREW,MACHINE:4-40 X 0.5,PNH,STL	83486	318-004-40416X
					(END ATTACHING PARTS)		
-10	361-1336-00			1	SPACER,PLATE:0.05 X 2.148 X 0.7,ALUMINUM	80009	361-1336-00
					(ATTACHING PARTS)		
-11	211-0370-00			2	SCREW,MACHINE:4-40 X 0.5,FLH,100 DEG,STL	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		
-12	----- -----			1	CKT BD ASSY:X-Y PLOTTER (SEE A20 REPL)		
					(ATTACHING PARTS)		
-13	211-0325-00			4	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
					(END ATTACHING PARTS)		
					OPTION 12 ONLY		
-14	334-5961-00			1	OVERLAY,PANEL:SIDE RS232	80009	334-5961-00
-15	211-0371-00			2	SCREW,MACHINE:4-40 X 0.5,PNH,STL	83486	318-004-40416X
-16	129-1083-01			4	SPACER,POST:0.2 L,4-40,STEEL,0.188 HEX	80009	129-1083-01
-17	210-1307-00			4	WASHER,LOCK:0.115 ID,SPLIT,0.025 THK	86928	A384-25N
-18	342-0743-01			1	INSUL,CKT BOARD:POLYCARBONATE	80009	342-0743-01
-19	----- -----			1	CIRCUIT BD ASSY:OPT MEMORY (SEE A23 REPL)		
					(ATTACHING PARTS)		
-20	211-0379-00			4	SCREW,MACHINE:4-40 X 0.312,FLH,CD PL,T-9	80009	211-0379-00
					(END ATTACHING PARTS)		
-21	----- -----			1	CKT BD ASSY:RS-232 OR GPIB(SEE A21,22 REPL)		
					(ATTACHING PARTS)		
-22	129-1095-00			4	SPACER,POST:0.43 L,4-40 INT/EXT,AL,0.25 HEX	80009	129-1095-00
-22.1	211-0325-00			6	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
					(END ATTACHING PARTS)		
-23	129-1085-00			2	SPACER,POST:0.25 L,4-40,BRS,0.25 HEX	80009	129-1085-00
-24	210-0056-00			2	WASHER,LOCK:#10 SPLIT,0.047 THK,SI BRZ	86928	ORDER BY DESCR
-25	343-0088-00			1	CLAMP,CABLE:0.062 DIA,PLASTIC	80009	343-0088-00
-26	334-6221-00			1	MARKER,IDENT:MKD CAUTION,BATTERY	80009	334-6221-00
-27	344-0116-00			1	RTNR,CAPACITOR:0.625 DIA,STEEL	90201	TH-17
					(ATTACHING PARTS)		
-28	211-0325-00			1	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
					(END ATTACHING PARTS)		
					OPTION 10 ONLY		
-29	334-5963-00			1	OVERLAY,PANEL:SIDE,GPIB	80009	334-5963-00
-30	211-0371-00			2	SCREW,MACHINE:4-40 X 0.5,PNH,STL	83486	318-004-40416X
-31	129-1085-00			2	SPACER,POST:0.25 L,4-40,BRS,0.25 HEX	80009	129-1085-00
-32	210-0056-00			2	WASHER,LOCK:#10 SPLIT,0.047 THK,SI BRZ	86928	ORDER BY DESCR
-33	342-0743-01			1	INSUL,CKT BOARD:POLYCARBONATE	80009	342-0743-01
-34	----- -----			1	CIRCUIT BD ASSY:OPT MEMORY (SEE A23 REPL)		
					(ATTACHING PARTS)		
-35	211-0379-00			4	SCREW,MACHINE:4-40 X 0.312,FLH,CD PL,T-9	80009	211-0379-00
					(END ATTACHING PARTS)		
-36	----- -----			1	CKT BDE ASSY:RS-232 OR GPIB(SEE A21,22 REPL		
					(ATTACHING PARTS)		
-37	129-1095-00			4	SPACER,POST:0.43 L,4-40 INT/EXT,AL,0.25 HEX	80009	129-1095-00
-37.1	211-0325-00			6	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
					(END ATTACHING PARTS)		
-38	129-1085-00			2	SPACER,POST:0.25 L,4-40,BRS,0.25 HEX	80009	129-1085-00
-39	210-0056-00			2	WASHER,LOCK:#10 SPLIT,0.047 THK,SI BRZ	86928	ORDER BY DESCR

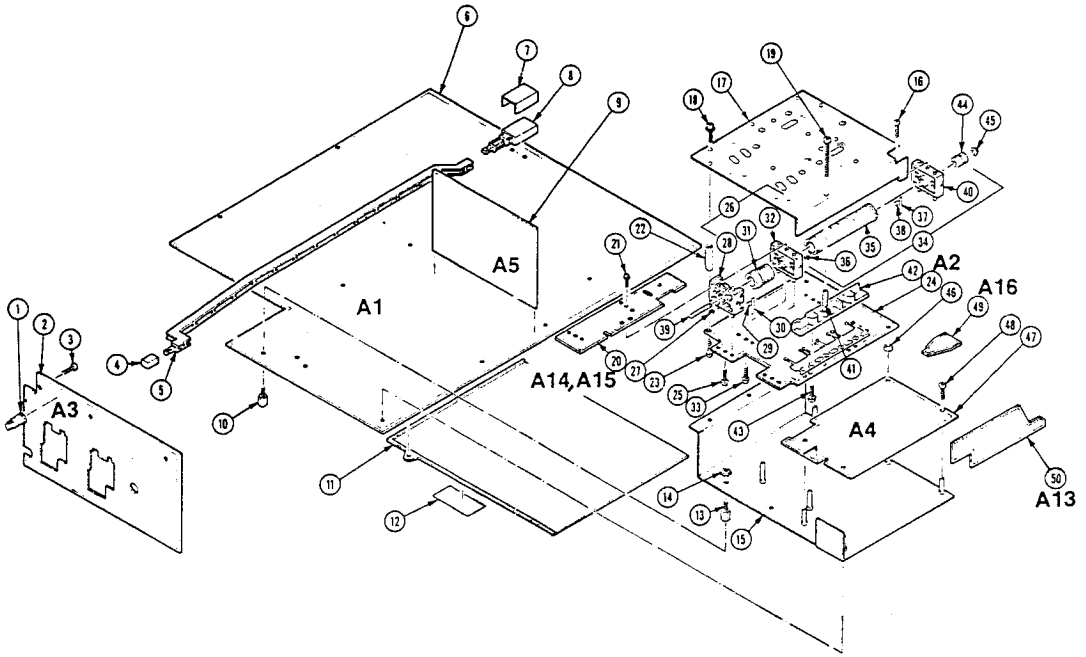
Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
-40	343-0088-00			1	CLAMP,CABLE:0.062 DIA,PLASTIC	80009	343-0088-00
-41	334-6221-00			1	MARKER,IDENT:MKD CAUTION,BATTERY	80009	334-6221-00
-42	211-0325-00			1	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
	344-0116-00			1	RTNR,CAPACITOR:0.625 DIA,STEEL (ATTACHING PARTS)	90201	TH-17
-43	211-0325-00			1	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9 (END ATTACHING PARTS)	01536	ORDER BY DESCR
-44	407-3456-00	B010100	B022559	1	BRKT,CHAS MTG:FRONT STORAGE	80009	407-3456-00
	407-3456-01	B022560		1	BRKT,CHAS MTG:FRONT STORAGE (ATTACHING PARTS)	80009	407-3456-01
	211-0325-00	B022560		1	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
-45	213-0881-00			2	SCREW,TPG,TR:6-32 X 0.25 TYPE TT,FILH,STL (END ATTACHING PARTS)	83385	ORDER BY DESCR
-46	361-1192-00	B010100	B022529	1	SPACER,SLEEVE:0.45 L X 0.25 ID,AL	80009	361-1192-00
-47	214-3375-00			1	LEVER,SWITCH:AC-GND-DC,PLASTIC	80009	214-3375-00
-48	407-3217-00			1	BRACKET,GROUND:ALUMINUM (ATTACHING PARTS)	TK1570	ORDER BY DESCR
-49	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL (END ATTACHING PARTS)	78189	211-041800-00
-50	386-4443-00			1	SUPPORT,SHIELD:CRT,FRONT,PLASTIC	80009	386-4443-00
-51	337-2774-00			1	SHIELD,ELEC:CRT,STEEL	23740	C-2059
-52	334-1951-00			1	MARKER,IDENT:MKD WARNING,CRT VOLTAGES	22670	ORDER BY DESCR
-53	334-1379-00			1	MARKER,IDENT:MKD HI VACUUM	22670	ORDER BY DESCR
-54	----- -----			1	DELAY LINE: (SEE DL9210 REPL) (ATTACHING PARTS)		
-55	213-0882-00			4	SCREW,TPG,TR:6-32 X 0.437 TAPTITE,PNH,STL (END ATTACHING PARTS)	83385	ORDER BY DESCR
					DELAY LINE ASSEMBLY INCLUDES:		
-56	346-0121-00			2	.STRAP,TIEDOWN,E:6.125 L,NYLON	06383	PLC1.5I-S8
-57	346-0128-00			1	.STRAP,TIEDOWN,E:8.0 L X 0.1 W,NYLON	06383	PLT2M
	210-0802-00	B010100	B021267	1	.WASHER,FLAT:0.15 ID X 0.312 OD X 0.032,STL	12327	ORDER BY DESCR
	210-1426-00	B021268		2	.EYELET,METALLIC:0.2 X 0.345,BRS	TK0869	ORDER BY DESCR
	343-1309-00	B021268		2	.CLAMP,CABLE:0.25 DIA,STEEL	75272	ORDER BY DESCR
-58	136-0830-00			1	SKT,PL-IN ELEK:CRT SOCKET ASSY (CRT SKT IS SUBPART OF A1 MAIN BOARD ASSY)	80009	136-0830-00
-59	214-1061-05			1	SPRING,GROUND:PLATED	TK1326	ORDER BY DESCR
-60	426-1766-00			1	MOUNT,RESILIENT:CRT,REAR	80009	426-1766-00
-61	200-2519-00			1	CAP,CRT SOCKET:NATURAL LEXAN	80009	200-2519-00
-62	627-0005-00			1	SHIELD ASSEMBLY:POWER SUPPLY	80009	627-0005-00
-63	337-3200-00			1	.SHIELD,ELEC:POWER SUPPLY (ATTACHING PARTS)	80009	337-3200-00
-63.1	211-0305-00			1	.SCR,ASSEM WSHR:4-40 X 0.437,PNH,STL,T9 (END ATTACHING PARTS)	01536	ORDER BY DESCR
-64	348-0555-00			1	.GROMMET,PLASTIC:SIL GY,U SHAPE,0.52 ID	80009	348-0555-00
-65	344-0347-00			1	.CLIP,ELECTRICAL:ANODE,0.72 OD,NYLON	80009	344-0347-00
-66	334-4251-00			1	.MARKER,IDENT:MKD CAUTION	07416	ORDER BY DESCR
-67	344-0334-00			1	CLIP,CIRCUIT BD:PLASTIC	80009	344-0334-00
-68	----- -----			1	FAN,TUBEAXIAL:(SEE B9965 REPL) (ATTACHING PARTS)		
-69	211-0086-00			2	SCREW,MACHINE:4-40 X 0.75,FLH,100 DEG,STL	80009	211-0086-00
-70	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-71	213-0926-00			2	SCREW,TPG,TR:4-40 X 0.5,TYPE TT,PNH,STL (END ATTACHING PARTS)	TK1543	829-07625
-72	200-2845-00			1	COVER,CKT BD:LINE FILTER (SUBPART OF A6 EMI FILTER BOARD)	80009	200-2845-00
-73	407-2729-00			1	BRACKET,HEAT SK:ALUMINUM (ATTACHING PARTS)	80009	407-2729-00
-74	211-0305-00			1	SCR,ASSEM WSHR:4-40 X 0.437,PNH,STL,T9	01536	ORDER BY DESCR
-75	211-0303-00			2	SCREW,MACHINE:4-40 X 0.25,FLH 100 DEG,STL	93907	ORDER BY DESCR
	210-0586-00			1	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL (END ATTACHING PARTS)	78189	211-041800-00
-76	343-1025-00			1	RETAINER,XSTR: (ATTACHING PARTS)	80009	343-1025-00
-77	211-0379-00			1	SCREW,MACHINE:4-40 X 0.312,FLH,CD PL,T-9	80009	211-0379-00

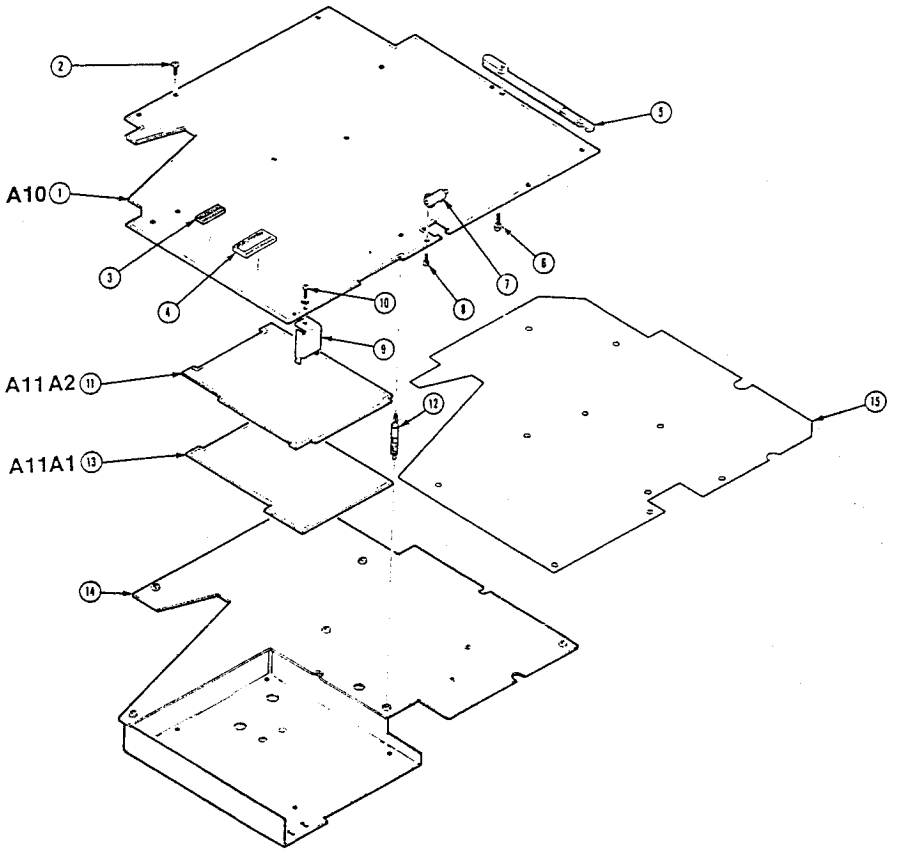
Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-78	210-0586-00			1	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL (END ATTACHING PARTS)	78189	211-041800-00
-79	342-0582-00			1	INSULATOR,PLATE:TRANSISTOR,CERAMIC	80009	342-0582-00
-80	343-0969-00			1	RETAINER,XSTR: (ATTACHING PARTS)	80009	343-0969-00
-81	211-0379-00			1	SCREW,MACHINE:4-40 X 0.312,FLH,CD PL,T-9	80009	211-0379-00
-82	210-0408-00			1	NUT,PLAIN,HEX:6-32 X 0.312,BRS CD PL (END ATTACHING PARTS)	73743	3040-402
-83	342-0555-00			1	INSULATOR,PLATE:HEAT SINK,ALUMINA	80009	342-0555-00
-84	----- -----			1	LINE FILTER ASSY:(SEE FL9001 REPL) (ATTACHING PARTS)		
-85	211-0380-00			2	SCREW,MACHINE:4-40 X 0.375,FLH,CD PL,T-9	80009	211-0380-00
-86	210-0583-00			2	NUT,PLAIN,HEX:0.25-32 X 0.312,BRS CD PL (END ATTACHING PARTS)	73743	2X-20319-402
-87	386-2996-01			1	SUPPORT,CHASSIS: (ATTACHING PARTS)	80009	386-2996-01
-88	213-0881-00			2	SCREW,TPG,TR:6-32 X 0.25 TYPE TT,FILH,STL (END ATTACHING PARTS)	83385	ORDER BY DESCR
-89	334-3379-02			1	MARKER,IDENT:MARKED GROUND SYMBOL	22670	ORDER BY DESCR
-90	210-0202-00			1	TERMINAL,LUG:0.146 ID,LOCKING,BRZ TIN PL (ATTACHING PARTS)	86928	A-373-158-2
-91	210-0457-00			1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL (END ATTACHING PARTS)	78189	511-061800-00
-92	200-1388-03			1	COVER,FUSE LEAD:POLYURETHANE	80009	200-1388-03
-93	200-2264-00			1	CAP,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
-94	204-0833-00			1	BODY,FUSEHOLDER:3AG & 5 X 20MM FUSES	TK0861	031 1653 (FEU)
-95	210-1039-00			1	WASHER,LOCK:0.521 ID,INT,0.025 THK,SST	24931	ORDER BY DESCR
-96	----- -----			1	CKT BD ASSY:EMI FILTER (SEE A6 REPL) (ATTACHING PARTS)		
-97	211-0379-00			2	SCREW,MACHINE:4-40 X 0.312,FLH,CD PL,T-9 (END ATTACHING PARTS)	80009	211-0379-00
					EMI FILTER BOARD ASSEMBLY INCLUDES:		
-98	129-0999-00			2	.SPACER,POST:0.485 L,4-40 INT/EXT,STL (ATTACHING PARTS)	80009	129-0999-00
-99	210-0586-00			2	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL (END ATTACHING PARTS)	78189	211-041800-00
-100	214-3327-01			3	HINGE,CKT BOARD:11.6 L,PLASTIC (ATTACHING PARTS)	80009	214-3327-01
-101	211-0305-00	B010100	B010134	3	SCR,ASSEM WSHR:4-40 X 0.437,PNH,STL,T9	01536	ORDER BY DESCR
	211-0332-00	B010135		3	SCR,ASSEM WSHR:4-40 X 0.5,PNH,STL,T9 (END ATTACHING PARTS)	01536	ORDER BY DESCR
-102	441-1592-00			1	CHASSIS,SCOPE:REAR	80009	441-1592-00
-103	342-0563-00			2	INSULATOR,PLATE:TRANSISTOR	18565	69-11-8805-1674
-104	----- -----			1	SEMICOND DVC,DI:(SEE CR970) ATTACHING PARTS		
-105	210-0586-00	B010100	B021444	1	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
	210-0551-00	B021445		1	NUT,PLAIN,HEX:4-40 X 0.25,ST CD PL	TK0435	ORDER BY DESCR
-106	210-0004-00	B022078		1	WASHER,LOCK:#4 INTL,0.015 THK,STL	77900	1204-00-00-0541C
-107	210-1171-00			1	WASHER,SHLDR:0.12 X 0.143 X 0.07,NYLON END ATTACHING PARTS	00261	A7148516P2

Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
377-0512-01			5	INSERT,KNOB:0.172 ID X 0.28 OD X 0.64,NYL	80009	377-0512-01
----- -----			1	CKT BD ASSY:FRONT PANEL (SEE A3 REPL)		
				(ATTACHING PARTS)		
211-0325-00			3	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
210-1011-00	B011281		1	WASHER,FLAT:0.13 X 0.375 X 0.01,NYLON	83309	ORDER BY DESCR
				(END ATTACHING PARTS)		
366-1480-03			1	PUSH BUTTON:BLACK,OFF	80009	366-1480-03
384-1576-01			1	EXTENSION SHAFT:12.544 L,PLASTIC	80009	384-1576-01
----- -----			1	CKT BD ASSY:MAIN (SEE A1 REPL)		
200-2735-00			1	.COVER,POWER SW:BLACK,POLYCARBONATE	80009	200-2735-00
----- -----			1	.SWITCH,PUSH: (SEE S901 REPL)		
361-1047-00			1	.SPACER,VAR RES:0.3 X 0.615 X 0.55,PLSTC	80009	361-1047-00
----- -----			1	CKT BD ASSY:ALT SWEEP (SEE A5 REPL)		
129-0999-00			1	SPACER,POST:0.485 L,4-40 INT/EXT,STL	80009	129-0999-00
337-2773-01			1	SHIELD,ELEC:PWR SPLY,LWR,PLSTC,W/MRKR	80009	337-2773-01
337-2773-02			1	SHIELD,ELEC:POWER SUPPLY,LOWER PLASTIC	80009	337-2773-02
334-4251-00			1	MARKER,IDENT:MKD CAUTION	07416	ORDER BY DESCR
129-0906-00			1	SPACER,POST:0.685 L,4-40 INT/EXT,AL	80009	129-0906-00
				(ATTACHING PARTS)		
210-0586-00			1	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
				(END ATTACHING PARTS)		
337-3291-00			1	SHIELD,ELEC:SW BD,BOTTOM	80009	337-3291-00
				(ATTACHING PARTS)		
211-0325-00			1	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
				(END ATTACHING PARTS)		
337-3201-01			1	SHIELD,ATTEN:TOP	80009	337-3201-01
				(ATTACHING PARTS)		
211-0325-00			2	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
211-0332-00	B010400		1	SCR,ASSEM WSHR:4-40 X 0.5,PNH,STL,T9	01536	ORDER BY DESCR
211-0326-00			2	SCREW,MACHINE:4-40 X 1.25,PNH,STL	83486	ORDER BY DESCR
				(END ATTACHING PARTS)		
----- -----			2	CKT BD ASSY:LOGIC (SEE A14,A15 REPL)		
				(ATTACHING PARTS)		
211-0325-00			2	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
				(END ATTACHING PARTS)		
129-0988-00			1	SPACER,POST:0.966 L,4-40 EA END,AL	80009	129-0988-00
				(ATTACHING PARTS)		
211-0325-00			1	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
				(END ATTACHING PARTS)		
----- -----			1	CKT BD ASSY:ATTENUATOR (SEE A2 REPL)		
				(ATTACHING PARTS)		
211-0302-00			2	SCR,ASSEM WSHR:4-40 X 0.75,PNH,STL,TORX DR	01536	ORDER BY DESCR
				(END ATTACHING PARTS)		
				ATTENUATOR BOARD ASSEMBLY INCLUDES:		
----- -----			2	.SW ASSY:ACTUATOR,COUPLING (SEE S1,S51 REPL)		
210-0406-00			2	..NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
401-0370-01			2	..BEARING,CAM SW:END,0.6 DIA	80009	401-0370-01
214-1752-00			4	..ROLLER,DETENT:0.125 OD X 0.16,SST	80009	214-1752-00
214-1126-01			4	..SPRING,FLAT:0.7 X 0.125,CU BE GRN CLR	80009	214-1126-01
105-0934-01			2	..ACTUATOR,CAM SW:AC-GND-DC	80009	105-0934-01
401-0369-00			2	.BEARING,CAM SW:CENTER,0.6 DIA	80009	401-0369-00
				(ATTACHING PARTS)		
211-0325-00			2	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
				(END ATTACHING PARTS)		
----- -----			2	.SW ASSY:ACTUATOR,V/DIV (SEE S10,S60 REPL)		
105-0935-01			2	.:ACTUATOR,CAM SW:ATTENUATOR	80009	105-0935-01
210-0406-00			2	..NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
214-1126-01			2	..SPRING,FLAT:0.7 X 0.125,CU BE GRN CLR	80009	214-1126-01
214-1126-02			2	..SPRING,FLAT:0.7 X 0.125,CU BE RED CLR	80009	214-1126-02
214-1752-00			4	..ROLLER,DETENT:0.125 OD X 0.16,SST	80009	214-1752-00
376-0209-00			2	..CPLG,SHAFT,RGD:0.127 ID,PLASTIC	80009	376-0209-00
401-0370-00			2	..BEARING,CAM SW:END,0.6 DIA	80009	401-0370-00
361-1218-00			2	.SPACER,SLEEVE:0.738 L X 0.13 ID,BRS	80009	361-1218-00
343-1020-00			2	.RETAINER,CONT:ABS GRAY	80009	343-1020-00
				(ATTACHING PARTS)		
211-0325-00			4	.SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
3-						(END ATTACHING PARTS)		
-44	376-0051-01			2		.CPLG,SHAFT,FLEX:0.127 ID X 0.375 OD,DELRIN	80009	376-0051-01
-45	361-1300-00			2		.SPACER,BEARING:0.115 ID X 0.2 OD,BRASS	80009	361-1300-00
-46	361-1191-00	B010100	B012361	1		.SPACER,CKT BD:0.222 X 0.125 X 0.25,	80009	361-1191-00
	361-1166-00	B012362		1		.SPACER,SLEEVE:0.228 L X 0.162 ID,BRS	80009	361-1166-00
-47	----- -----			1		CKT BD ASSY:TIMING (SEE A4 REPL) (ATTACHING PARTS)		
-48	211-0325-00			3		SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9 (END ATTACHING PARTS)	01536	ORDER BY DESCR
-49	----- -----			1		CKT BD ASSY:SWEEP REFERENCE (SEE A16 REPL)		
-50	----- -----			1		CKT BD ASSY:SWP INTERFACE (SEE A13 REPL)		
	174-0160-00			1		CA ASSY,SP,ELEC:2,26 AWG,4.0 L,1-2 (FROM A1 TO POWER ON LIGHT)	80009	174-0160-00
	176-0045-00			1		BRAID,WIRE:24 STRANDS,36 AWG,TINNED COPPER	70903	5112R424/36
	210-1011-00			1		WASHER,FLAT:0.13 X 0.375 X 0.01,NYLON	83309	ORDER BY DESCR
	344-0367-00	B010100	B011570	3		CLIP,GROUND:CU-BE	80009	344-0367-00
	214-2270-00	B011571	B022102	1		CONTACT,ELEC:CRT TO SHLD,CU-BE CU-SN-ZN PL	80009	214-2270-00
	344-0367-00	B011571		1		CLIP,GROUND:CU-BE	80009	344-0367-00

FIG. 2 CHASSIS,REAR




A10 1
2
3
4
5
6
7
8
9
10
A11A2 11
12
15
A11A1 13
14

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 5-28-87 Change Reference: M63744

Product: 2230 SERVICE Manual Part No.: 070-4999-00

DESCRIPTION Product Group 41

EFFECTIVE SERIAL NUMBER: B023320

REPLACEABLE MECHANICAL PARTS LIST CHANGES

CHANGE TO:

2-20	211-0343-00	4	SCREW,MACHINE: 4-40 X 0.25,TRUSS HEAD,STL CD PL,TORX,T9
2-28	211-0343-00	1	SCREW,MACHINE: 4-40 X 0.25,TRUSS HEAD,STL CD PL,TORX,T9
2-35	211-0343-00	4	SCREW,MACHINE: 4-40 X 0.25,TRUSS HEAD,STL CD PL,TORX,T9
2-43	211-0343-00	1	SCREW,MACHINE: 4-40 X 0.25,TRUSS HEAD,STL CD PL,TORX,T9

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 5-22-87 Change Reference: M63636

Product: 2230 SERVICE Manual Part No.: 070-4999-00

DESCRIPTION Product Group 41

EFFECTIVE SERIAL NUMBER: B023219

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A1R908	315-0222-00	RES,FXD,FILM: 2.2K OHM,5%,0.25W
		(CHASSIS PARTS)
Q9070	151-1245-00	TRANSISTOR: MOSFET,N-CHAN,TO-220

ADD:

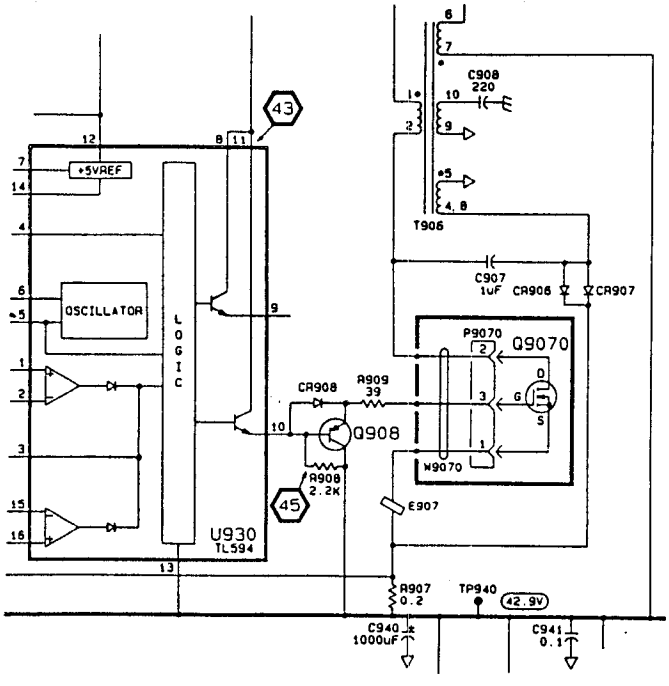
A1CR906	152-0808-00	SEMICOND DVC,DI: RECT,SI,400V,1.5 A,50 NS

DIAGRAM CHANGES

DIAGRAM 8 POWER INPUT, PREREGULATOR, & INVERTER

Change the value of resistor R908 to 2.2K Ω.
Add diode CR906 in parallel with CR907.

See the partial digram below for these changes.



MANUAL CHANGE INFORMATION

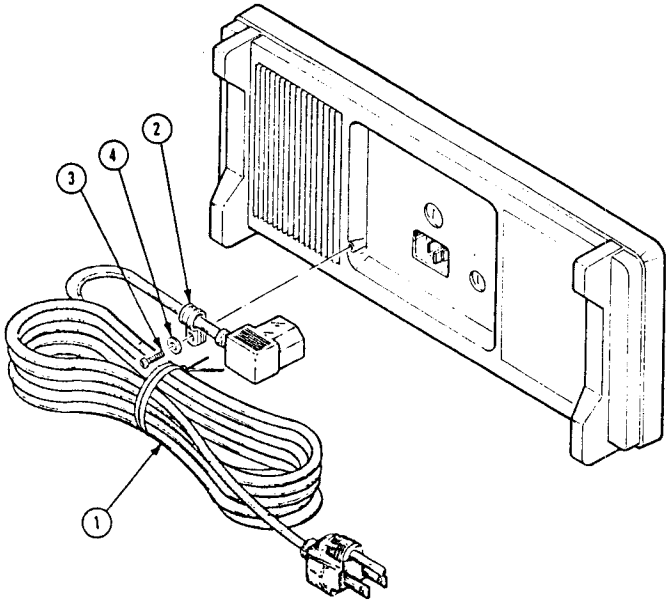
At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

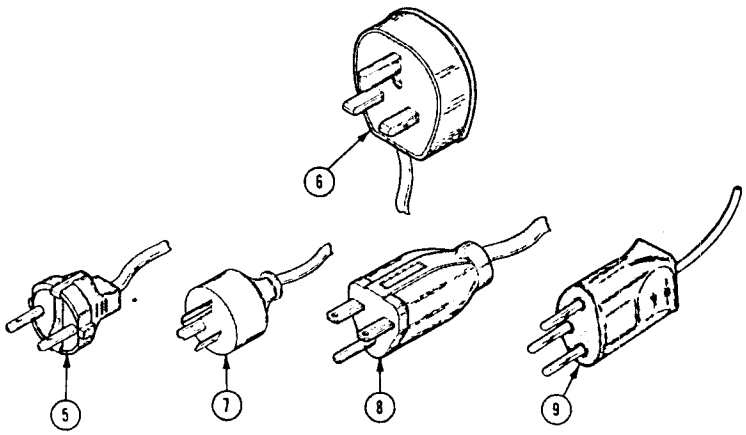
Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
4-1	----- -----			1	CKT BD ASSY:STORAGE (SEE A10 REPL)		
					(ATTACHING PARTS)		
-2	211-0325-00	B010100	B011015	4	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
	211-0379-00	B011016	B011570	4	SCREW,MACHINE:4-40 X 0.312,FLH,CD PL,T-9	80009	211-0379-00
	211-0379-00	B011571		2	SCREW,MACHINE:4-40 X 0.312,FLH,CD PL,T-9	80009	211-0379-00
	211-0325-00	B011571	B022102	2	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
	211-0305-00	B022103		1	SCR,ASSEM WSHR:4-40 X 0.437,PNH,STL,T9	01536	ORDER BY DESCR
	211-0325-00	B022103		1	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
					(END ATTACHING PARTS)		
	211-0305-00				STORAGE BOARD ASSEMBLY INCLUDES:		
-3	136-0755-00			3	.SCR,ASSEM WSHR:4-40 X 0.437,PNH,STL,T9	01536	ORDER BY DESCR
-4	136-0757-00			3	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
	386-1130-00			1	.SKT,PL-IN ELEK:MICROCIRCUIT,40 DIP	09922	DILB40P-108
	343-0549-00	B010857		2	.INSULATOR,DISK:TRANSISTOR,NYLON	13103	7717-15N
				1	STRAP,TIEDOWN,E:0.091 W X 4.0 L,ZYTEL	06383	PLT1M
					(TO HOLD W4100 IN PLACE)		
-5	343-1098-00			1	RETAINER,CKT BD:PLASTIC	80009	343-1098-00
					(ATTACHING PARTS)		
-6	211-0304-00			1	SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,T9	01536	ORDER BY DESCR
					(END ATTACHING PARTS)		
-7	214-3327-01			3	HINGE,CKT BOARD:11.6 L,PLASTIC	80009	214-3327-01
					(ATTACHING PARTS)		
-8	211-0303-00	B010100	B010134	3	SCREW,MACHINE:4-40 X 0.25,FLH 100 DEG,STL	93907	ORDER BY DESCR
	211-0323-00	B010135		3	SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG,STL	83385	ORDER BY DESCR
					(END ATTACHING PARTS)		
-9	361-1337-00			1	SPACER,BRACKET:CHROMATE	80009	361-1337-00
					(ATTACHING PARTS)		
-10	211-0325-00			1	SCR,ASSEM WSHR:4-40 X 0.25,PNH,STL,TORX T9	01536	ORDER BY DESCR
					(END ATTACHING PARTS)		
-11	----- -----			1	CKT BD ASSY:VECTOR GEN (SEE A11A2 REPL)		
-12	361-1303-00			4	SPACER,CKT BD:0.375 THK,POLYCARBONATE BLACK	80009	361-1303-00
-13	----- -----			1	CKT BD ASSY:IN/OUT (SEE A11A1 REPL)		
-14	441-1594-00	B010100	B022102	1	CHASSIS,SCOPE:CKT BD	80009	441-1594-00
	441-1594-01	B022103		1	CHASSIS,SCOPE:CKT BD	80009	441-1594-01
-15	342-0766-00			1	INSUL,CKT BD:POLYCARBONATE	80009	342-0766-00

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
					STANDARD ACCESSORIES		
	----- -----			2	PROBE,VOLTAGE:P6122,1.5M,10X W/ACCESSORIES		
	159-0023-00			1	FUSE,CARTRIDGE:3AG,2A,250V,SLOW BLOW	71400	MDX2
	131-3579-00			1	CONNECTOR ASSY:9 PIN,MALE W/HARDWARE	80009	131-3579-00
-1	161-0104-00			1	CABLE ASSY,PWR,:3 WIRE,98.0 L,W/RTANG CONN	16428	CH8352, FH-8352
-2	343-0003-00			1	CLAMP,LOOP:0.25 ID,PLASTIC	06915	E4 CLEAR ROUND
-3	213-0882-00			1	SCREW,TPG,TR:6-32 X 0.437 TAPTITE,PNH,STL	83385	ORDER BY DESCR
-4	210-0803-00			1	WASHER,FLAT:0.15 ID X 0.375 OD X 0.032	12327	ORDER BY DESCR
	016-0677-02			1	POUCH,ACCESSORY:	TK0174	016-0677-02
	070-4998-01			1	MANUAL,TECH:OPERATORS,2230	80009	070-4998-01
	070-5370-00			1	MANUAL,TECH:USERS GUIDE,2230	80009	070-5370-00
					OPTIONAL ACCESSORIES		
	070-5709-00			1	CARD,INFO:REFERENCE,2230 (OPTION 10,12 ONLY)	80009	070-5709-00
	070-5757-00			1	MANUAL,TECH:INSTR,2230 (OPTION 10,12 ONLY)	80009	070-5757-00
	070-6090-00			1	MANUAL,TECH:RS232/GPIB (OPTION 10,12 ONLY)	80009	070-6090-00
	020-0859-00			1	COMPONENT KIT:EUROPEAN	80009	020-0859-00
	200-2265-00			1	.CAP,FUSEHOLDER:5 X 20MM FUSES	TK0861	FEK 031.1663
	343-0170-00	B021930		1	.RTNR,CA TO CA:U/W 0.25 OD CABLES	80009	343-0170-00
-5	161-0104-06			1	.CABLE ASSY,PWR,:3 X 0.75MM SQ,220V,98.0 L	S3109	ORDER BY DESCR
	020-0860-00			1	COMPONENT KIT:UNITED KINGDOM	80009	020-0860-00
	343-0170-00	B021930		1	.RTNR,CA TO CA:U/W 0.25 OD CABLES	80009	343-0170-00
	200-2265-00			1	.CAP,FUSEHOLDER:5 X 20MM FUSES	TK0861	FEK 031.1663
-6	161-0104-07			1	.CABLE ASSY,PWR,:3 X 0.75MM SQ,240V,98.0 L	TK1373	A25UK-RA
	020-0861-00			1	COMPONENT KIT:AUSTRALIAN	80009	020-0861-00
	343-0170-00	B021930		1	.RTNR,CA TO CA:U/W 0.25 OD CABLES	80009	343-0170-00
	200-2265-00			1	.CAP,FUSEHOLDER:5 X 20MM FUSES	TK0861	FEK 031.1663
-7	161-0104-05			1	.CABLE ASSY,PWR,:3,18 AWG,240V,98.0 L	S3109	ORDER BY DESCR
	020-0862-00			1	COMPONENT KIT:NORTH AMERICAN	80009	020-0862-00
	343-0170-00	B021930		1	.RTNR,CA TO CA:U/W 0.25 OD CABLES	80009	343-0170-00
	200-2264-00			1	.CAP,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
-8	161-0104-08			1	.CABLE ASSY,PWR,:3,18 AWG,240V,98.0 L	70903	ORDER BY DESCR
	020-0863-00			1	COMPONENT KIT:SWISS	80009	020-0863-00
	343-0170-00	B021930		1	.RTNR,CA TO CA:U/W 0.25 OD CABLES	80009	343-0170-00
	200-2265-00			1	.CAP,FUSEHOLDER:5 X 20MM FUSES	TK0861	FEK 031.1663
-9	161-0167-00			1	.CABLE ASSY,PWR,:3.0 X 0.75,6A,240V,2.5M L	S3109	ORDER BY DESCR
	013-0191-00			1	TIP,PROBE:W/ACTUATOR	80009	013-0191-00
	016-1003-00			1	ADAPTER,RACK:	80009	016-1003-00
	016-0566-00			1	VISOR,CRT:	80009	016-0566-00
	016-0792-01			1	CASE,CARRYING:24.5 X 16.5 X 11.5	TK1336	ORDER BY DESCR
	016-0848-00			1	COVER,PROT:WATERPROOF VINYL	80009	016-0848-00
	346-0199-00			1	STRAP,CARRYING:MKD TEKTRONIX	80009	346-0199-00
	070-4999-00			1	MANUAL,TECH:SERVICE,2230	80009	070-4999-00


1
2
3
4


5
6
7
8
9